EVM User's Guide: UCC33420Q1-EVM

UCC33420EVM-080 Evaluation Module for Automotive and Industrial Applications

Description

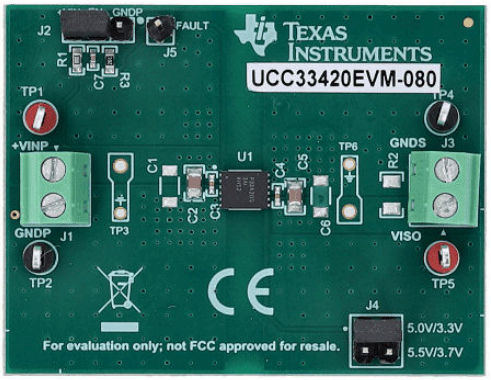
The UCC33420EVM-080 is intended to allow designers to evaluate the performance and capabilities of UCC33xx0 family of automotive and industrial devices. UCC33420 is an isolated DC/DC converter module able to deliver 1.5W with 3kVrms of isolation in a very small and compact 4mmx5mmx1mm VSON-12 package, reducing footprint and providing a high-power density. UCC334x0 devices can operate from 4.5V to 5.5V and UCC330x0 from 3.0V to 5.5V at the input side. UCC33x20 devices can regulate the secondary side to 5V or 5.5V and UCC33x10 to 3.3V or 3.7V configuring the SEL pin. This EVM demonstrates typical isolated bias supply voltages used in automotive and industrial applications.

Features

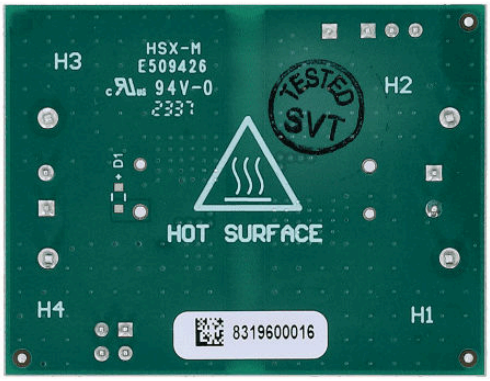
- UCC33420-Q1 1.5W DC/DC isolated converter module with isolated bias supply power.
- Transformer, power and control stage fully integrated in a 4mmx5mmx1mm VSON-12 package with 12 pins
- AEC-Q100, 3-kVrms isolation, protection features and low electromagnetic emissions
- EVM demonstrates an isolated bias supply used in automotive and industrial applications

Applications

- Factory automation PLC modules
- EV charging infrastructure
- Battery Management Systems (BMS)
- HEV/EV OBC and DC/DC converter
- Isolated power for voltage and current sensors
- Isolated bias power for digital isolators
- Isolated bias power for RS-485, RS-422 and CAN



UCC33420EVM-080 (Top View)



UCC33420EVM-080 (Bottom View)

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1 Evaluation Module Overview

1.1 Introduction

This user's guide provides directions for use of the UCC33420EVM-080 to evaluate the UCC33420-Q1 high frequency integrated transformer DC-DC converter, low emissions, 3 kV_{RMS} module from Texas Instruments. UCC33420-Q1 comes in a minimum footprint VSON-12 package which provides high-power density, 1.5W nominal power. The UCC33420-Q1 delivers class-leading efficiency in power conversion from the primary to the secondary side while removing the need for external transformers or power modules commonly required in existing designs. This integration allows for minimal printed circuit board (PCB) area as well as decreased height profile.

1.2 Kit Contents

Table 1-1. UCC33420EVM-080 Kit Contents

Designator	Description	Quantity
PCB1	UCC33420EVM-080 Circuit Board	1

1.3 Device Information

1.3.1 U1 Component Selection

The UCC33420-Q1 is the default IC used in the UCC33420EVM-080 but any of the alternate versions listed in Table 1-2can be used for evaluation. Each of the component versions listed in Table 1-2 are pin-to-pin compatible.

Table 1-2. UCC33x20-Q1 devices

General Part Number	Orderable Part Number	Input Voltage/Output Voltage/Isolation
UCC33420-Q1	PUCC33420QRAQRQ1	4.5V-5.5V/5.0V/3kV_{RMS}
UCC33420	PUCC33420RAQR	4.5V-5.5V/5.0V/3kV_{RMS}
UCC33020-Q1	PUCC33420QRAQRQ1	3.3V-5.5V/5.0V/3kV_{RMS}
UCC33020	PUCC33420RAQR	3.3V-5.5V/5.0V/3kV_{RMS}

If IC replacement is required, TI recommends to always use best practice soldering techniques which can include taking appropriate ESD precautions and having qualified personnel, skilled at surface mount soldering and board level rework.

1.3.2 UCC33420-Q1 Pin Definition

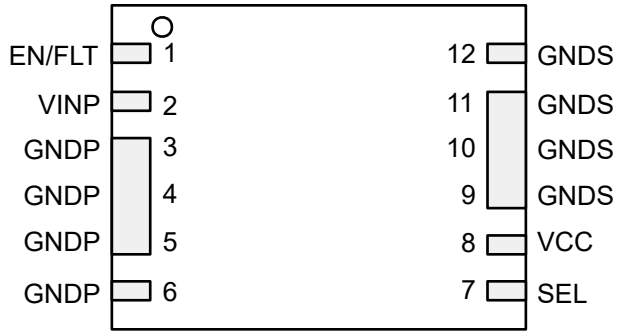

Figure 1-1. UCC33420-Q1 Package (Top View)

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Table 1-3. UCC33420-Q1 Pin Description

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN/FLT	1	I/O	Multi-functional enable input pin and output fault pin. Connect to microcontroller through an 18kΩ or greater pull-up resistor. **Enable input pin:** Forcing EN low disables the device. Pull high to enable normal device functionality. **Fault output pin:** This pin is pulled low for 200us to alert that power converter is shutdown due to a fault condition.
VINP	2	P	Primary input supply voltage. Connect parallel 15nF 0402, and 10µF ceramic bypass capacitors close to VINP to GNDP pins.
GNDP	3, 4, 5, 6	G	Power ground return connection for VINP.
SEL	7	I	VCC selection pin. VCC setpoint is 5V when SEL is connected to VCC and 5.5V when SEL is shorted to GNDS.
VCC	8	P	Isolated supply output voltage pin. Connect parallel 15nF 0402, and 22µF ceramic bypass capacitors close to VCC and GNDS pins.
GNDS	9, 10, 11, 12	G	Power ground return connection for VCC.

(1) P=Power, G=Ground, I=Input, 0=Output

1.4 Specification

Table 1-4. UCC33420-Q1 EVM Electrical Characteristics

VINP=5V, VCC=5V, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
VINP	Input voltage range	P_{VCC}=1.5W	4.5	5	5.5	V
I_{IN_FL}	Input current at full load	VINP=4.5V-5.5V, VCC=5.0V, I_{out}=300 mA		535		mA
I_{IN_NL}	Input current at no load	VINP =5.0V, VCC=5.0V, I_{out}=0 mA		7	15	mA
OUTPUT CHARACTERISTICS						
VCC	DC full load set-point	VINP=4.5V-5.5V, VCC=5.0V, I_{out}=300 mA	4.85	5	5.15	V
I_{out}	VCC load current range	VINP=4.5V-5.5V	0		300	mA
$VCC_{\%LD}$	Load regulation	VINP=5.0V, VCC=5.0V, I_{out} =0-300mA		0.5		%
$VCC_{(AC)}$	pk-to-pk AC ripple	20MHz bandwidth, VINP=5.0V, VCC=5.0V, I_{out}=300mA, T_A=25ºC, C_{OUT}=22uF		50	75	mV
P_{MAX}	Recommended maximum output power	VINP=5.0V, I_{out}=300mA, T_A=25ºC		1.5		W
SYSTEM CHARACTERISTICS						
η	Full load efficiency	VINP=5.0V, VCC=5.0V, I_{out}=300mA, T_A=25ºC, C_{OUT}=22uF		59		%
f_{SW}	Switching frequency			64.5		MHz

Table 1-5. UCC33020-Q1 EVM Electrical Characteristics

VINP=3.3V, VCC=5V, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
VINP	Input voltage range		3.0		5.5	V
I_{IN_FL}	Input current at full load	VINP=3.3V, VCC=5.0V, I_{out}=100 mA	390	415	450	mA
		VINP=5.0V, VCC=5.0V, I_{out}=200 mA	365	400	435	mA

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Table 1-5. UCC33020-Q1 EVM Electrical Characteristics (continued)

VINP=3.3V, VCC=5V, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN_NL}	Input current at no load	VINP =3.3V, VCC=5.0V, I_{out}=0 mA		7	15	mA
		VINP =5.0V, VCC=5.0V, I_{out}=0 mA		7	15	mA
OUTPUT CHARACTERISTICS						
VCC	DC full load set-point	VINP=3.3V, VCC=5.0V, I_{out}=0-100 mA	4.85	5	5.15	V
		VINP=5.0V, VCC=5.0V, I_{out}=0-200 mA	4.85	5	5.15	V
I_{out}	VCC load current range	VINP=3.3V, VCC=5.0V	0		100	mA
		VINP=5.0V, VCC=5.0V	0		200	mA
$VCC_{\%LD}$	Load regulation	VINP=3.3V, VCC=5.0V, I_{out} =0-100mA		0.2	0.4	%
		VINP=5.0V, VCC=5.0V, I_{out} =0-200mA		0.5	0.7	%
$VCC_{(AC)}$	pk-to-pk AC ripple	20MHz bandwidth, VINP=3.3V, VCC=5.0V, I_{out}=100mA, Ta=25ºC, C_{OUT}=22uF		50	75	mV
		20MHz bandwidth, VINP=5.0V, VCC=5.0V, I_{out}=200mA, Ta=25ºC, C_{OUT}=22uF		50	75	mV
P_{MAX}	Recommended maximum output power	VINP=3.3V, I_{out}=100mA, Ta=25ºC		0.5		W
		VINP=5.0V, I_{out}=200mA, Ta=25ºC		1		W
SYSTEM CHARACTERISTICS						
η	Full load efficiency	VINP=3.3V, VCC=5.0V, I_{out}=100mA, Ta=25ºC, C_{OUT}=22uF		50		%
		VINP=5.0V, VCC=5.0V, I_{out}=200mA, Ta=25ºC, C_{OUT}=22uF		52		%
f_{SW}	Switching frequency			64.5		MHz

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2 Hardware

2.1 EVM Setup and Operation

2.1.1 Recommended Test Equipment

1. V_{EN}: DC power supply: 5.0V, 10mA
2. VINP: DC power supply: 5.0V, 1A
3. I_{out}: Electronic load or fixed resistor: 5V, 500mA
4. (2) DVMs measuring DC voltage <10V
5. (2) DVMs measuring DC current <1.0A on I_{VINP} and I_{out}
6. Oscilloscope: 4 channel, 500MHz or higher, voltage probes, current probes
7. Minimum wire gauge 20 AWG to 22 AWG or heavier
8. Thermal camera or thermocouple to measure U1 case temperature

2.1.2 External Connections for Easy Evaluation

The UCC33420EVM-080 EVM utilizes screw terminals for easily connecting to VINP and VCC. EN connections are made through pin connectors. Connecting the appropriate ammeters and voltmeters, as shown in Figure 4-1, allows accurate EVM efficiency measurements.

Connecting Test Equipment:

1. Connect the VINP DC power supply capable of 4.5V<VINP<5.5V, 1A at J1:1-2 (VINP-GNDP). With the power supply disable, adjust the power supply to 5.0V, and set the current limit to 4A.
2. Connect a power supply capable of 5V, 100mA at J2:2-1 to serve as the pull up bias for EN/FLT. With the supply disabled, set to 3.3V/5.0V. As an option, the user can use the input power supply as a bias supply connecting a jumper to short +VINP and EN pins at J2:1-2 (top left corner).
3. Connect a variable load between J3:1 (VCC) and J3:2 (GNDS). If using an electronic load, then set to constant current (CC), 300mA. Leave the load disabled until the EVM is powered.
4. Some electronic loads are not able to regulate or stabilize CC when setting in the low mA range. Monitor the input current and load currents by inserting ammeters as shown in Figure 2-1. A current probe can be used with the oscilloscope to verify the stability of the DC current being regulated by an electronic load.

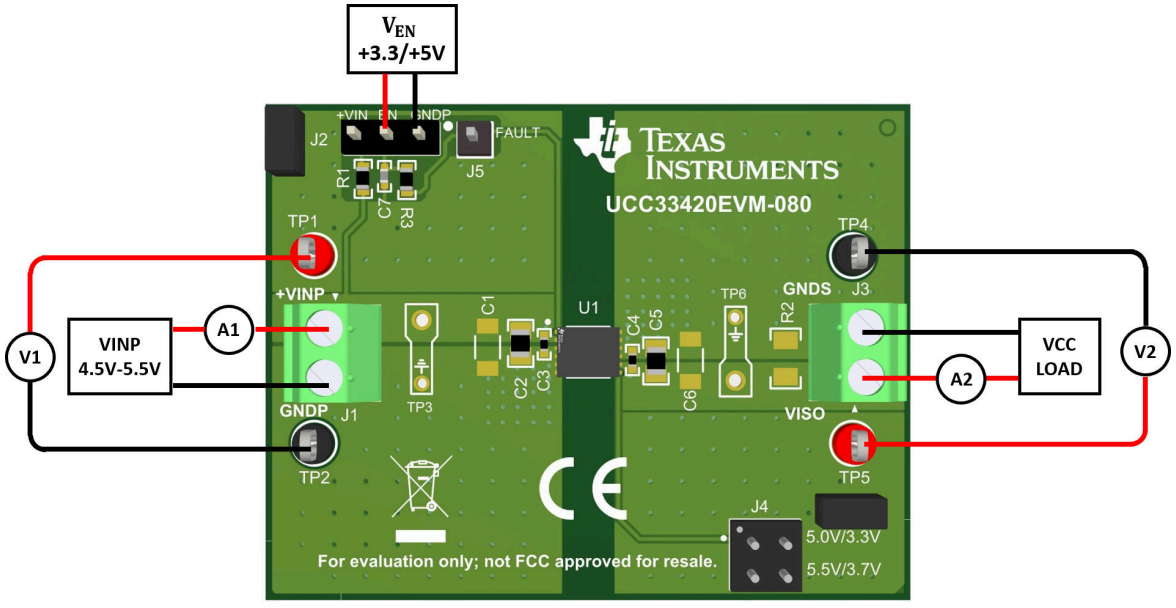

Figure 2-1. Typical Efficiency Measurement Setup

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2.1.3 Powering the EVM

WARNING

- Hot surface. Contact can cause burns. U1 package surface can reach temperatures of 100°C above ambient. Do not touch!
- Do not test this EVM unless trained in the proper safety, handling and testing of power electronics.

Power on for Start-up:

1. Verify VINP and V_{EN} power supplies are off/disabled and no voltage is applied to the DUT.
2. Verify the load on VCC is disabled.
3. Turn on the VINP DC power supply. Verify 5V is present at TP1-to-TP2.
4. Turn on the V_{EN} bias power supply. EVM is now enabled with VCC in regulation under no load condition.
5. Verify 5V present on VCC-GNDS.
6. Enable the 300mA load on VCC.
7. The UCC33420 is now regulating VCC and processing 1.5W of isolated output power.
8. Vary VINP between 4.5 V<VINP<5.5 V, vary I_{out} between 0 mA<I_{out}<300 mA.
9. Insert oscilloscope probes into TP3 and TP6 for measuring VINP and VCC startup, steady state and AC ripple voltage.

Power off for Shutdown:

1. Turn off V_{EN} power supply.
2. Disable I_{out} load.
3. Turn off VINP power supply.

2.1.4 EVM Test Points

Table 2-1 describes the various EVM test points, allowing easy access for connecting oscilloscope probes, DVM test leads and wire connections to lab test equipment as outlined in Section 2.1.1. Maintain separation between the primary side, GNDP, and secondary side, GNDS. Ensure that primary-side test points are not referenced to GNDS through improper test equipment insertion. Likewise, secondary-side test points are not to be referenced to GNDP through improper test equipment insertion.

Table 2-1. Input, Output, Test Point (I/O/TP) Description

PIN	I/O/TP	COLOR	DESCRIPTION		MIN	TYP	MAX	UNIT
J1	I	Green	VINP, primary input voltage.		4.5	5.0	5.5	V
J2:1-2	I	Black	EN, on			0		V
J2:2-3	I	Black	EN, off		0	V_{BIAS}	5.5	V
J4:1-2	O	Black	Selector 5.0V/3.3V output voltage.		0		5.7	V
J4:3-4	O	Black	Selector 5.5V/3.7V output voltage.		0		5.7	V
J3	O	Green	VCC, secondary output voltage.		0		5.7	V
TP1	TP	Red	VINP, primary input voltage test point.		4.5	5	5.5	V
TP2	TP	Black	GNDP, primary ground test point.			0		V
TP3	TP	PCB	VINP-to-GNDP, scope probe point.		4.5	5	5.5	V
TP4	TP	Black	GNDS, secondary ground test point.			0		V
TP5	TP	Red	VCC, secondary output voltage test point.		4.85	5	5.15	V
TP6	TP	PCB	VCC-to-GNDS, scope probe point.	SEL 5.0V	4.85	5	5.15	V
				SEL 5.5V	5.34	5.5	5.67	V

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2.1.5 Oscilloscope Probes: Probing the EVM

Using TP3 and TP6 Oscilloscope Probe PCB Test Points

The UCC33420-Q1 is a high frequency DC-DC module that requires careful measurement for accurately capturing transient events and measuring high frequency, AC ripple voltage. Remove the *witch hat* probe tip cover and ground lead from the scope probe. If scope probe ground springs are not available, wrap a piece of 22 AWG bare wire around the scope probe ground ring. Insert probe tip and ground into the EVM as shown in Figure 2-2.

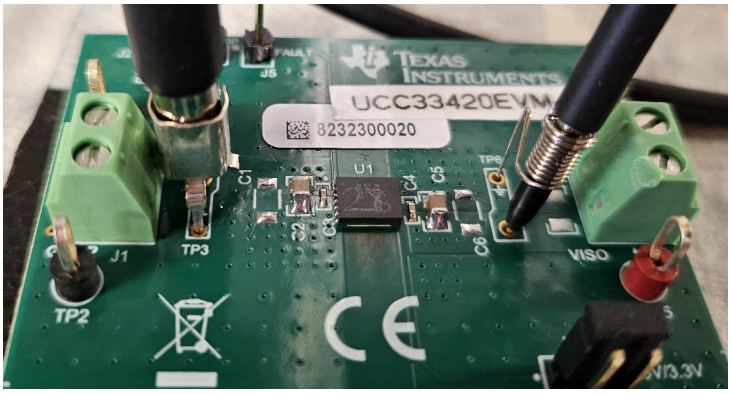

Figure 2-2. PCB Scope Probe Test Points

The EVM input (VINP, GNDP) and output nomenclature (VCC, GNDS) corresponds to what is commonly used when referring to isolated amplifiers that need to be biased from primary and secondary sides.

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3 Implementation Results

3.1 Schematic

Figure 3-1 shows the EVM electrical schematic. C1, C6, R2 and D1 are intentionally unpopulated as indicated by a red X placed directly over the component. The user can use C1 and C8 placeholders to add input or output capacitance as required for their systems.

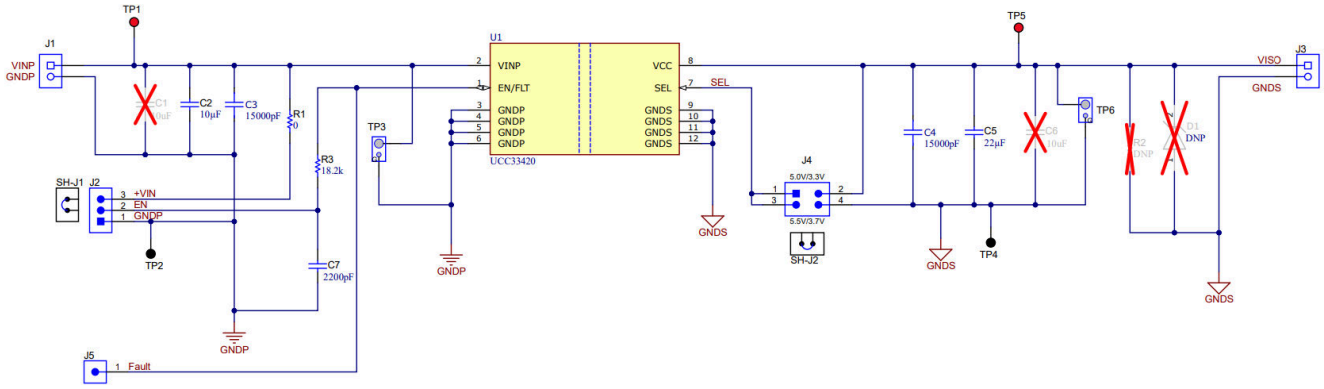

Figure 3-1. Schematic

3.2 Performance Data

UCC33420-Q1 VINP=5.0V, VCC=5.0V, T_A=25°C (unless otherwise noted).

UCC33020-Q1 VINP=3.3V, VCC=5.0V, T_A=25°C (unless otherwise noted).

3.2.1 Efficiency Data

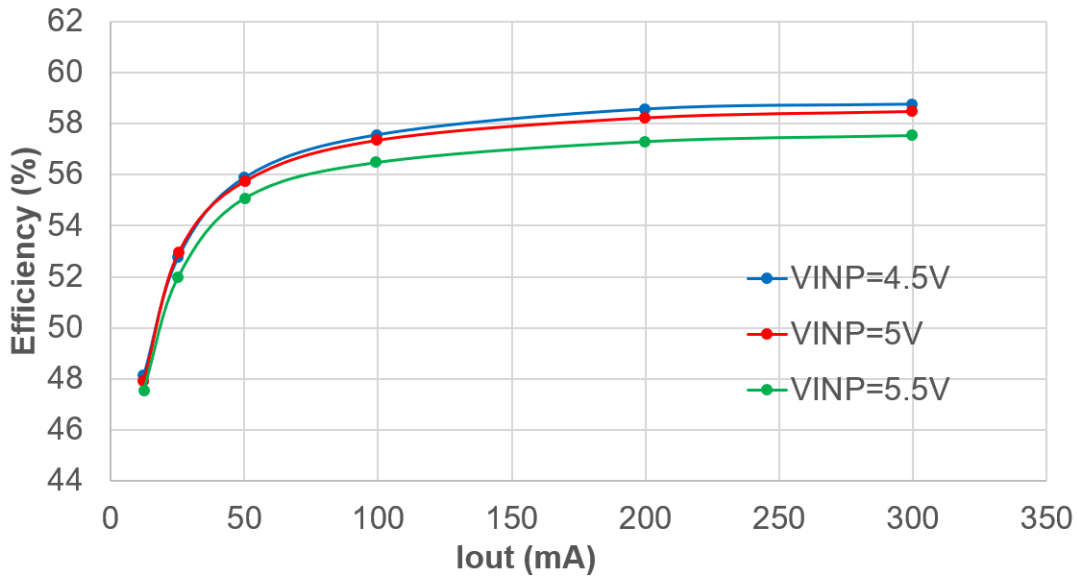

Figure 3-2. UCC33420-Q1 Efficiency VCC=5.0V

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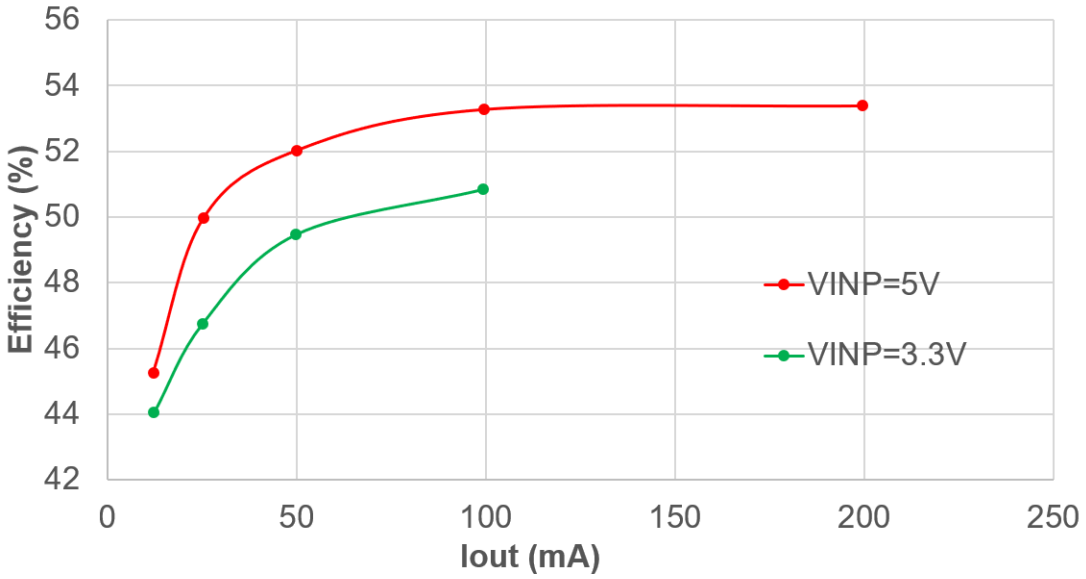

Figure 3-3. UCC33020-Q1 Efficiency VCC=5.0V

3.2.2 Regulation Data

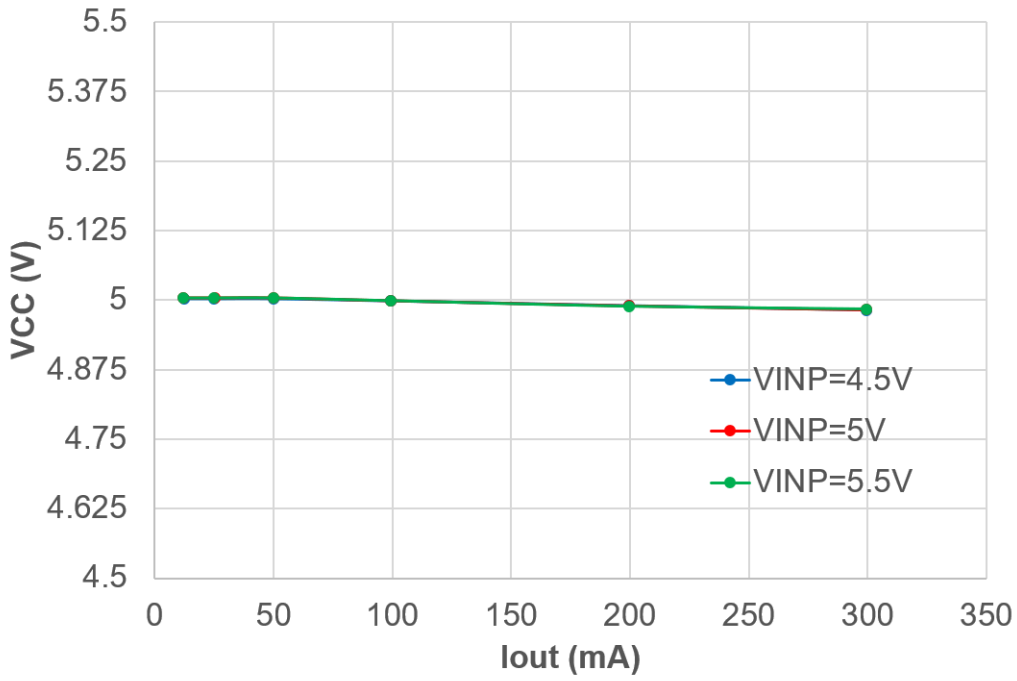

Figure 3-4. UCC33420-Q1 Regulation vs Load Current VCC=5.0V

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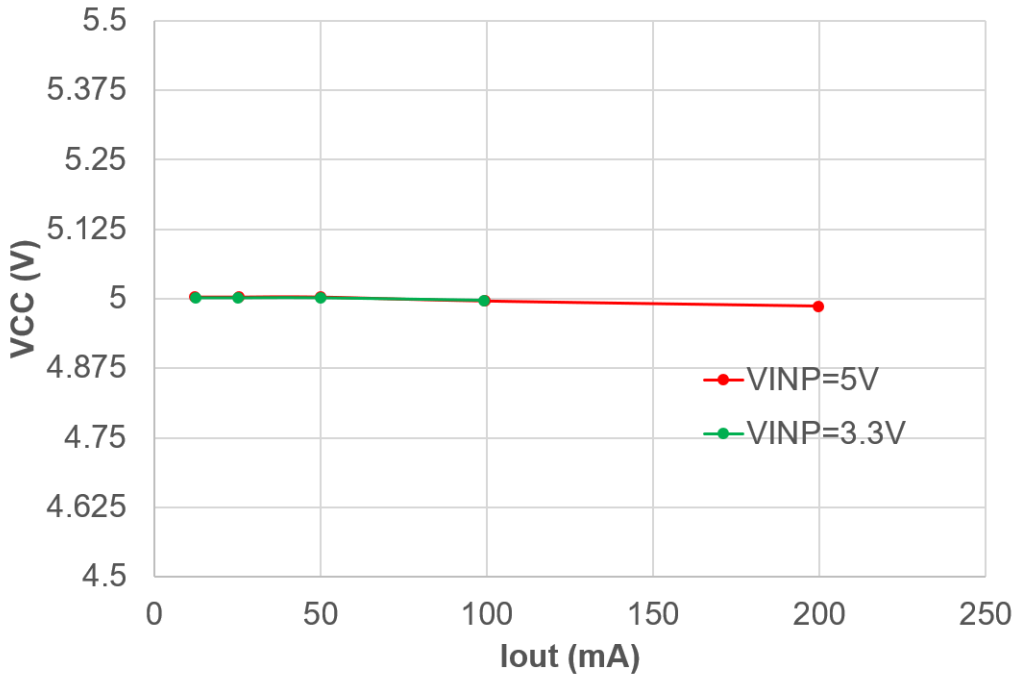

Figure 3-5. UCC33020-Q1 Regulation vs Load Current VCC=5.0V

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3.2.3 Startup Waveforms

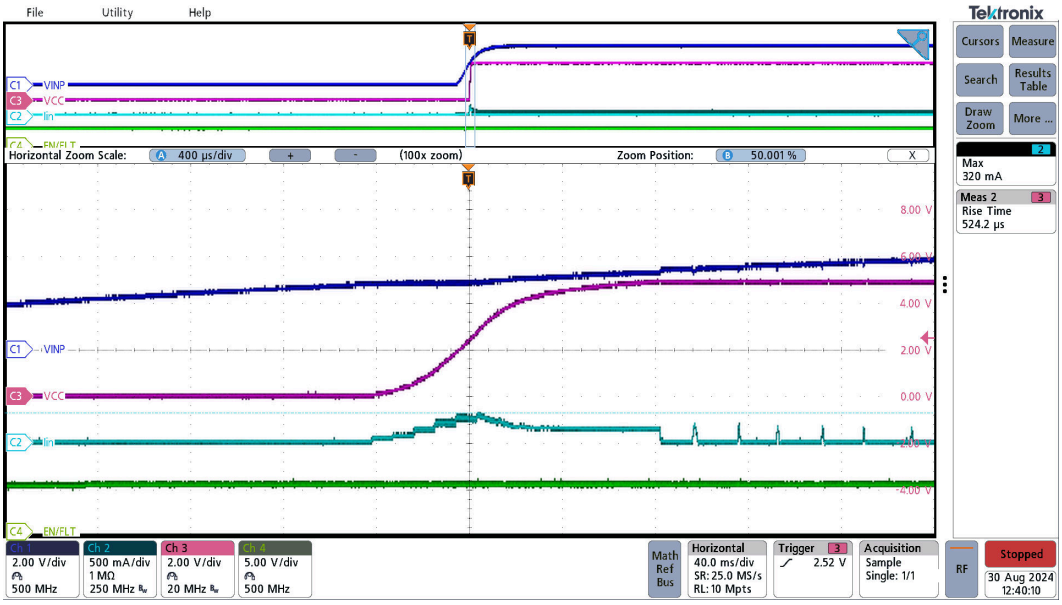

Figure 3-6. UCC33420-Q1 Start-up, sequence EN=5.0V → VINP=5.0V, VCC=5.0V, Iout=0mA

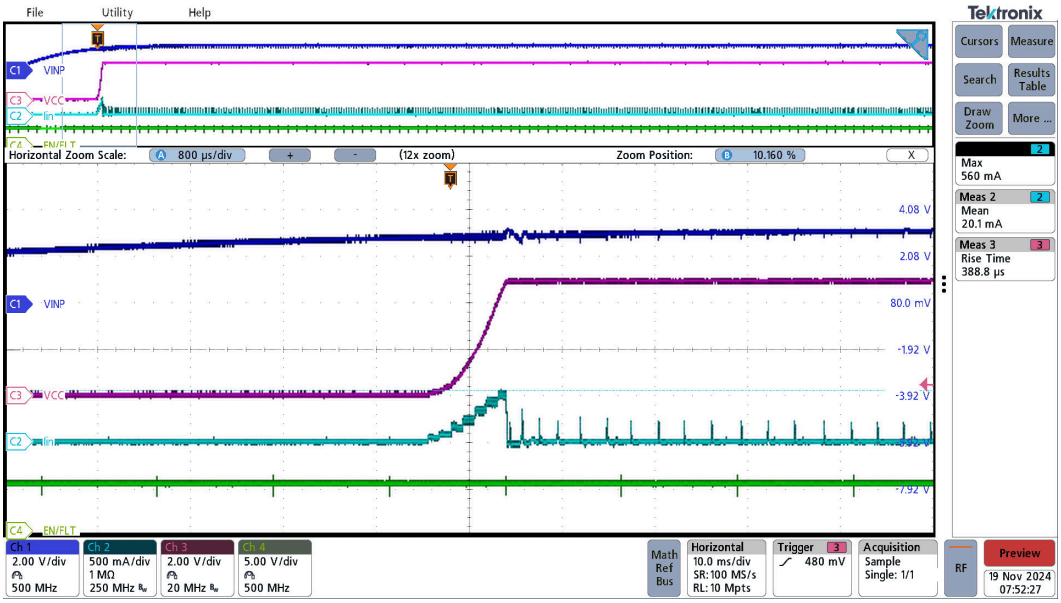

Figure 3-7. UCC33020-Q1 Start-up, sequence EN=5.0V → VINP=3.3V, VCC=5.0V, Iout=0mA

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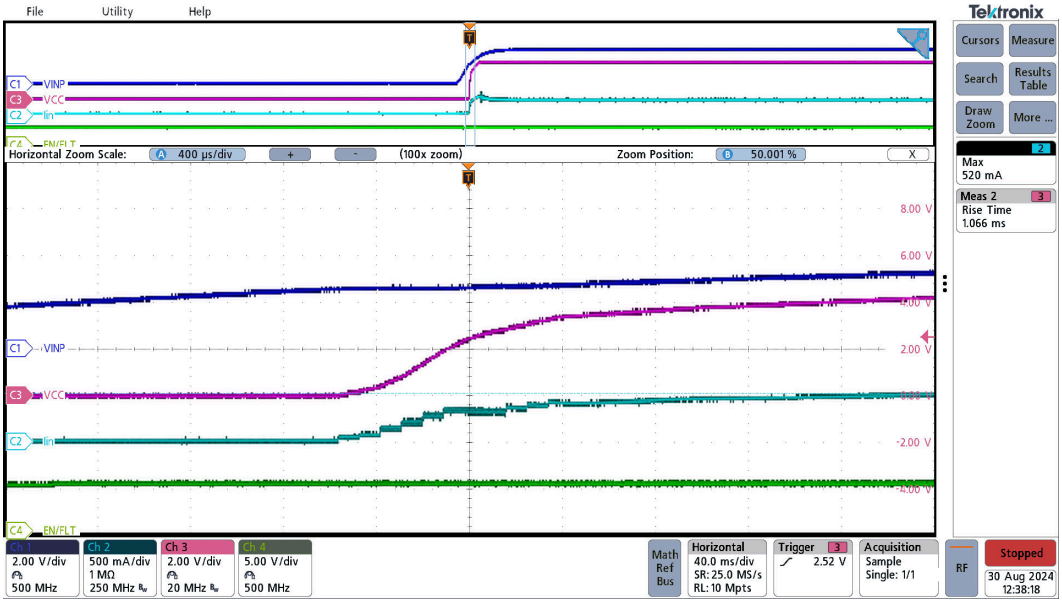

Figure 3-8. UCC33420-Q1 Start-up, sequence EN=5.0V → VINP=5.0V, VCC=5.0V, Rload=18Ω

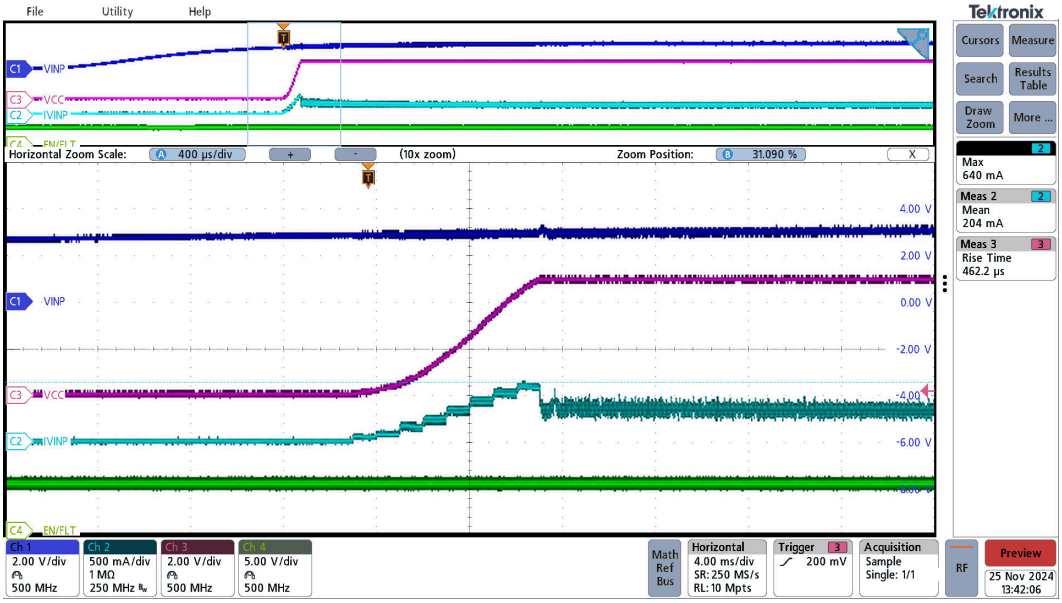

Figure 3-9. UCC33020-Q1 Start-up, sequence EN=5.0V → VINP=3.3V, VCC=5.0V, Rload=50Ω

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3.2.4 Inrush Current

Inrush current measurements made with VINP applied first, then toggling EN pin second. The input capacitors are pre-biased to VINP and make negligible contribution to the measured inrush current.

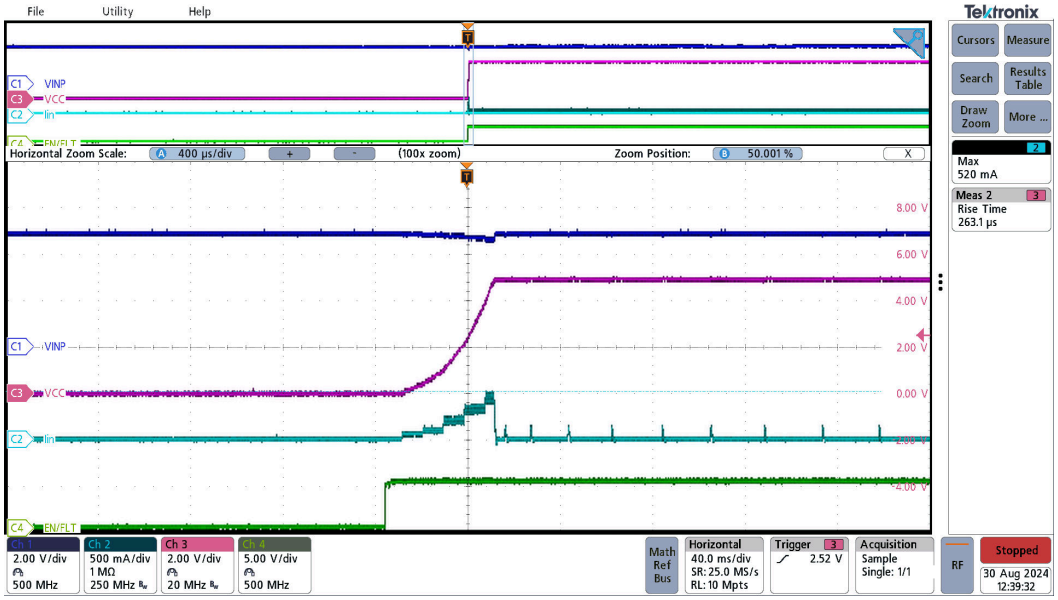

Figure 3-10. UCC33420-Q1 Inrush current , sequence VINP=5.0V → EN=5.0V, VCC=5.0V, Iout=0mA

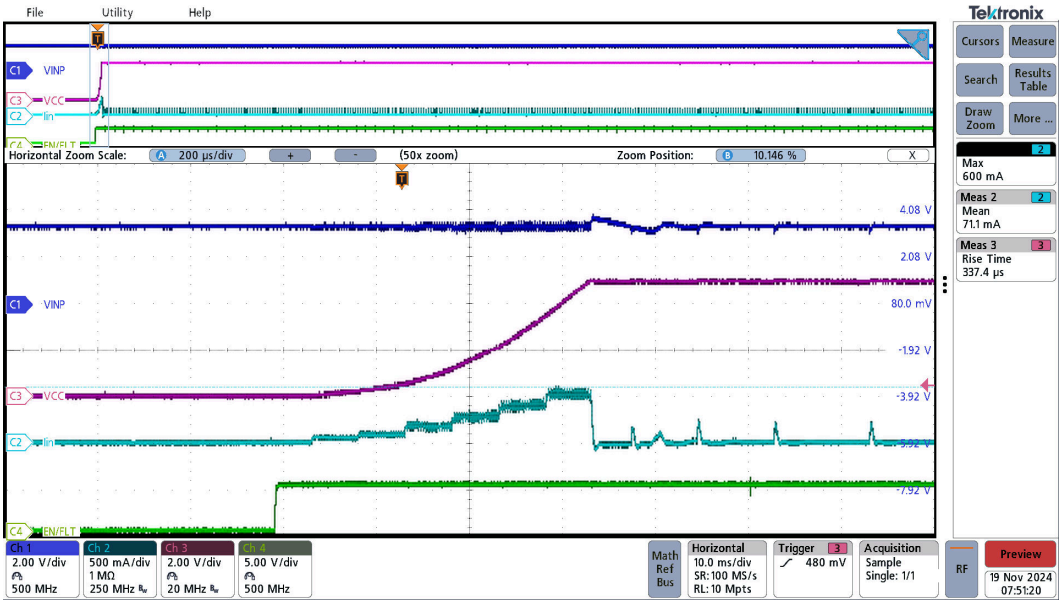

Figure 3-11. UCC33020-Q1 Inrush current , sequence VINP=3.3V → EN=5.0V, VCC=5.0V, Iout=0mA

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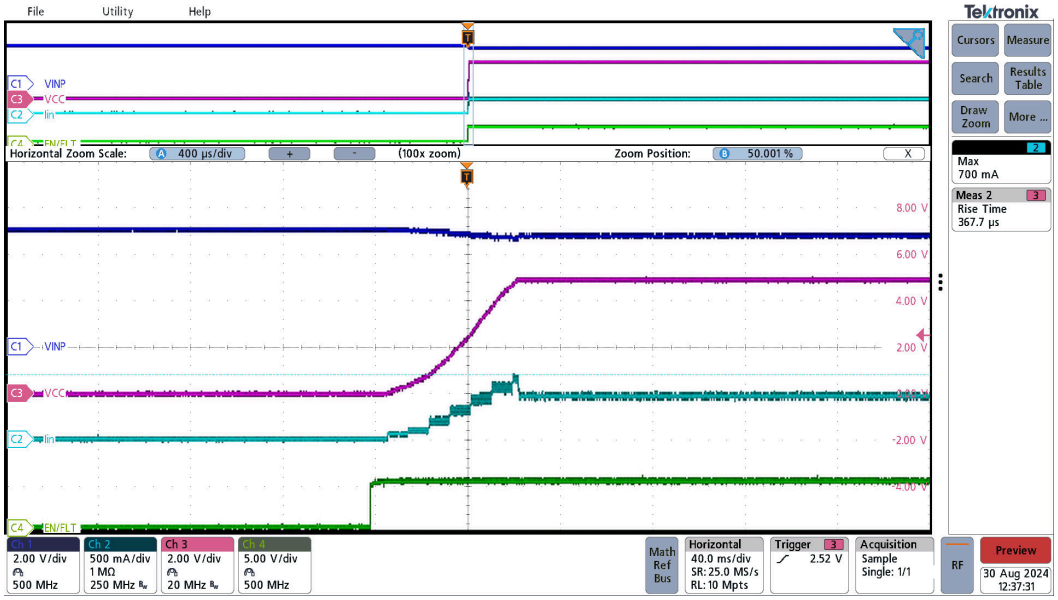

Figure 3-12. UCC33420-Q1 Inrush current, sequence VINP=5.0V → EN=5.0V, VCC=5.0V, Rload=18Ω

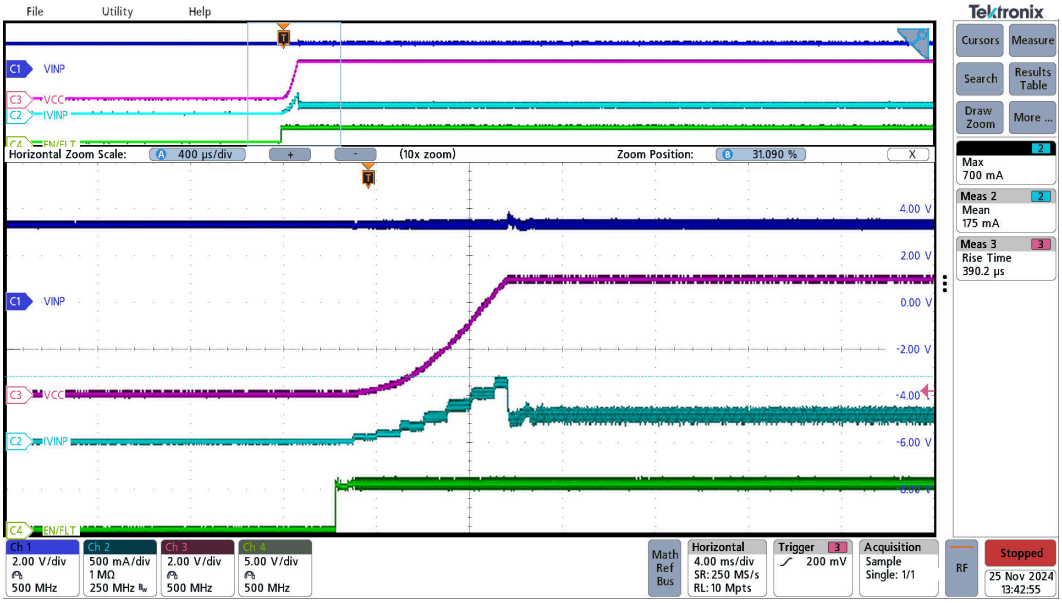

Figure 3-13. UCC33020-Q1 Inrush current, sequence VINP=3.3V → EN=5.0V, VCC=5.0V, Rload=50Ω

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3.2.5 AC Ripple Voltage

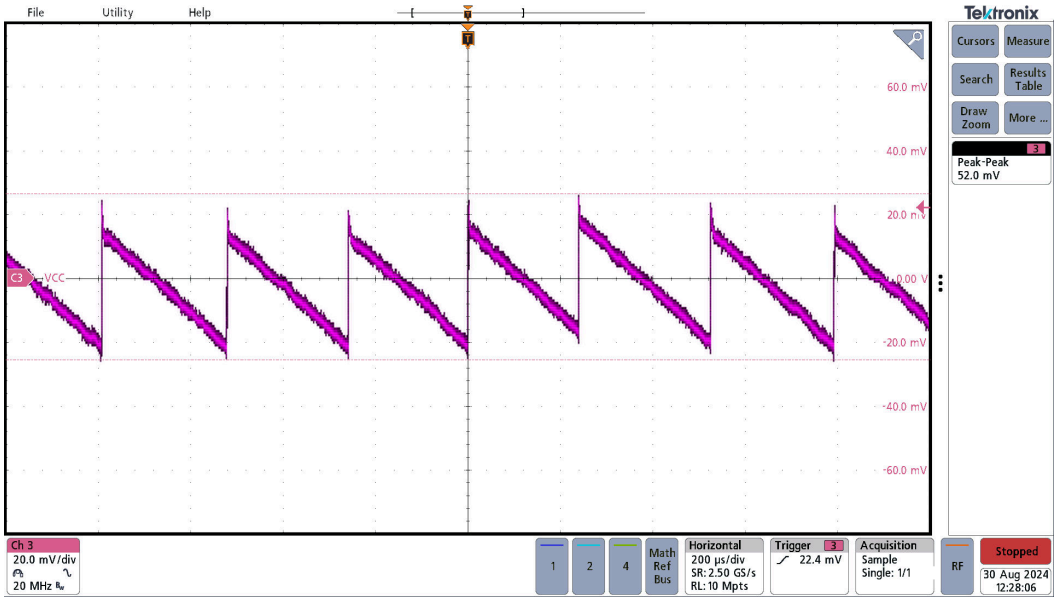

Figure 3-14. UCC33420-Q1 VCC AC Ripple, VINP=5.0V, VCC=5.0V, Iout=0mA

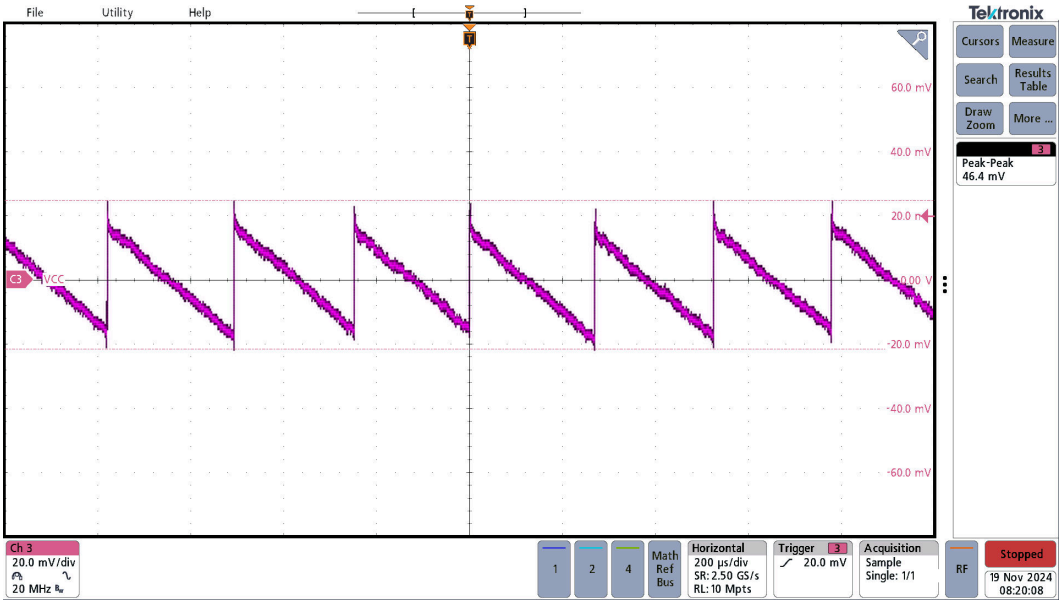

Figure 3-15. UCC33020-Q1 VCC AC Ripple, VINP=3.3V, VCC=5.0V, Iout=0mA

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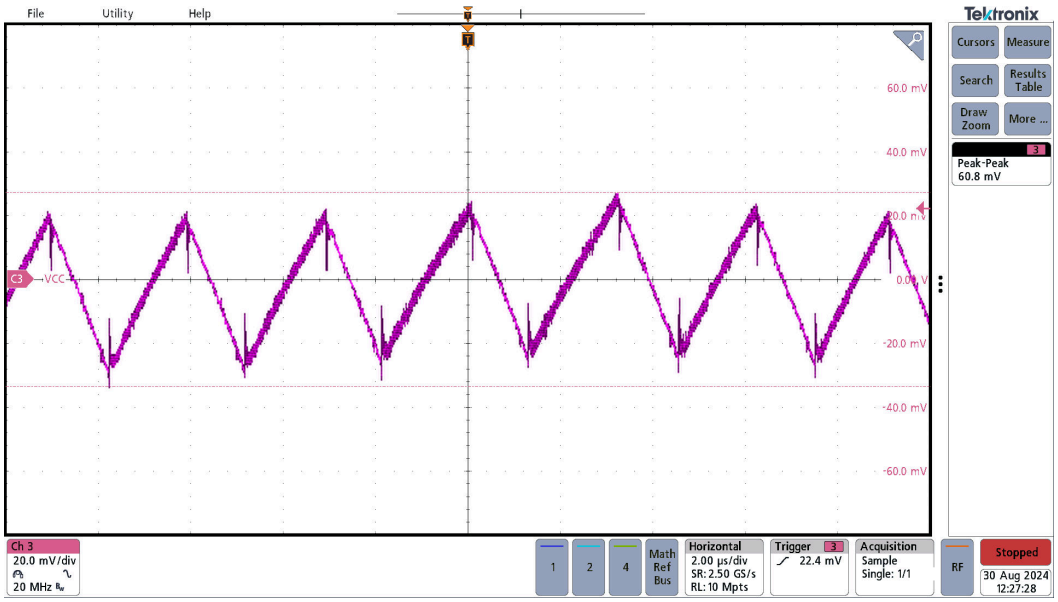

Figure 3-16. UCC33420-Q1 VCC AC Ripple, VINP=5.0V, VCC=5.0V, Iout=300mA

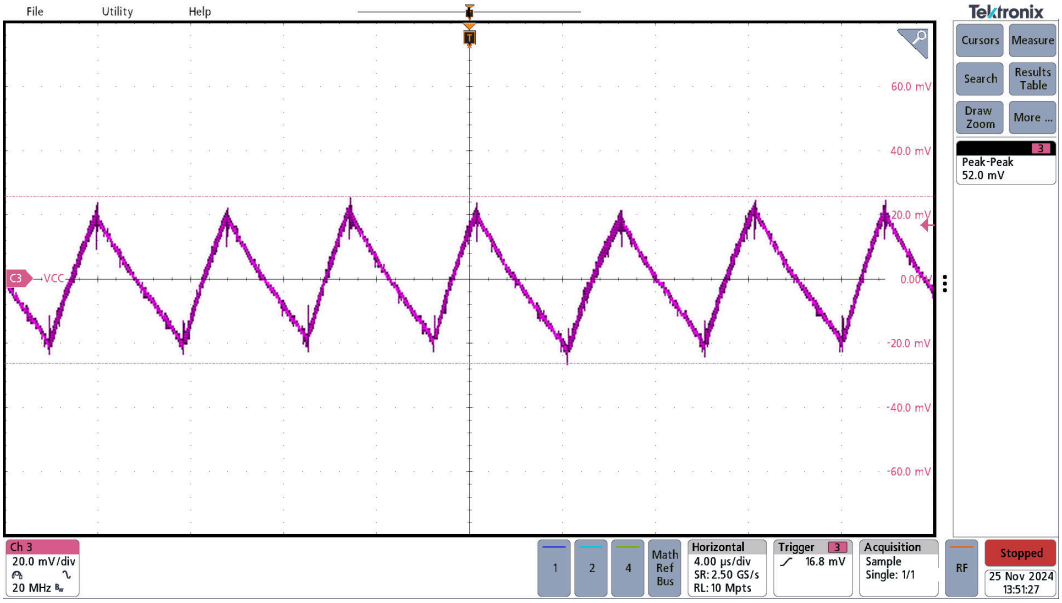

Figure 3-17. UCC33020-Q1 VCC AC Ripple, VINP=3.3V, VCC=5.0V, Iout=100mA

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3.2.6 Load Transient

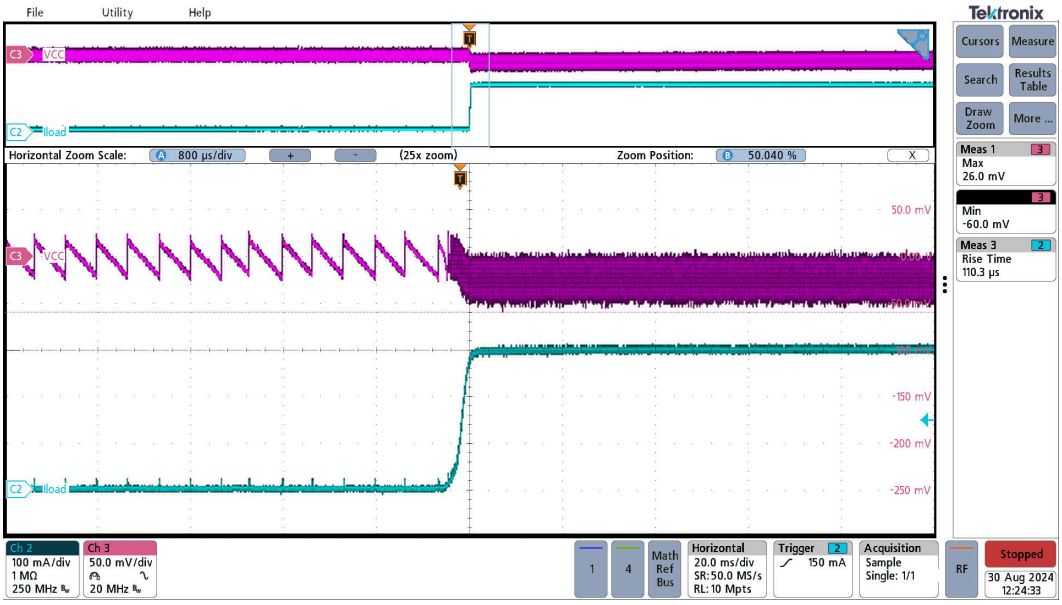

Figure 3-18. UCC33420-Q1 Load transient, VINP=5.0V, VCC=5.0V, No load (Iout=0mA) to Full load (Iout=300mA)

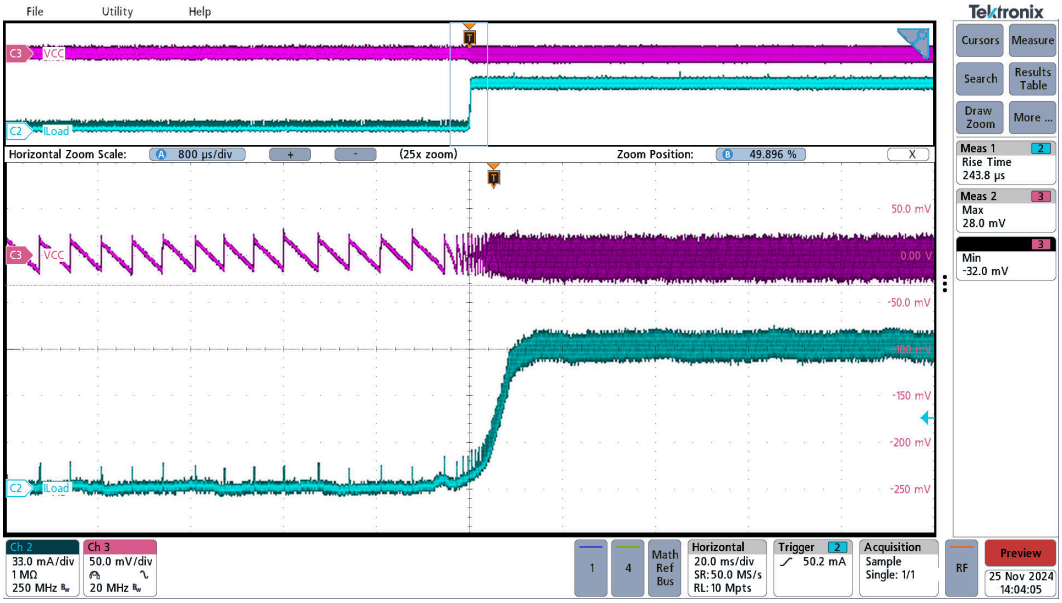

Figure 3-19. UCC33020-Q1 Load transient, VINP=3.3V, VCC=5.0V, No load (Iout=0mA) to Full load (Iout=100mA)

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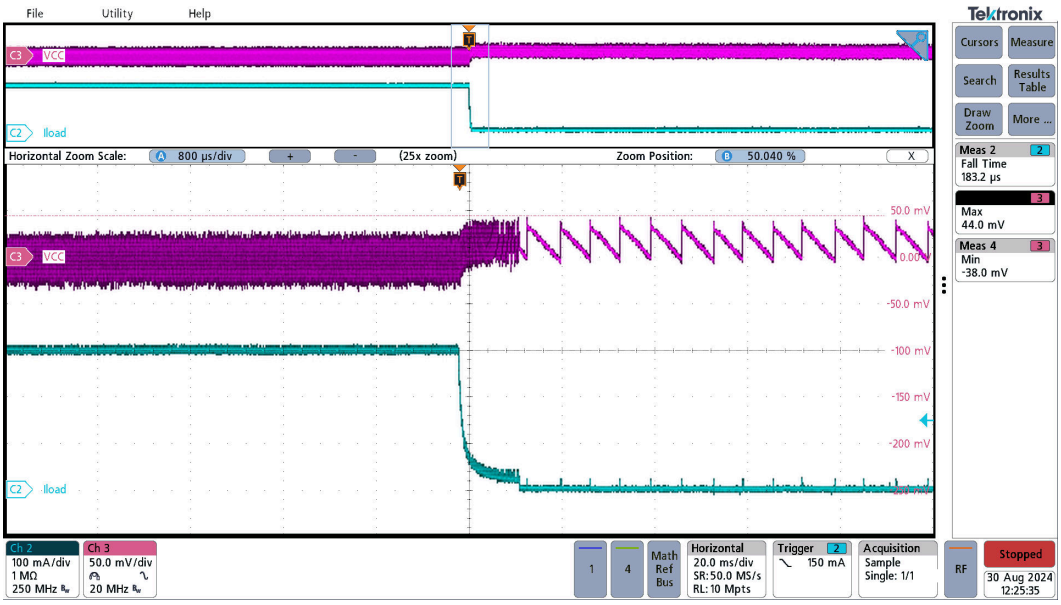

Figure 3-20. UCC33420-Q1 Load transient, VINP=5.0V, VCC=5.0V, Full load (Iout=300mA) to No load (Iout=0mA)

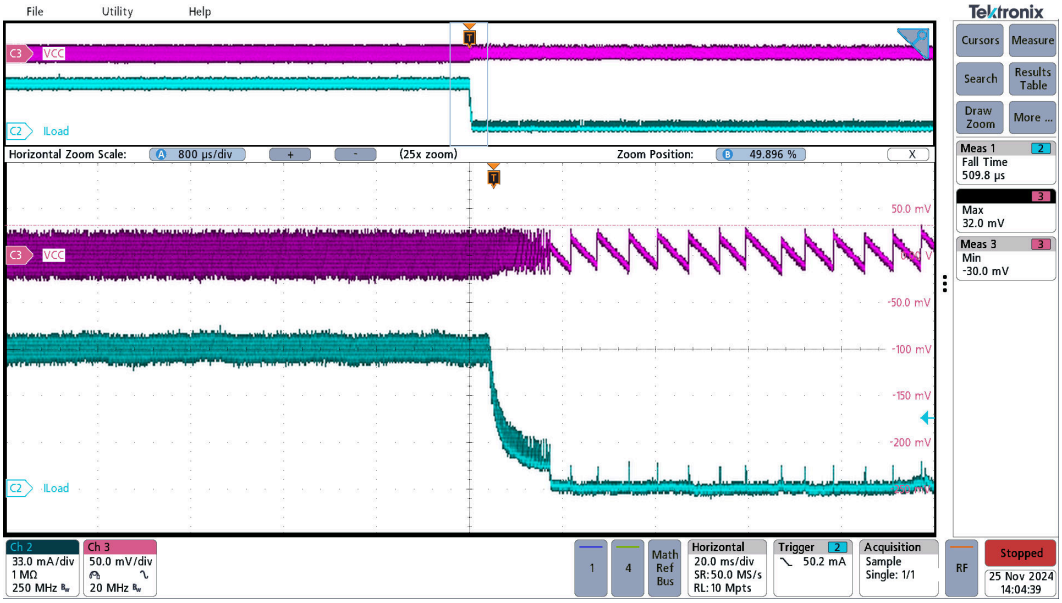

Figure 3-21. UCC33020-Q1 Load transient, VINP=3.3V, VCC=5.0V, Full load (Iout=100mA) to No load (Iout=0mA)

3.2.7 VCC Short-Circuit

Short circuit is applied with an electronic load. FLT pin is pulled down during 200µs and the device tries to restart after 160ms as shown in the waveform below. Device restarts successfully after short circuit is released.

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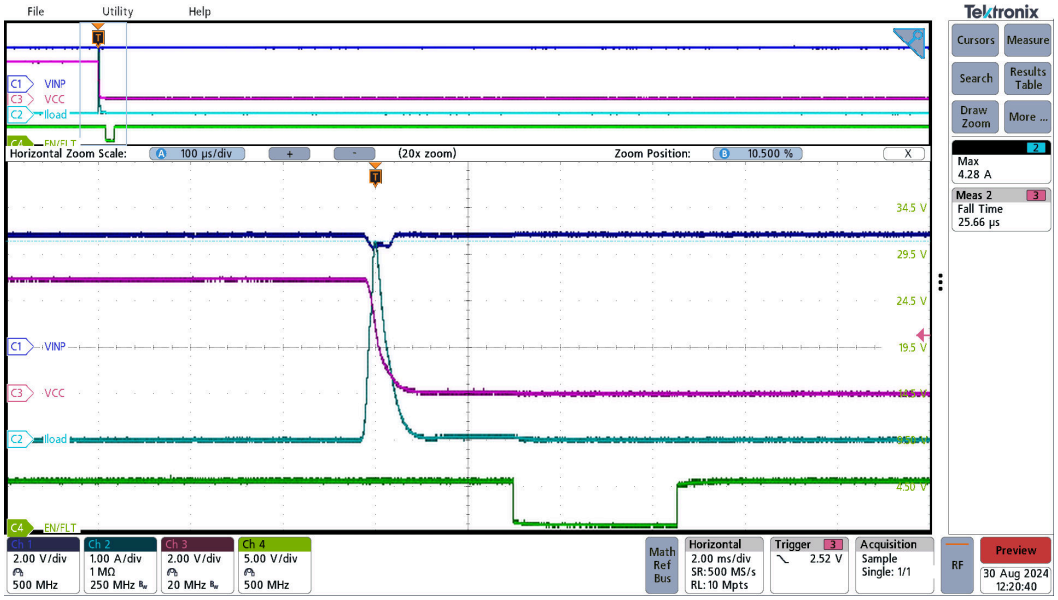

Figure 3-22. UCC33420-Q1 Short circuit, VINP=5.0V, VCC=5.0V

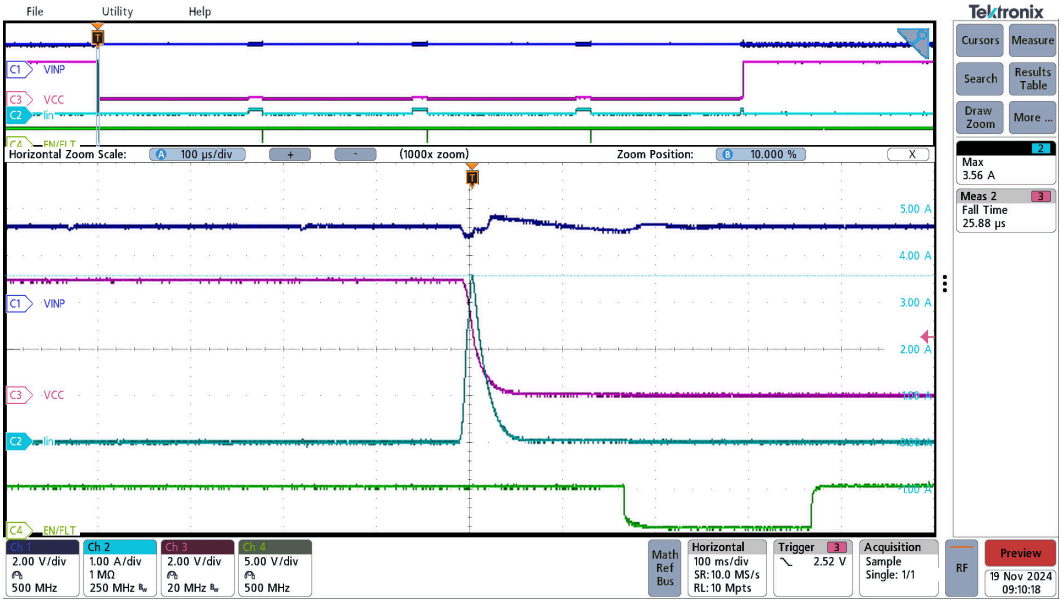

Figure 3-23. UCC33020-Q1 Short circuit, VINP=3.3V, VCC=5.0V

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3.2.8 Thermal Performance

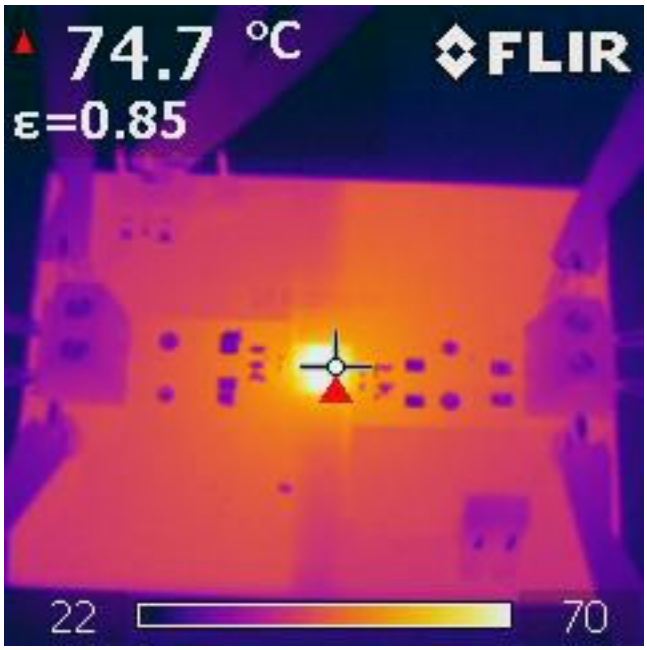

Figure 3-24. UCC33420-Q1 VINP=5.0V, VCC=5.0V, Iout=300mA, Pout=1.5W, TA=25°C

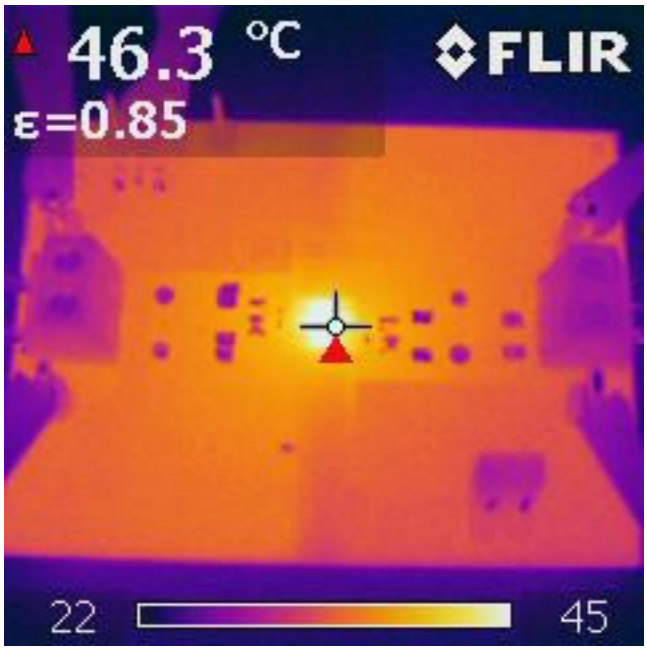

Figure 3-25. UCC33020-Q1 VINP=3.3V, VCC=5.0V, Iout=100mA, Pout=0.5W, TA=25°C

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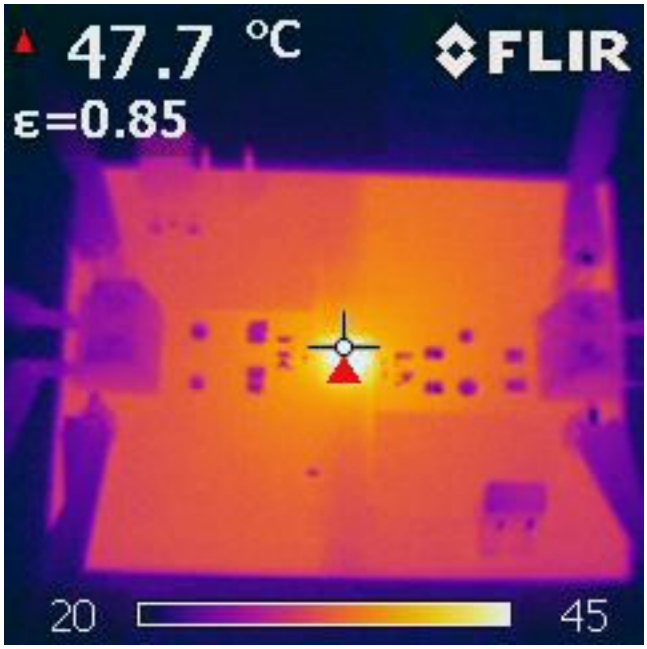

Figure 3-26. UCC33420-Q1 VINP=5.0V, VCC=5.0V, Iout=150mA, Pout=0.75W, TA=25°C

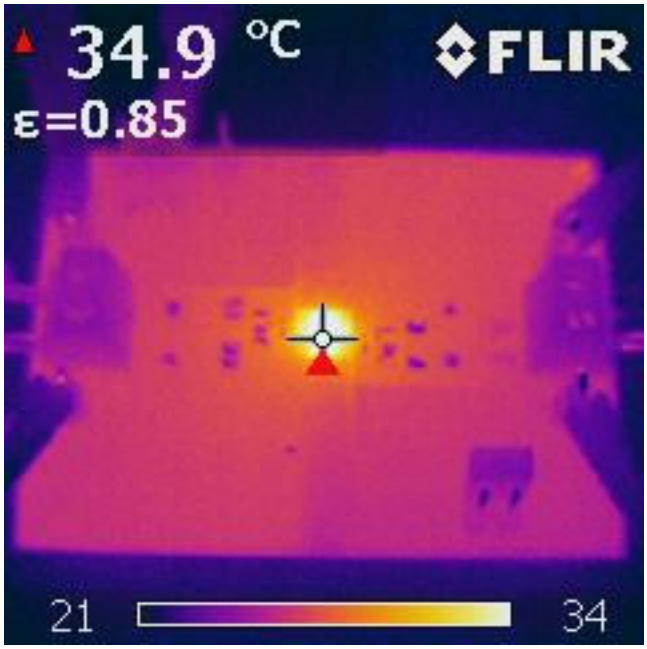

Figure 3-27. UCC33020-Q1 VINP=3.3V, VCC=5.0V, Iout=50mA, Pout=0.25W, TA=25°C

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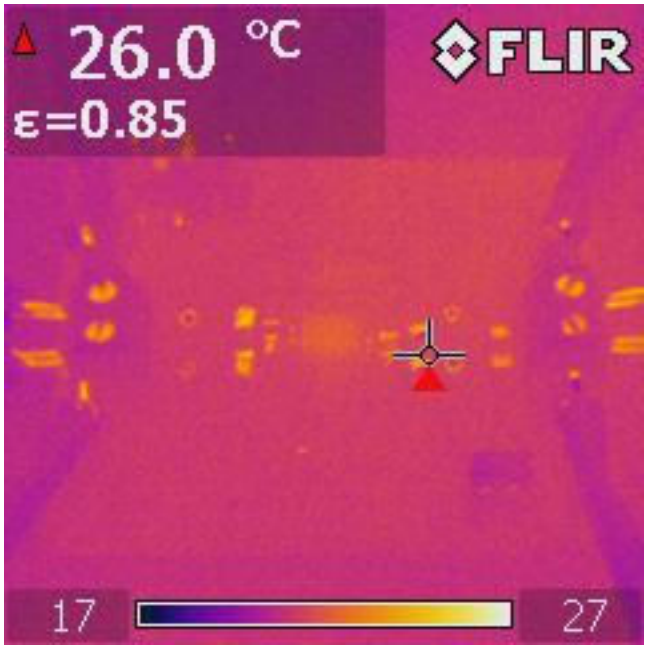

Figure 3-28. UCC33420-Q1 VINP=5.0V, VCC=5.0V, Iout=0mA, Pout=0W, TA=25°C

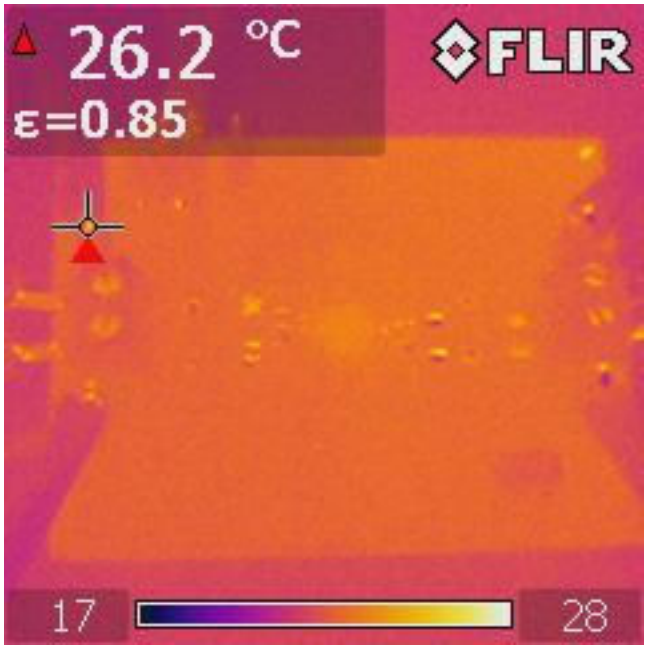

Figure 3-29. UCC33020-Q1 VINP=3.3V, VCC=5.0V, Iout=0mA, Pout=0W, TA=25°C

Note

The calibration of the thermal camera set the emissivity used on the thermal performance pictures.

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4 Hardware Design Files

4.1 Assembly and Printed Circuit Board (PCB)

The UCC33420EVM-080 is designed using a four-layer, FR4, PCB, fabricated with 1-ounce copper on all four layers. The EVM PCB demonstrates the important use of ground planes and tented stitching vias for shielding and providing low impedance connection between GND layers. For higher density PCBs such as automotive traction inverters, the PCB can include several additional signal layers but similar design methodology should be applied as best as possible.

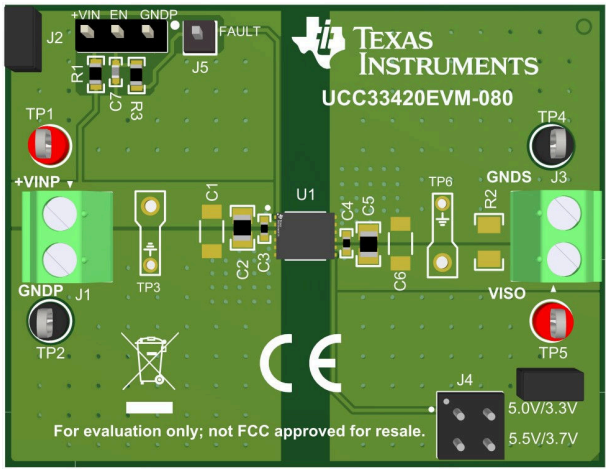

Figure 4-1. Fully Assembled 3D (Top View)

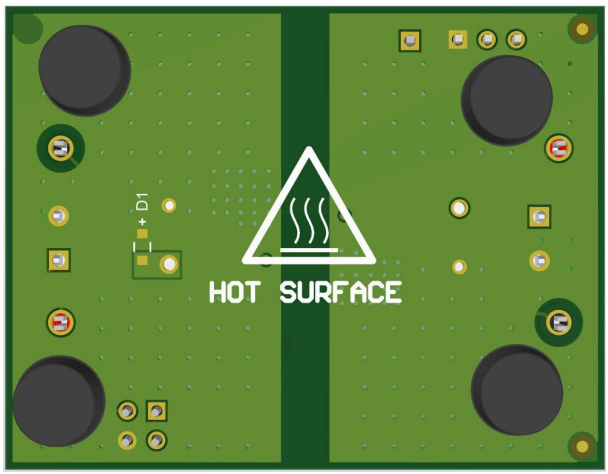

Figure 4-2. Fully Assembled 3D (Bottom View)

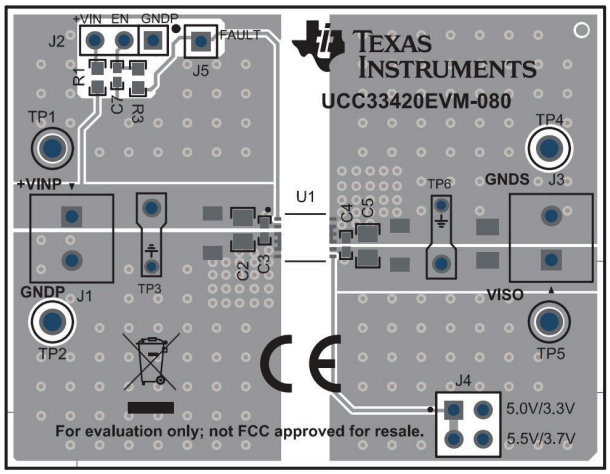

Figure 4-3. PCB Top Layer, Assembly

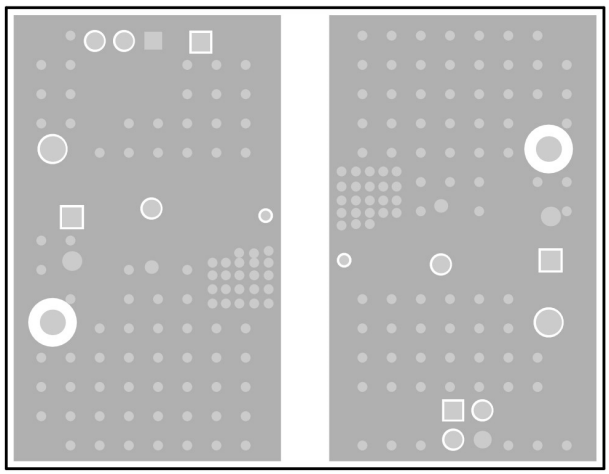

Figure 4-4. Ground Layer 2

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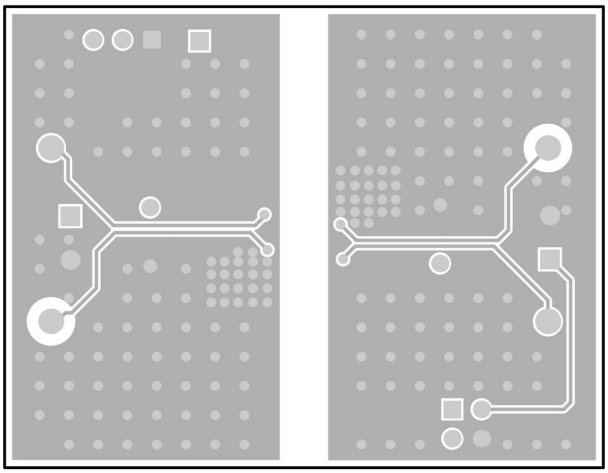

Figure 4-5. Ground Layer 3

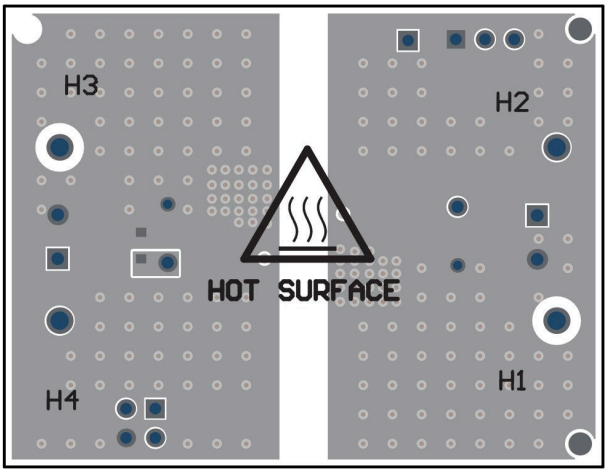

Figure 4-6. PCB Bottom Layer, Assembly (Mirrored View)

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4.2 Bill of Materials (BOM)

Table 4-1. Bill of Materials

Designator	Qty	Description	Part Number	Manufacturer
PCB1	1	Printed Circuit Board	HVP080E1	Any
C2	1	CAP, CERM, 10µF, 10V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	GCJ21BR71A106K E01L	MuRata
C3, C4	2	0.015uF ±10% 50V, Ceramic Capacitor X7R, 0402 (1005 Metric)	GCM155R71H153KA55D	MuRata
C5	1	CAP, CERM, 22µF, 10V, +/- 20%, X7R, 0805	GRM21BZ71A226ME15L	MuRata
C7	1	CAP, CERM, 2200pF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71H222KA37D	MuRata
H1, H2, H3, H4	4	Bumpers	SJ61A6	3M
J1, J3	2	Conn Term Block, 2POS, 3.81mm, TH	1727010	Phoenix Contact
J2	1	Header, 100mil, 3x1, Tin, TH	PEC03SAAN	Sullins Connector
J4	1	Header, 100mil, 2x2, Tin, TH	PEC02DAAN	Sullins Connector
J5	1	Header, 1x1, Tin, TH	PEC01SAAN	Sullins Connector
R1	1	RES, 0Ω, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R3	1	RES, 18.2kΩ, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060318K2FKEA	Vishay-Dale
SH-J1, SH-J2	2	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector
TP1, TP5	2	Test Point, Multipurpose, Red, TH	5010	Keystone
TP2, TP4	2	Test Point, Multipurpose, Black, TH	5011	Keystone
U1	1	1.5W, High-Density, >3 kVRMS Isolated DC-DC Converter	PUCC33420-Q1	Texas Instruments
U1-alt	0	1.5W, High-Density, >3 kVRMS Isolated DC-DC Converter	PUCC33420RAQR	Texas Instruments
U1-alt	0	1.5W, High-Density, >3 kVRMS Isolated DC-DC Converter	PUCC33410QRAQRQ1	Texas Instruments
U1-alt	0	1.5W, High-Density, >3 kVRMS Isolated DC-DC Converter	PUCC33410RAQR	Texas Instruments
C1, C6	0	CAP, CERM, 10µF, 10V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	GCM31CR71A106KA64L	MuRata
R2	0	RES, 200Ω, 5%, 0.25W, AEC-Q200 Grade 0, 1206	CRCW1206200RJNEA	Vishay-Dale
D1	0	Zener Diode 5.94V 960mW ±2.61%	PLZ6V2A-G3/H	Vishay

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5 Additional Information

5.1 Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2024) to Revision C (December 2024)	Page
• Added UCC33020-Q1 and UCC33020 devices to UCC33x20-Q1 devices table	2
• Updated UCC33420-Q1 EVM Electrical Characteristics	3
• Added UCC33020-Q1 EVM Electrical Characteristics	3
• Updated Schematic	8
• Updated UCC33420-Q1 Performance Data	8
• Added UCC33020-Q1 Performance Data	8
• Updated Bill of Materials table	25

Changes from Revision A (May 2024) to Revision B (May 2024)	Page
• Updated *Applications* section	1
• Updated capacitors recommendations on Description section of *UCC33420-Q1 Pin Description* table	2
• Updated schematics	8

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