

Power Supply Reference Design for Samsung™ s3c2416 Using TPS650240 or TPS650250

This reference design details the power supply requirements of the Samsung™ s3c2416 processor and how to design with the TPS650240 or TPS650250.

1 Features

- TPS650240/TPS650250 integrated power management unit
- 2.5-V to 6-V input voltage range
- Output current up to 1000mA(TPS650240),/1600mA(TPS650250)
- Up to 97% efficiency
- Small 5-mm × 5-mm, 32-pin QFN package

2 Introduction

This reference design applies to the Samsung™ s3c2416 processor family. It provides all required analog and logic supply rails to power up a s3c2416 processor.

3 Requirements

Table 1. Samsung™ s3c2416 Processor Power Requirements

Core/IO	Pin Name	Voltage	I _{max} [mA]	Tolerance	Power-On Sequence
	VDDalive	1.2	30	±5%	2
	VDD_SRAMi VDD_SDRAMi	1.8	600	±5%	1
	VDDi VDDA_MPLL VDDA_EPLL VDDiarm Vgate	1.3	600	±5%	3
	VDD_OP VDD_LCD VDD_SD VDDA_ADC	3.3	950	±5%	1
	VDDI_UDEV	1.2	70	±5%	3
	VDDA33x VDD_USBOSC	3.3	150	±5%	3
	VDD_RTC	3.3	5	±5%	1

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Table 2. Samsung™ s3c2416 Voltage Requirements at 400 MHz

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage for Alive Block	VDDalive	1.15	1.2	1.25	V
DC Supply Voltage for Core Block	ARMCLK/HCLK				V
	400/133 MHz	VDDiarm, VDDi, VDDA_MPLL, VDDA_EPLL	1.25	1.3	
DC Supply Voltage for I/O Block1	VDD_OP1 ⁽¹⁾	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for I/O Block2	VDD_OP2	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for I/O Block3	VDD_OP3	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for USBOSC PAD	VDD_USBOSC	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for SRAM I/F	VDD_SRAM	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for SDRAM I/F	VDD_SDRAM	1.7	1.8 / 2.5	2.7	V
DC Supply Voltage for RTC	VDD_RTC	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for SD/LCD	VDD_SD	1.7	1.8 / 2.5 / 3.3	3.6	V
	VDD_LCD	1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for USB PHY 3.3 V	VDDA33x	3.3-5%	3.3	3.3+5%	V
DC Supply Voltage for USB PHY 1.2 V	VDDI_UDEV	1.2-5%	1.2	1.2+5%	V
DC Supply Voltage for ADC	VDDA_ADC	3	3.3	3.6	V
DC Input Voltage	V _{IN}	3	3.3	3.6	V
		2.3	2.5	2.7	
		1.7	1.8	1.95	
DC Output Voltage	V _{OUT}	3	3.3	3.6	V
		2.3	2.5	2.7	
		1.7	1.8	1.95	
Operating Temperature	T _A	Industrial		85	°C
		Extended		70	

⁽¹⁾ If USB function is not used, VDD_OP1 has a range of 2.3 V to 3.6 V.

Table 3. Samsung™ s3c2416 Voltage Requirements at 266 MHz

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage for Alive Block	VDDalive	1.15	1.2	1.25	V
DC Supply Voltage for Core Block	ARMCLK / HCLK				V
	266/133 MHz	VDDiarm	1.25	1.3	
		VDDi, VDDA_MPLL, VDDA_EPLL	1.25	1.3	1.35
DC Supply Voltage for I/O Block1	VDD_OP1 ⁽¹⁾	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for I/O Block2	VDD_OP2	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for I/O Block3	VDD_OP3	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for USB OSC PAD	VDD_USBOSC	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for SRAM I/F	VDD_SRAM	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for SDRAM I/F	VDD_SDRAM	1.7	1.8 / 2.5	2.7	V
DC Supply Voltage for RTC	VDD_RTC	1.7	1.8 / 2.5 / 3.3	3.6	V
DC Supply Voltage for SD/LCD	VDD_SD	1.7	1.8 / 2.5 / 3.3	3.6	V
	VDD_LCD	1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for USB PHY 3.3 V	VDDA33x	3.3-5%	3.3	3.3+5%	V
DC Supply Voltage for USB PHY 1.2 V	VDDI_UDEV	1.2-5%	1.2	1.2+5%	V
DC Supply Voltage for ADC	VDDA_ADC	3	3.3	3.6	V

⁽¹⁾ If the USB function is not used, VDD_OP1 has a range of 2.3 V to 3.6 V.

Table 3. Samsung™ s3c2416 Voltage Requirements at 266 MHz (continued)

Parameter	Symbol		Min	Typ	Max	Unit
DC Input Voltage	V_{IN}		3	3.3	3.6	V
			2.3	2.5	2.7	
			1.7	1.8	1.95	
DC Output Voltage	V_{OUT}		3	3.3	3.6	V
			2.3	2.5	2.7	
			1.7	1.8	1.95	
Operating Temperature	T_A	Industrial	-40		85	°C
		Extended	-20		70	

4 Powering Samsung™ s3c2416 Using TPS650240 or TPS650250

The TPS650240/TPS650250 is an integrated power management integrated circuit (PMIC) for applications requiring multiple power rails supplied by one Li-Ion or Li-Polymer battery.

The TPS650240/TPS650250 provides three efficient, step-down converters targeted at providing the core voltage, peripheral, I/O, and memory rails in a processor-based system. All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents.

The application block diagram of the TPS650240 and s3c2416 is shown in [Figure 1](#).

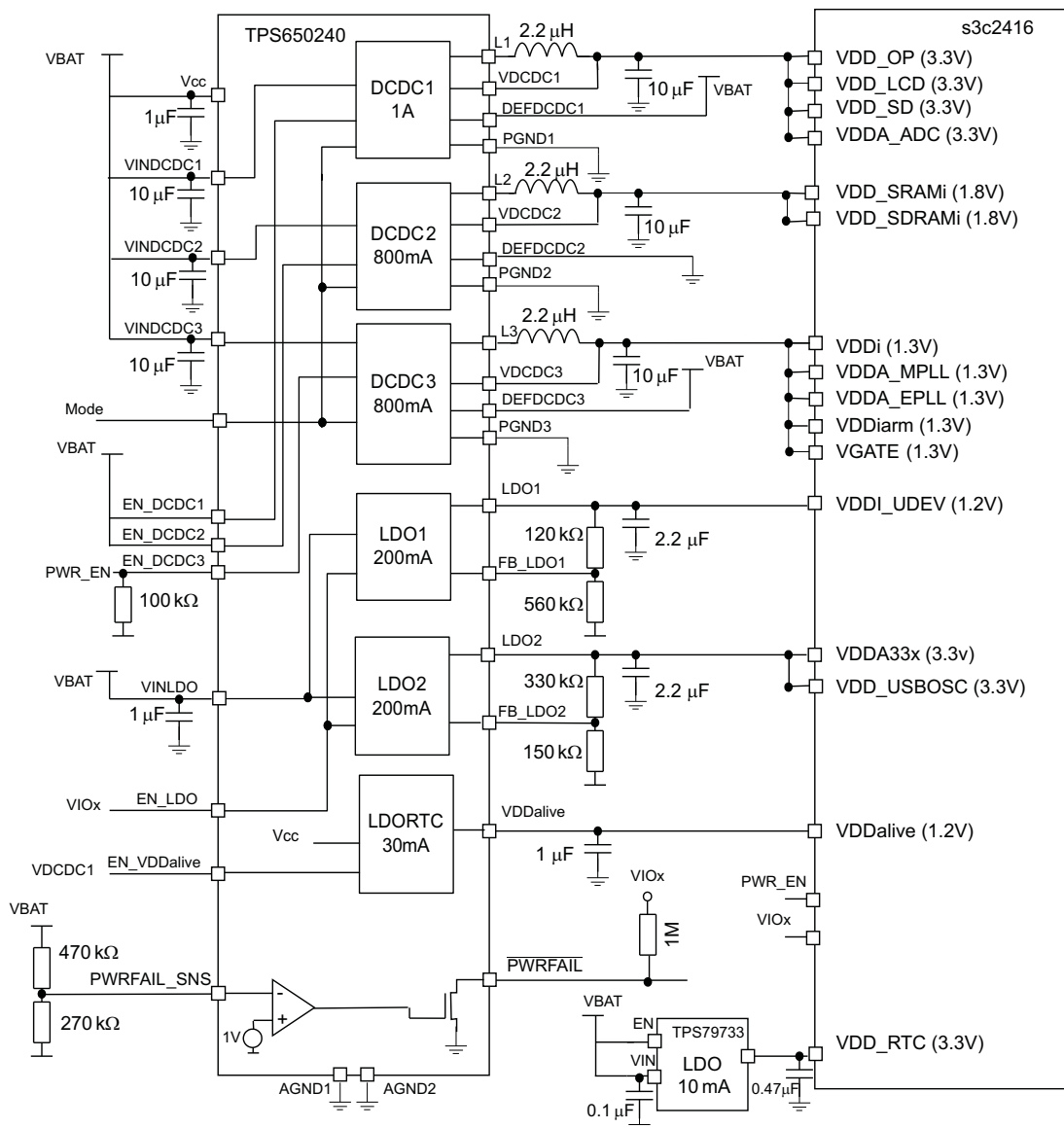


Figure 1. TPS650240 Functional Block Diagram

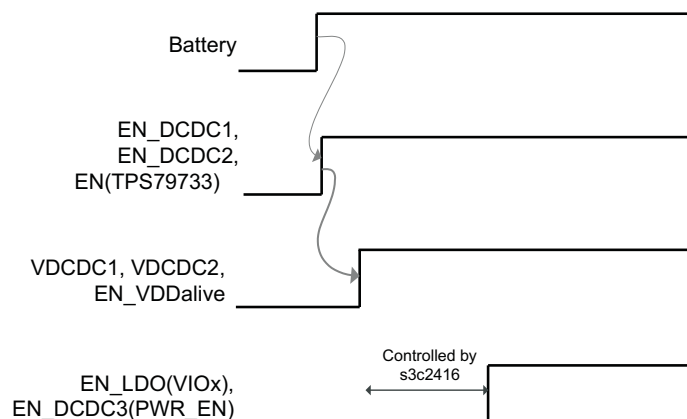


Figure 2. TPS650240 Sequencing Implementation

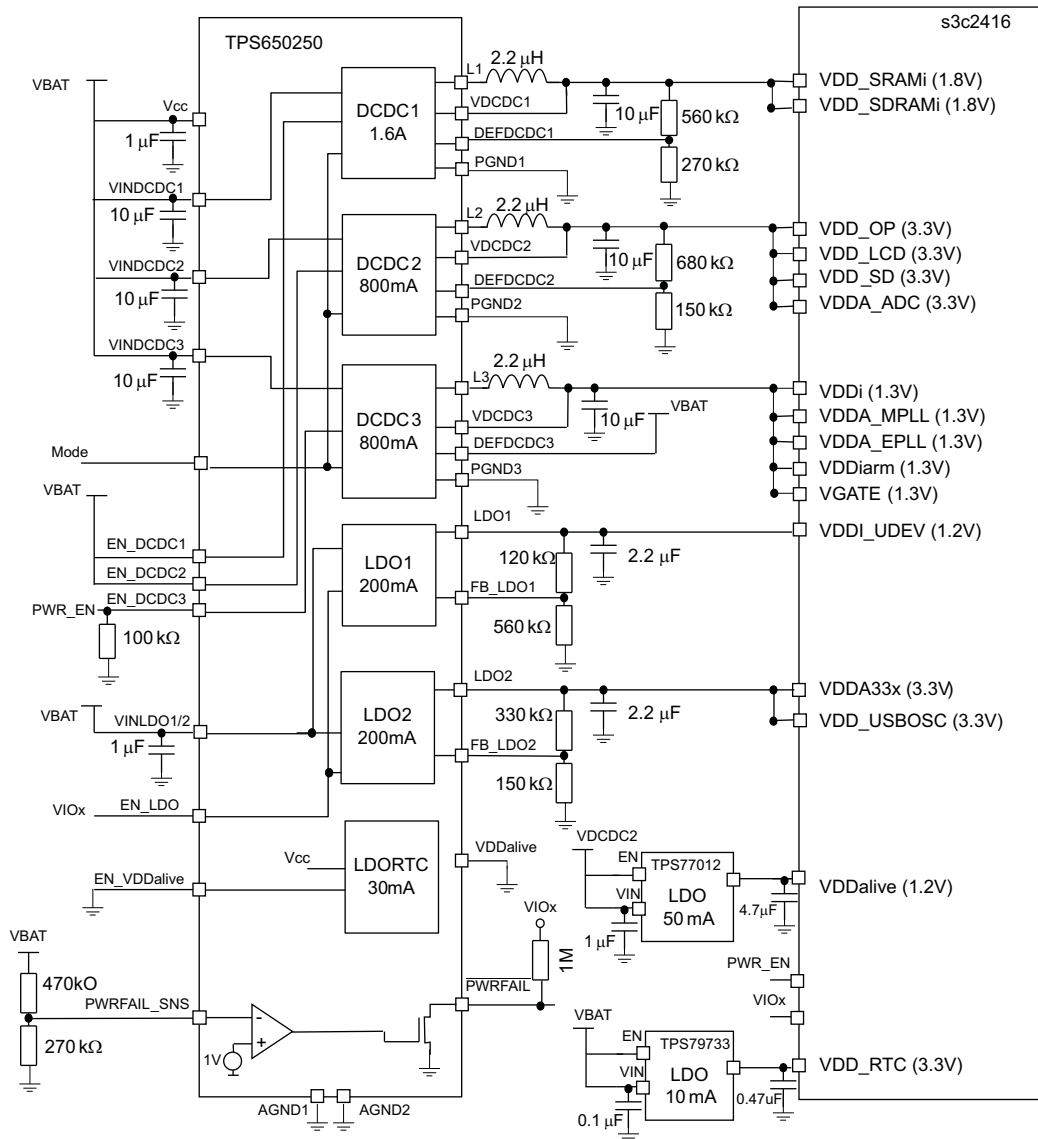


Figure 3. TPS650250 Functional Block Diagram

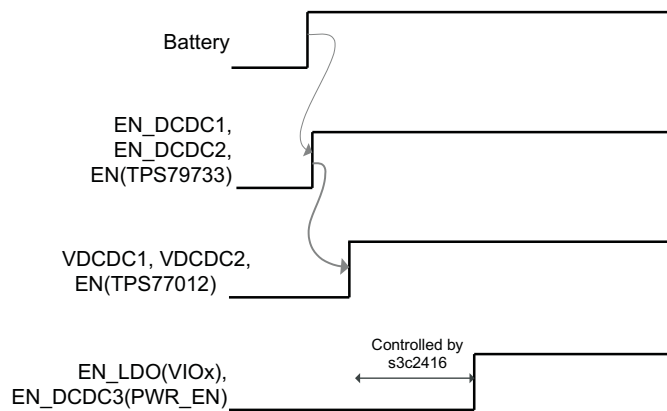


Figure 4. TPS650250 Sequencing Implementation

Figure 2 illustrates an implementation of the sequence. The valid battery voltage presence enables DCDC1, DCDC2 and the external LDO which supplies VDD_RTC. VDDalive rail will be enabled by DCDC1's output. PWR_EN and VIOx from s3c2416 control the LDO1/2 and DCDC3 output.

If a specific power sequence is needed, each individual EN_DCDC and EN_LDO pin can be externally controlled according to the defined sequence. For further details, contact the microprocessor manufacturer (in this application Samsung™ Semiconductor). TPS650250 (see Figure 3) can be used for the same application, the main difference is that TPS650250 provides extra external adjustable flexibility on DCDC3 and higher current capability of DCDC1.

5 References

1. s3c2416 data sheet from Samsung Semiconductor, REV1, 8/2008
2. TPS650240, Power Management ICs for Li-Ion Powered Systems data sheet ([SLVS774](#))
3. TPS650250, Power Management ICs for Li-Ion Powered Systems data sheet ([SLVS843](#))

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