Application Report
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How to Design a Thermally-Efficient Integrated BLDC Motor Drive PCB

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ABSTRACT

This application report provides an in-depth discussion of thermal design for three-phase integrated BLDC motor drive PCBs in context of the DRV10987. Theoretical and experimental calculations for junction, ambient, and case temperature are discussed.

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Trademarks

1 Introduction

For BLDC motor drive applications, temperature is often a critical design specification that cannot be violated. Specifically, cooling applications such as pedestal fans, ceiling fans, HVAC automotive seat blowers, washer and dryer fans, server fans, and refrigerator fans should try to dissipate heat as efficiently as possible. This allows for the lowest possible ambient (T_A) and case (T_C) temperature, in addition to, the lowest possible silicon die or junction temperature (T_J) inside the device package. As previously mentioned, these temperatures are important because the ambient, case, and junction temperatures link to critical design specifications.

For the ambient and case temperature, the design specifications are often determined by the application. For example, dryer units deal with very hot ambient temperatures and a dryer fan motor drive circuit produces extra heat that contributes to the overall ambient temperature. As a result, a system used in a home-appliance dryer might design a dryer system that should not violate an ambient temperature of 65°C. In addition, some applications might have heat sensitive material (that is, waterproofing sealant) in close proximity to the motor drive circuits that are disrupted if the case temperature exceeds a certain temperature.

For junction temperature, many devices will not operate correctly if the minimum or maximum junction temperature specifications are violated. For example, the DRV10987 has a maximum junction temperature of 150°C in the absolute maximum ratings table of *DRV10987 12- to 24-V, Three-Phase, Sensorless BLDC Motor Driver* . While the DRV10987 has overtemperature protection that shuts down the device, this does not excuse good design practices which could prevent the overtemperature condition from occurring. In addition, motor drive applications are driven by design specifications such as output current. Since the current is directly correlated to the power dissipated, increasing the junction temperature, better thermal design allows for higher current with the same temperature.

1.1 Understanding the Thermal Model

Heat dissipation on a printed circuit board (PCB) can be broken down into a simple model that closely resembles the electrical circuit model. Specifically, the electrical circuit model is broken down to voltage (V), current (I), and resistance (R) through a simple relationship shown in Equation 1:

$$V = I \times R \tag{1}$$

The thermal model takes temperature (T), power dissipation (P), and thermal resistance (θ) and relates them to voltage, current, and resistance, respectively. This is shown in Equation 2.

$$T = P \times \theta \tag{2}$$

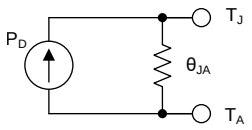

Figure 1. Thermal Model to Electrical Model Schematic

In Figure 1, the thermal model is represented in a schematic format to illustrate the typical conventions established by electrical circuit modeling. Since the ambient and junction temperature are represented as voltages, their difference is simply the sum of all dissipated power times the thermal resistance between the silicon die and the ambient air. This is represented in Equation 3.

$$T_J = P_D \times \theta_{JA} + T_A \tag{3}$$

2 Understanding Sources of Power Dissipation

Since there are multiple sources of power dissipation in a BLDC motor driver, their sum results in the total power dissipated in the circuit. This is used to calculate the junction temperature. While a short description is provided for each source of power dissipation, more information is found in *Calculating Motor Driver Power Dissipation* .

Equation 4 summarizes all sources of power dissipation.

$$P_D = P_{RDS} + P_{SW} + P_{IVM} + P_{LDO} \tag{4}$$

2.1 $R_{DS(on)}$

The largest source of dissipated power inside a three-phase BLDC motor driver is the current flowing through the power MOSFETs. When the FETs are turned on, the high- and low-side FETs act as resistors ($R_{DS(on)}$) that allow the current to flow from the supply to the terminal windings of the motor. The act of current flowing through the windings is what causes a magnetic field to develop and attract the permanent magnets on the rotor to cause motion. The power dissipated is represented by Equation 5.

$$P_{RDS} = 1.5 \times R_{DS(on)} \times \left(I_{OUT(RMS)}\right)^2 \quad (5)$$

Where:

- $R_{DS(on)}$ = sum of $R_{DS(on)}$ for both the high- and low-side FETs
- $I_{OUT(RMS)}$ = RMS output current being applied to the motor windings (not to be confused with the supply current)

Since $R_{DS(on)}$ increases as temperature increases, note that the lower the junction temperature and power dissipation from the FETs reduces the power dissipated.

In the case of the DRV10987, the typical $R_{DS(on)}$ at T_A = 25°C is 425 mΩ and the maximum continuous current is 2 $A_{(RMS)}$. Since the DRV10987 is a three-phase BLDC motor driver with 180° sinusoidal control, all of the power MOSFETs and phase terminal windings have current flowing through them during operation. The sum of the phase shifted sinusoidal current waveforms equate to a constant power dissipation.

2.2 Switching Loss

For a three-phase BLDC driver, switching loss refers to the power dissipated when a transistor switches from high to low and low to high. Since three-phase BLDCs are controlled with PWM signals on the gates of the power MOSFETs, some power is dissipated every time the switching occurs. This is represented in Equation 6.

$$P_{SW} = \frac{V_M^2 \times I_{OUT(RMS)} \times f_{SW}}{SR} \quad (6)$$

Where:

- V_M = supply voltage that is supplied to motor, otherwise known as motor voltage
- $I_{OUT(RMS)}$ = RMS output current being applied to the motor windings (not to be confused with the supply current)
- f_{SW} = switching frequency of the PWM signal
- SR = slew rate of the switching signal.

The DRV10987 has a maximum output current of 2 $A_{(RMS)}$ and can operate with a supply voltage from 6.2 V to 28 V. The PWM switching frequency is configured for 25 kHz or 50 kHz and the slew rate can be configured for 120, 80, 50, or 35 V/µs.

2.3 Operating Supply Current Dissipation

The driver consumes some current during operation. Note that the absence of a speed command can place the devices into sleep or standby to minimize current. However, the power dissipated calculations only rely on operation conditions. This is shown in Equation 7:

$$P_{IVM} = I_{VCC} \times V_M \quad (7)$$

Where:

- V_M = supply voltage that is supplied to motor, otherwise known as motor voltage
- I_{VCC} = active current during operation

The DRV10987 uses the specification called active current to quantify the amount of supply current consumed during operation. Note that the DRV10987 includes a step-down hysteretic voltage regulator that can operate with an external inductor or resistor. Depending on the component and mode used in the design, the active current is defined differently. Consult *DRV10987 12- to 24-V, Three-Phase, Sensorless BLDC Motor Driver* in the step-down regulator section for more information.

The typical value of the active current in the resistor mode is 13 mA, the maximum value is 16 mA.

2.4 Other Power Dissipation

Many motor drivers, including the DRV10987, have an LDO regulator that provides some current. The LDO offered on the DRV10987 outputs 3.3 V and more information is found in *DRV10987 12- to 24-V, Three-Phase, Sensorless BLDC Motor Driver* . This is represented in Equation 8:

$$P_{LDO} = I_{LDO\_OUT}(V_M - V_{OUT}) \quad (8)$$

Where:

- I_{LDO_OUT} = output current from the LDO with load
- V_M = supply voltage that is supplied to motor, otherwise known as motor voltage
- V_{OUT} = output voltage of the LDO

If the LDO is not outputting any current, ignore this power dissipation.

3 Understanding Thermal Resistance

For many semiconductor devices, the junction-to-thermal resistance is often given as a specification in the data sheet. For example, the DRV10987 shows θ_{JA} is 36.1 °C/W. While this specification is based on data and JEDEC standards, the junction-to-thermal resistance does not account for real world factors and good thermal design like board thickness, use of a die attach pad (DAP) or power pad, copper thickness, vias, and breaks in the thermal path. These factors can reduce the thermal resistance making it easier for heat to uniformly dissipate and reduce the junction temperature.

3.1 Simplified Model

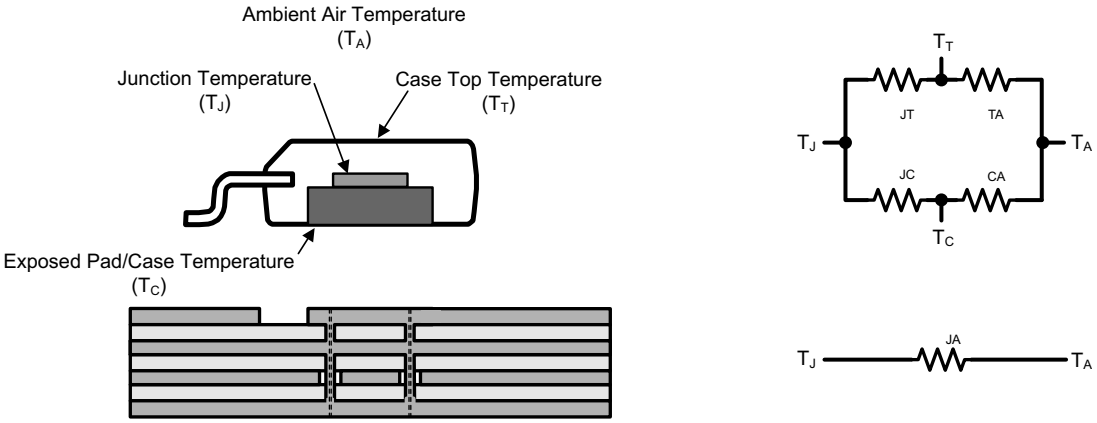

Figure 2. Simplified Thermal Resistance Model for a Typical PCB

As Figure 2 illustrates, the thermal model shows that the junction-to-ambient thermal resistance is but one component. However, the thermal resistance can be broken up into multiple parallel paths that make up all of the thermal resistance. In this case, a simplified version of the model is used.

Figure 2 shows that there are two paths for heat to travel from the junctions of the silicon: up towards the top of the case and down towards the power pad through the bottom of the PCB. This equivalent thermal resistance is found in Equation 9:

$$\theta_{JA} = (\theta_{JT} + \theta_{TA}) || (\theta_{JC} + \theta_{CA}) \quad (9)$$

Where:

- θ_{JT} = junction-to-case (top) thermal resistance
- θ_{TA} = case (top) to ambient thermal resistance
- θ_{JC} = junction-to-case (power pad or equivalent path of least resistance) thermal resistance
- θ_{CA} = case (power pad or equivalent path of least resistance) to ambient thermal resistance (through PCB)

Equation 9 describes an important relationship for identifying the thermal resistance of the system. θ_{JT}, θ_{TA}, and θ_{JC} are all fixed values that cannot be influenced by the designer. However, θ_{CA} can be greatly reduced applying good thermal design. Since the paths to the top and bottom of the case are in parallel, if the θ_{CA} is reduced to a small enough value, ignore the path to the top of the case.

NOTE: θ_{JT}, θ_{TA}, and θ_{JC} are all values that are widely known or found in the data sheet where θ_{CA} is calculated.

3.2 Factors of Junction-to-Case Thermal Resistance (θ_{CA})

As Figure 3 shows, there are many paths for heat to travel: through the copper plane laterally, vertically through thermal vias, through the vertical FR-4 laminate of the PCB, and radiating off the surface of the board to the ambient air. These paths are broken into parallel paths where the thermal resistance varies. As previously mentioned, it is important to make every path low resistance. As a result, higher resistance paths such as paths using the FR-4, contribute less to the overall θ_{CA}.

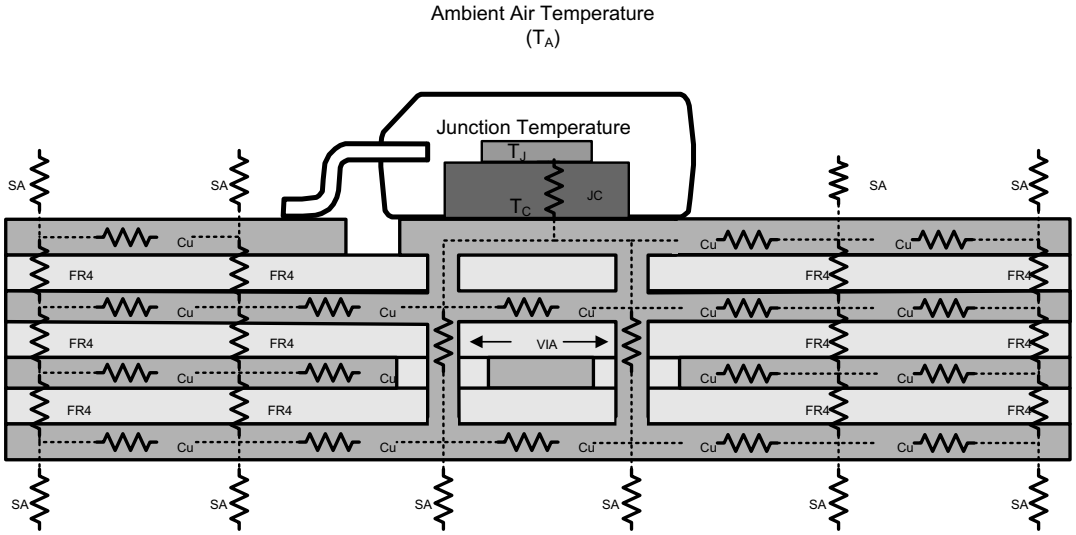

Figure 3. Expanded Thermal Resistance Model for a Typical PCB

While these thermal resistances are modeled like resistors in an electrical circuit model, the modeled resistor network is complicated and may not perfectly model the board. Generally, vias and copper planes have a lower thermal resistance than the FR-4 laminate of the PCB. Equations and typical values for these factors are found in *AN-2020 Thermal Design By Insight, Not Hindsight* . However, the effects of these equations are summarized into general guidelines and design rules in Section 5 with supporting data in Section 4.

NOTE: A useful θ_{CA} and θ_{JA} can be obtained through thermal modeling PCB simulation software. However, this modeling is usually provided as a service and associated as an extra cost during production.

4 Example Calculations and Data

Before showing the typical calculations and data collection used in thermal analysis, the methods for finding the junction temperature must be discussed.

$$T_J = P_D \times \theta_{JA} + T_A \quad (10)$$

As previously mentioned, Equation 10 shows the very inaccurate and rough measurement that is typically used to calculate the junction temperature. This method does not take into account the effects of good thermal PCB design.

$$T_J = P_D \times \Psi_{JT} + T_C \quad (11)$$

Where:

- Ψ_{JT} = junction to top of case characterization parameter
- T_C = temperature at the top of the case

Equation 11 illustrates how junction temperature is calculated when measuring the temperature at the top of the case. Using the measured temperature at the top of the case and power dissipation, the characterization parameter Ψ_{JT} is taken from the data sheet to calculate the junction temperature.

While θ_{JT} is often confused for Ψ_{JT} when doing the calculation, the use of junction to top of case thermal resisitance, θ_{JT}, only works in context of Equation 9 and the modeling of the parallel paths discussed in Section 3.1 and Section 3.2.

The characterization parameter Ψ_{JT} is based on widely-adopted standards (JEDEC51-2). Furthermore, Ψ_{JT} estimates junction temperature based on experimental data instead of theoretical modeling. As a result, use Ψ_{JT} when the actual case temperature is measured. More information is found in *Semiconductor and IC Package Thermal Metrics* .

Note that the JEDEC standards were developed to help standardize sizes and layout for testing thermal metrics in most data sheets. Look for the verbiage indicating JEDEC standards when evaluating thermal metrics between different devices.

4.1 Power Dissipated Example Calculation

Assumptions for calculations are based on measured or typical and maximum electrical characteristic values:

- Two boards with two different devices were tested using the same HSOP package size to minimize thermal resistance error.
- Board 1 was not optimized for thermal performance where board 2 was optimized.
- Board 1 had a one-oz copper pour while board 2 had a two-oz copper pour.
- V_{CC} = 19.6 V and $T_{A\_Measured}$ = 24°C.
- For simplicity, $I_{OUT(RMS)}$ = 2.9 $A_{(RMS)}$ for both boards despite $I_{OUT(RMS)\text{-}Board1}$ = 2.85 $A_{(RMS)}$ and $I_{OUT(RMS)\text{-}Board2}$ = 2.95 $A_{(RMS)}$. This introduces some error in favor of board 2.
- $R_{DS(on)}$ value assumes T_A = 25°C where $T_{A\_Measured}$ = 24°C. This will introduce some error for both boards.
- Slew rate (SR) was set to 35 V/µs and the PWM frequency was set to 25 kHz.
- Both boards were in inductor mode. The maximum specification (15 mA) was used for margin.
- The LDO had no load in both experiments.
- The same motor was used with both boards in same environment to minimize error.

Calculating P_{RDS}, more information is available in Section 2.1. Note 250 mΩ is the typical value for $R_{DS(on)}$ at T_A = 25°C, as mentioned in the assumptions:

$$P_{RDS} = 1.5 \times R_{DS(ON)} \times \left(I_{OUT(RMS)}\right)^2$$
$$P_{RDS} = 1.5(250 \times 10^{-3}) \times (2.9)^2$$
$$P_{RDS} = 3.154 \quad W \tag{12}$$

Calculating P_{SW}, more information is available in Section 2.2:

$$P_{SW} = \frac{V_M^2 \times I_{OUT(RMS)} \times f_{SW}}{SR}$$
$$P_{SW} = \frac{\left(19.6\right)^2 \times \left(2.9\right) \times \left(25 \times 10^3\right)}{\left(35 \times 10^6\right)}$$
$$P_{SW} = 0.796 \quad W \tag{13}$$

Calculating P_{IVM}, more information is available in Section 2.3:

$$P_{IVM} = I_{VCC} \times V_M$$

$$P_{IVM} = (15 \times 10^{-3}) \times (19.6)$$
$$P_{IVM} = 0.294 \quad W \tag{14}$$

Calculating P_{LDO_OUT}, more information is available in Section 2.4:

$$P_{LDO} = I_{LDO\_OUT}(V_M - V_{OUT})$$
$$P_{LDO} = (0)((19.6) - (3.3))$$
$$P_{LDO} = 0 \quad W \tag{15}$$

Calculating P_D:

$$P_D = P_{RDS} + P_{SW} + P_{IVM} + P_{LDO}$$
$$P_D = (3.154) + (0.796) + (0.294) + (0)$$
$$P_D = 4.244 \quad W \tag{16}$$

This value is used to calculate T_J.

4.2 Example: Board 1

To estimate the junction temperature (T_J) of the device, we use both Equation 10 and Equation 11. As previously mentioned, Equation 10 is inaccurate as an estimation. In the previous section we calculated the power dissipated on board 1 as 4.244 W. From the data sheet, θ_{JA} is 36.1°C/W and the Ψ_{JT} is 0.4°C/W. We use the measured value (157.5°C) of the top-of-case temperature when the device is dissipating 4.244 W for T_C. Figure 4 shows the measured top-of-case temperature for board 1.

$$T_J = (P_D \times \theta_{JA}) + T_A = (4.244 \times 36.1) + 24$$
$$T_J = 177.2°C \tag{17}$$

Where:

- T_A = ambient temperature
- T_J = junction temperature
- P_D= power dissipated
- θ_{JA} = junction-to-ambient thermal resistance

$$T_J = (P_D \times \Psi_{JT}) + T_C = (4.244 \times 0.4) + 157.5$$
$$T_J = 158.7°C \tag{18}$$

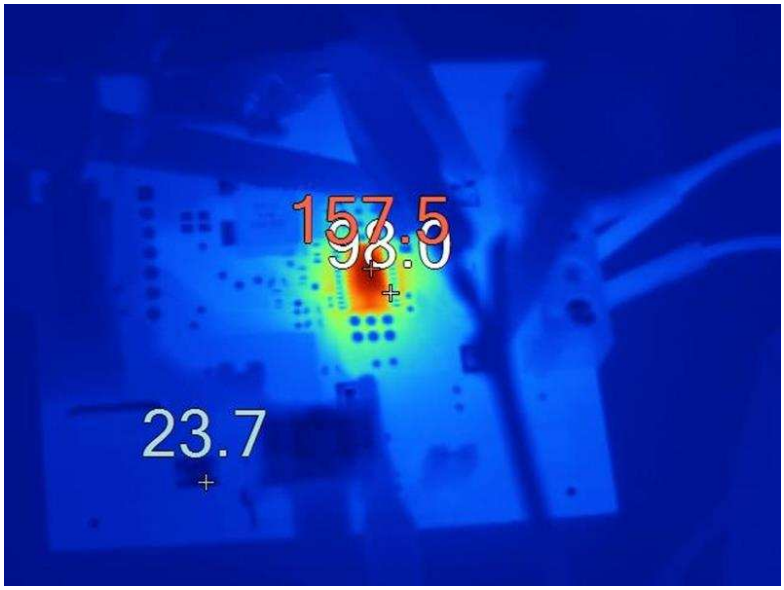

Figure 4. Board 1 Thermal Image for Top of Case Temperature

4.3 Example: Board 2

As with board 1, solving for T_J with the same power dissipation at the same ambient temperature, the junction temperature equals 291.07°C. This is because Equation 10 does not take into account PCB layout thermal techniques.

As for Equation 11, the only change is the measured T_C which is caused by thermal optimization techniques. Figure 5 shows the Top of Case temperature for Board 2.

$$T_J = (P_D \times \Psi_{JT}) + T_C = (4.244 \times 0.4) + 139.1$$
$$T_J = 140.8°C \quad (19)$$

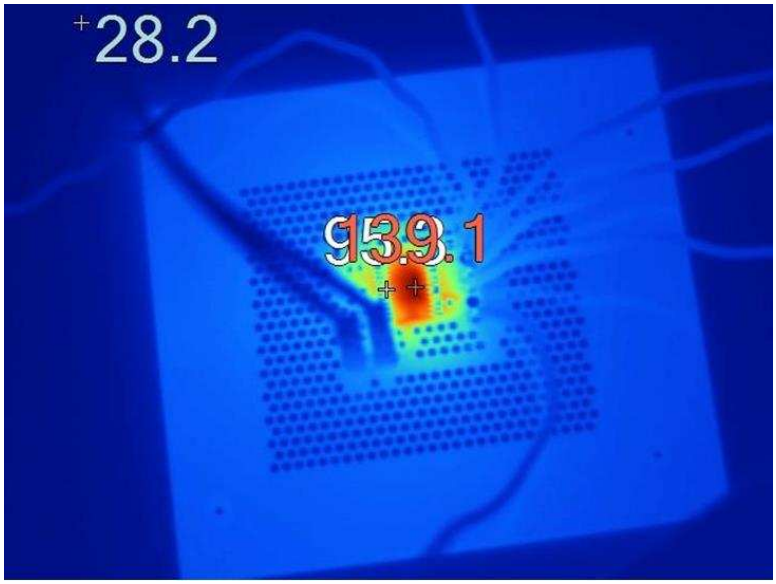

Figure 5. Board 2 Thermal Image for Top of Case Temperature

4.4 Test Results Summary

Table 1 and Table 2 show the measured thermal performance of board 1 and board 2, respectively.

Table 1. Board 1 Thermal Performance

Speed (RPM)	I RMS (A)	Voltage	Top of Case Temperature (°C)	Power (W)
6090	1.88	19.65	71.8	36.942
6420	2.05	19.6	79.1	40.18
6750	2.24	19.6	84.7	43.904
7140	2.4	19.64	91.8	47.136
7410	2.54	19.57	103.4	49.7078
7800	2.68	19.6	118.0	52.528
8190	2.78	19.6	132.4	54.488
8460	2.85	19.6	157.5	55.86

Table 2. Board 2 Thermal Performance

Speed (RPM)	I RMS (A)	Voltage	Top of Case Temperature (°C)	Power (W)
6150	1.52	19.57	53.8	29.746
6540	1.66	19.64	57.3	32.602
6930	1.824	19.63	61.9	35.8051
7230	1.975	19.55	67.1	38.611
7650	2.12	19.56	74.7	41.467
8010	2.24	19.57	81.4	43.837
8220	2.38	19.57	91.3	46.577
8490	2.54	19.55	102.6	49.657
8820	2.65	19.5	115.9	51.675
9150	2.78	19.43	123.4	54.0154
9330	2.95	19.41	139.1	57.318
9570	3.075	19.41	144.1	59.686

As the calculated and measured results show, using good thermal optimization layout techniques provides significant improvements in thermal performance allowing for better efficiency and higher power consumption while driving a motor. The calculations also show how using Equation 10 can be inaccurate for estimating a junction temperature far greater than the thermal shutdown temperature. Using Equation 11 is a better estimate for the junction temperature resulting in a realistic junction temperature.

5 Guidelines for Optimizing Thermal Performance

Use the following recommendations as guidelines for designing the PCB for thermal testing or functional evaluation:

- Use a large and multi-layer PCB:
  - Use Equation 20 to find the minimum recommended board size if θ_{JC} is unknown:

$$\text{Board Area } (\text{cm}^2) \geq 15.29 \ \frac{\text{cm}^2}{\text{W}} \times P_D$$

$$\text{Board Area } (\text{in}^2) \geq 2.37 \ \frac{\text{in}^2}{\text{W}} \times P_D \quad (20)$$

  - Use Equation 21 to find minimum recommended board size if θ_{JC} is known:

$$\text{Board Area } (\text{cm}^2) \geq 500 \frac{\frac{°\text{C} \times \text{cm2}}{\text{W}}}{\theta_{JA} - \theta_{JC}}$$

$$\text{Board Area } (\text{in}^2) \geq \frac{77.5 \frac{°\text{C} \times \text{in}^2}{\text{W}}}{\theta_{JA} - \theta_{JC}} \quad (21)$$

- TI recommends using at least one-oz copper.
  - Two-oz copper is recommended for designs that dissipate more than 3 W.
  - Four-oz copper is recommended for designs that dissipate more than 6 W.
  - Figure 6 shows the affects of board size and copper weight on thermal performance.

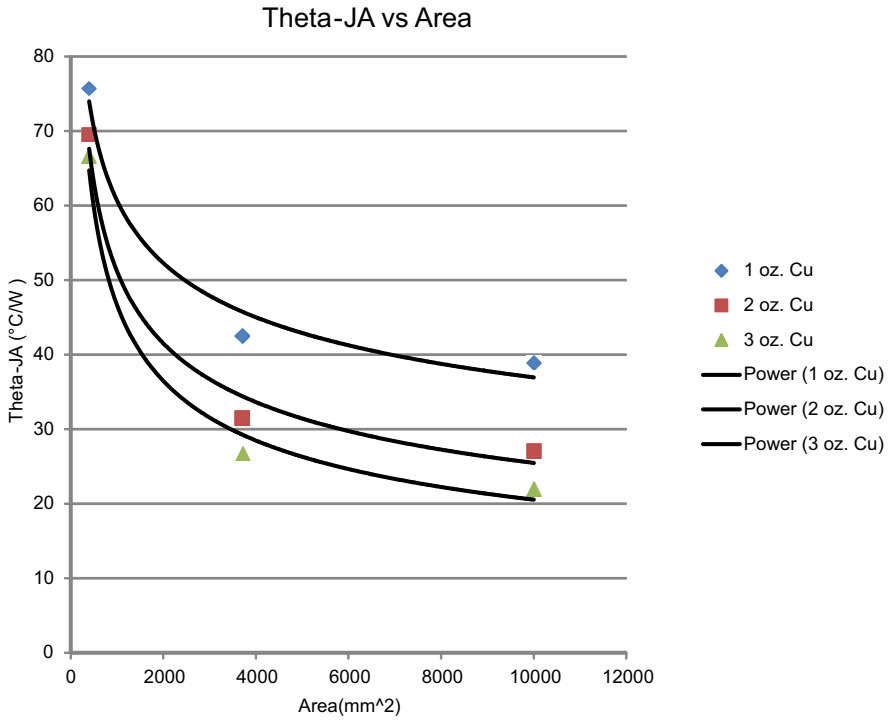

Figure 6. Thermal Simulation Data Comparing Board Size and Copper Weight

- Use thermal vias connecting the DAP landing pattern on the top layer, inter GND, and bottom GND layer in both DAP landing pattern and ground plane.
  - Use Equation 22 to find the thermal resistance of vias.

$$\theta_{VIA} \frac{\frac{1}{\lambda_{Cu}} \times Length}{\pi \times [(radius)^2 - (radius - plating\ thickness)^2]} \quad (22)$$

- Design the thermal vias near the periphery of the exposed DAP if the maximum number of vias is not applicable.
- Use 0.33-mm diameter vias if possible, especially for packages with small exposed pad, which may reduce θ_{JA} approximately 15% to 25%.
- Generate as large a GND plane as allowable on the top and bottom layers, especially near the package.
  - Generate with as few breaks as possible to create a heat spreader on the PCB.
- Connect the top GND pattern with the DAP landing pattern underneath the package.
- Gather the same functional pins together in die design, such as for GND, P_{VIN}, P_{OUT} in the power device. This allows maximizing the Cu area near the package by eliminating the needs for isolating each lead pattern on the PCB.
- Make the traces as long as possible, achieving better thermal conductivity near the package.
- Do not run traces parallel to the board edge, this blocks thermal path edges of the board

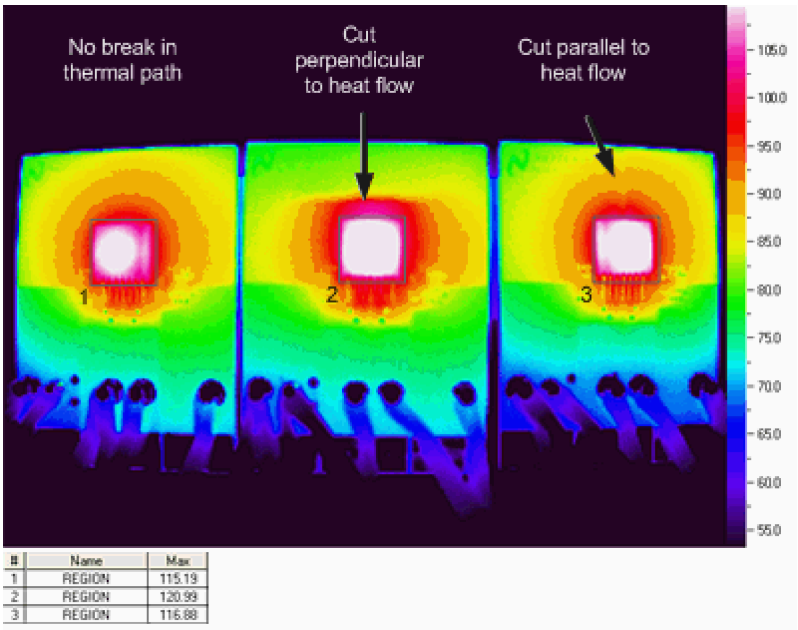

Figure 7. Hot Spot Created When a Break is Created in the Thermal Path

6 References

1. DRV10987 Product Folder: http://www.ti.com/product/DRV10987
2. Texas Instruments, *Calculating Motor Driver Power Dissipation Application Report*
3. Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight Application Report*
4. Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2017) to A Revision	Page
• Changed *Equation 5*.	3
• Added *thermal modeling PCB simulation software* note.	5
• Added last bullet in the *Power Dissipated Example Calculation* section.	6
• Changed *Equation 12*.	6
• Changed *Equation 13*.	6
• Changed 7.398 W to 4.244 W in the *Example: Board 1* section and made appropriate equation changes.	7
• Changed *Equation 18*.	7
• Changed *Equation 19*.	8

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