

How to Do PCB Modeling For a Power Converter

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ABSTRACT

PCB modeling is becoming more and more important in IC development. It is critical in the design stage, layout, and EMC design. This application report describes how to obtain the PCB model for a power converter and uses a buck converter as an example.

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1 Introduction

Nowadays, the parasitic of package and PCB become more and more critical in IC development. It is critical in the design stage and can help with IC simulation. Also, it is useful to judge a better layout to minimize the parasitic parameters and achieve a good EMC performance. The calculation for the EVM power loss and thermal analysis needs more accurate PCB modeling. The PCB modeling can be exported to Cadence netlist, which represents the equivalent circuit of the PCB.

2 The Basic of PCB Modeling

The basics of a PCB modeling is to build a 3D structure for the layout. Using the TPS563249 EVM as an example, [Figure 1](#) shows the ANSYS Q3D project file for one PCB. For a formal PCB file such as Altium Designer, it can all be set up as a 3D structure using Q3D analysis.

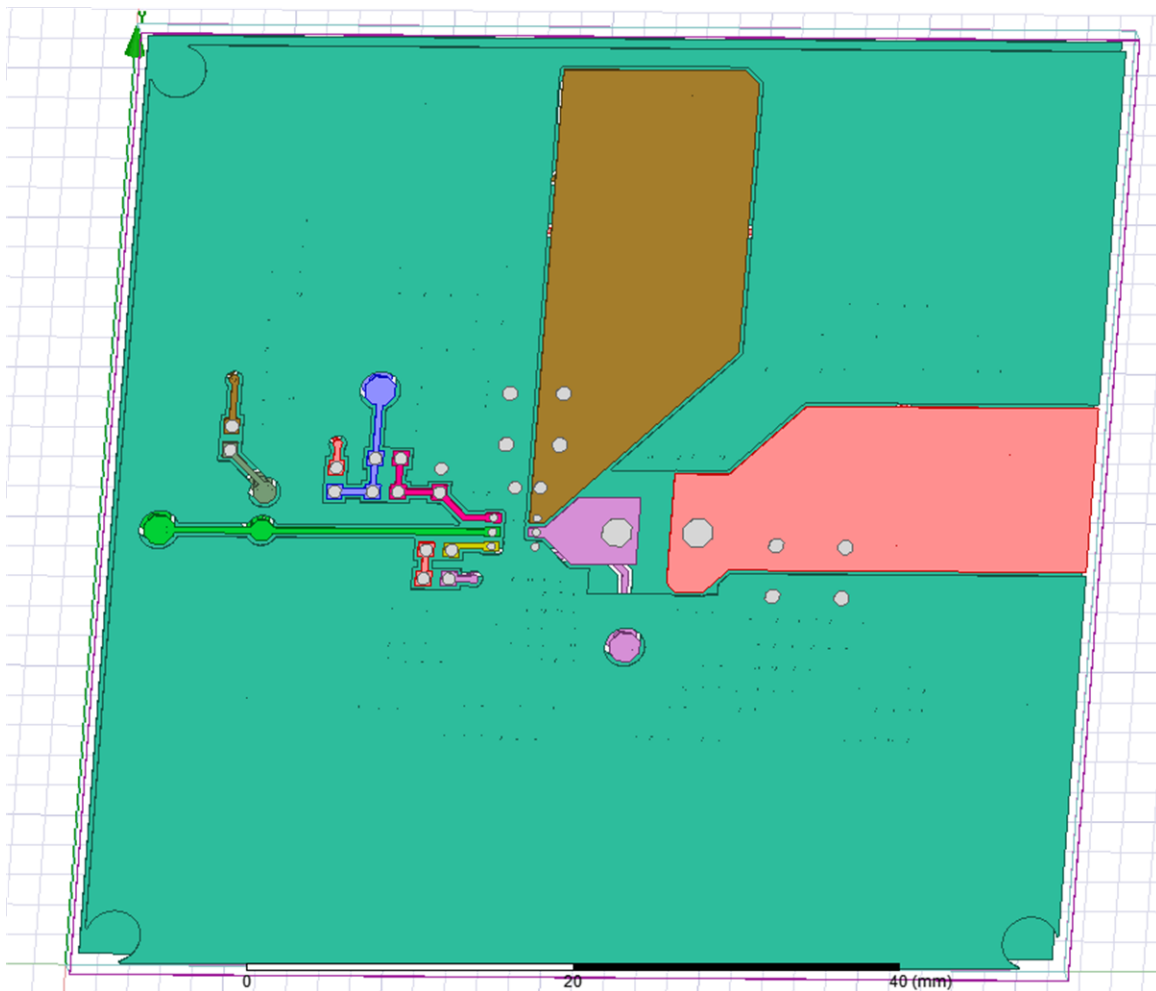


Figure 1. ANSYS Q3D File for TPS563249EVM

There are many critical nets for a buck converter PCB. Taking a D-CAP3 buck converter as an example, the feedback net and switching node net is more likely to be affected by noise. These nets are put at high priority for the PCB modeling and analysis. [Figure 2](#) shows the critical nets which use proper names. The ANSYS allows multiple source pins and only one sink pin to be defined on one net. [Figure 2](#) shows the sink positions are all fixed in IC pins.

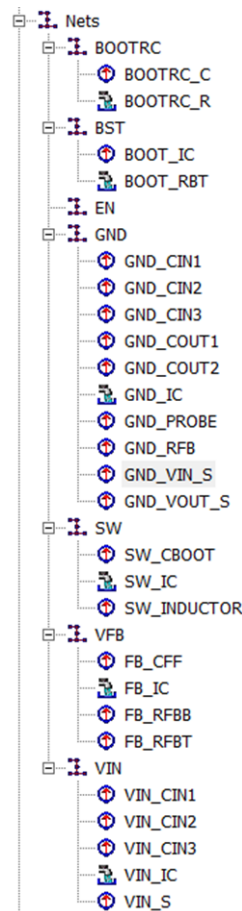


Figure 2. Critical Nets Shown in a Buck Converter

For example, the matrix data in Figure 3 and Figure 4 show the capacitance and inductance between two nets. For inductance, the diagonal element represents the inductance from the source to the sink on the very net. The off-diagonal element represents the mutual inductance between the two nets. In the Capacitance matrix, the off-diagonal elements are the mutual capacitances. The diagonal element represents the total capacitance of the very net including all mutual capacitance from this net to other nets and to the infinity ground.

Profile | Convergence | Matrix | Mesh Statistics

Conductance Units: mSie Maxwell Matrix 10 (MHz) Export...

Capacitance Units: pF Original All Freqs

Passivity Tolerance: .0001 Check Passivity Equivalent Circuit Export...

	BOOTRC	BST	GND	SW	VFB	VIN
Freq: 10 (MHz)						
BOOTRC	0.00031216, 0.33019	-1.2637E-05, -0.014825	-0.00026945, -0.2782	-1.1748E-05, -0.013729	-1.6612E-07, -0.00070004	7.4658E-09, -0.00030844
BST	-1.2637E-05, -0.014825	0.00031526, 0.33453	-0.00023974, -0.24501	-5.6803E-06, -0.006426	-3.6216E-06, -0.004728	1.0465E-08, -0.00069486
GND	-0.00026945, -0.2782	-0.00023974, -0.24501	0.038037, 39.327	-0.0028879, -2.9039	-0.00074399, -0.77223	-0.015009, -14.098
SW	-1.1748E-05, -0.013729	-5.6803E-06, -0.006426	-0.0028879, -2.9039	0.003039, 3.1223	-2.7066E-08, -0.00088249	-0.00012176, -0.15446
VFB	-1.6612E-07, -0.00070004	-3.6216E-06, -0.004728	-0.00074399, -0.77223	-2.7066E-08, -0.00088249	0.00082261, 0.87102	-7.494E-08, -0.0018951
VIN	7.4658E-09, -0.00030844	1.0465E-08, -0.00069486	-0.015009, -14.098	-0.00012176, -0.15446	-7.494E-08, -0.0018951	0.015395, 14.575

Figure 3. Capacitance Matrix

	BOOTRCBOOTRC_C	BST_BOOT_IC	GND_GND_CIN1	GND_GND_CIN2	GND_GND_CIN3	GND_GND_COUT1	GND_GND_COUT2	GND_GND_PROBE	GND_GND_RFB	GND_GND_VIN_S	GND_GND_VOUT_S
Freq: 10 (MHz)											
BOOTRCBOOTRC_C	0.00083149, 0.69136	0.00121	0.00074672	0.0011746	0.0015257	0.00086135	0.00089243	0.0005196	0.00088017	0.0024415	0.0012873
BST_BOOT_IC	0.000121	0.0013048, 1.2231	0.0005906	0.001082	0.0012547	0.0011278	0.0014547	0.0001818	0.00024689	0.0025963	0.00020571
GND_GND_CIN1	0.00074672	0.0005906	0.00042106, 1.5321	0.00031932, 1.5397	0.00028989, 1.5107	0.00022213, 0.53423	0.0002342, 0.56119	0.00017422, 0.043789	0.00029945, 1.3959	0.00025974, 1.6512	0.00022351, 0.42313
GND_GND_CIN2	0.0011746	0.001082	0.00031932, 1.5397	0.00042031, 2.1248	0.00033475, 2.1922	0.00023616, 0.57108	0.0002377, 0.59739	0.00018253, 0.04196	0.00032296, 1.7895	0.00028404, 2.4817	0.00023791, 0.37676
GND_GND_CIN3	0.0015257	0.0012547	0.00028989, 1.5107	0.00033475, 2.1922	0.0004402, 2.9184	0.00024308, 0.64499	0.00024484, 0.68289	0.0001862, 0.034417	0.00031581, 1.9195	0.00030217, 3.3929	0.00024518, 0.39628
GND_GND_COUT1	0.00086135	0.0011278	0.00022213, 0.53423	0.00023616, 0.57108	0.00024308, 0.64499	0.00044972, 4.5758	0.0004534, 4.757	0.00020246, 0.53965	0.00023806, 0.31974	0.00025207, 0.26489	0.00031026, 5.1168
GND_GND_COUT2	0.00089243	0.0014547	0.0002342, 0.56119	0.0002377, 0.59739	0.0002484, 0.68289	0.0004534, 4.757	0.00045838, 5.8842	0.00020201, 0.54516	0.00023962, 0.28966	0.00025461, 0.25565	0.00032714, 6.4017
GND_GND_PROBE	0.0005196	0.0001818	0.00017422, 0.043789	0.00018253, 0.04196	0.0001862, 0.04417	0.00020246, 0.53965	0.00020201, 0.54516	0.00033317, 0.77136	0.00018413, 0.079459	0.00019172, -0.059068	0.000202, 0.65116
GND_GND_RFB	0.00024689	0.00029945, 1.3959	0.00022962, 1.7895	0.00031581, 1.9195	0.00023088, 0.31974	0.00023962, 0.28966	0.00018413, 0.079459	0.00046708, 2.4574	0.00023705, 2.5167	0.00023807, 0.0715594	0.00022387, 0.0715594
GND_GND_VIN_S	0.0024415	0.0025963	0.00025974, 1.6512	0.00028404, 2.4817	0.00030217, 3.3929	0.00025207, 0.26489	0.00025461, 0.25565	0.00019172, -0.059068	0.00023705, 2.5167	0.00046844, 9.6656	0.00025614, -0.44899
GND_GND_VOUT_S	0.0012873	0.00020571	0.00022351, 0.42313	0.00023791, 0.37676	0.00024518, 0.39628	0.00031026, 5.1168	0.00032714, 6.4017	0.000202, 0.65316	0.00023987, 0.0016594	0.00025614, -0.44099	0.00039933, 10.153
SW_SW_CBOOT	0.0062679	0.0040197	0.0029657	0.003117	0.0027619	0.0027646	0.0014842	0.00059295	0.00058079	0.0038627	0.0019495
SW_SW_INDUCTOR	0.00094063	0.0016787	0.0010648	0.0014225	0.0012988	0.002314	0.0017072	0.00087651	0.00034019	0.0028384	0.000202, 0.65116
VFB_FB_OFF	0.0098318	0.0039099	0.0070212	0.0040843	0.0046668	0.0038553	0.0048629	0.00028211	0.00075711	0.003782	0.0069408
VFB_FB_RFB	0.0045437	0.0028995	0.0041107	0.0025789	0.0036911	0.0023541	0.0028563	0.00005111	0.00052526	0.00071501	0.0041621
VFB_FB_FBT	0.0054208	0.0039619	0.00071999	0.0025684	0.0040668	0.0035561	0.0043586	0.00046198	0.00069769	0.0006492	0.0064291
VIN_VN_CIN1	0.0034752	0.0012551	0.0001672	0.001899	0.0022427	0.00060757	0.00062028	0.00040176	0.00010596	0.0003333	0.0011442
VIN_VN_CIN2	0.0047479	0.0054864	0.011354	0.034363	0.052379	0.0020549	0.00060097	0.00066577	0.0013724	0.0007845	0.0010245
VIN_VN_CIN3	0.011202	0.006489	0.014129	0.049476	0.07194	0.0068466	0.00252605	0.0009565	0.0023959	0.014501	0.0023114
VIN_VN_S	0.023384	0.01743	0.016006	0.0726	0.14909	0.031119	0.045952	0.0016033	0.012306	0.040563	0.016212

Figure 4. Inductance Matrix

3 Bench Verification

Taking the TPS563249 EVM as an example, Figure 5 shows the simple parasitic inductance model according to the simulation result for the main power stage if mutual inductance is ignored. It is important for the design stage, especially for a converter whose MOSFET is inside the IC. It is also critical to design a RC snubber circuit to achieve good EMI performance.

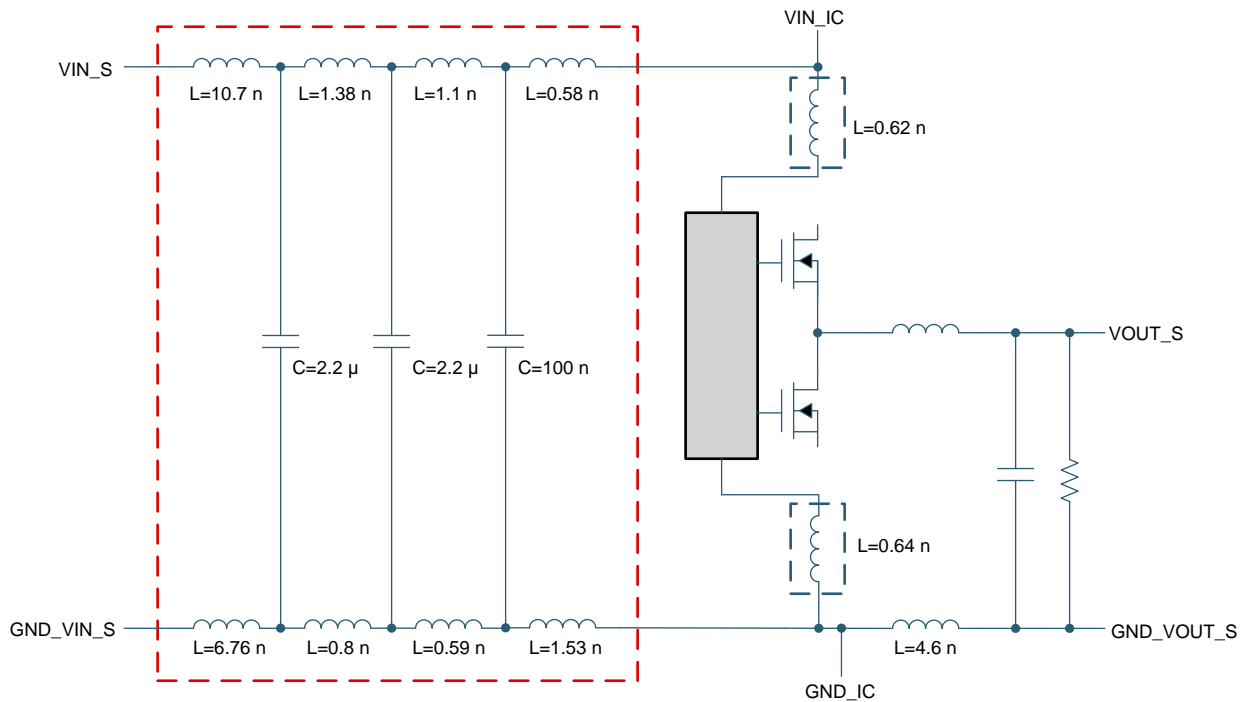


Figure 5. Simulation Results

Figure 6 shows the equivalent circuit analyzed from Q3D file. In the design stage, this can be imported into Cadence and helps simulate the high frequency signal and noise.

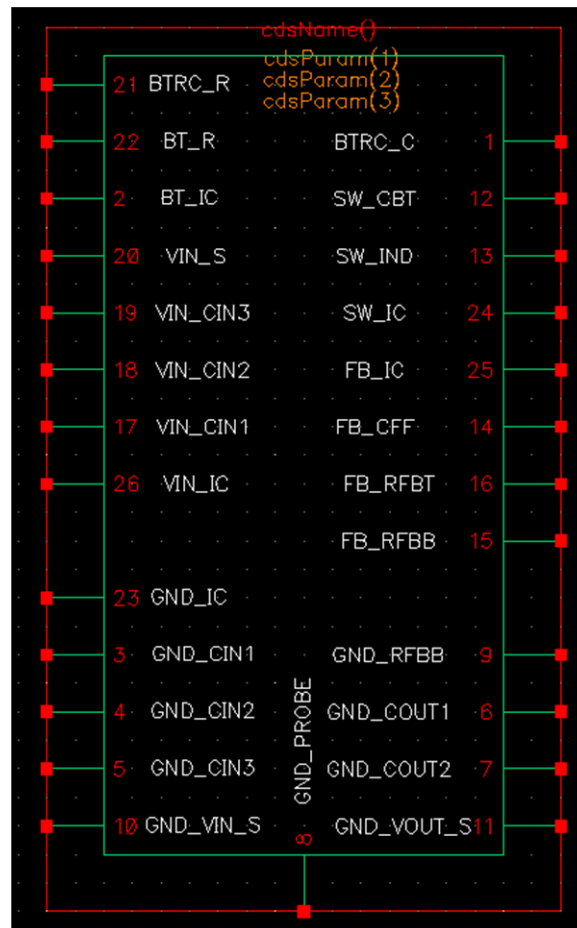


Figure 6. Equivalent Circuit for PCB Model in Cadence

4 Conclusion

This application report introduces how to achieve a PCB model including parasitic resistance, inductance, and capacitance. A buck converter PCB model is built taking the TPS563249EVM as an example. The equivalent circuit and parasitic parameter matrix are analyzed.

5 References

- Texas Instruments, [How SYNC Logic Affects EMI Performance for Dual-Channel Buck Converters Application Report](#)
- Texas Instruments, [How to Extend Buck Regulator to Positive Buck-Boost Configuration Application Report](#)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2018) to A Revision	Page
• Edited application report for clarity.	1

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