Application Report
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Power Stage Gain and Slope Compensation Measurement in PCM (Peak Current Mode) BUCK Converter

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ABSTRACT

This application report introduces a method to measure the power stage gain (G_{M-PS}) and slope compensation (S_e) in a PCM (Peak Current Mode) BUCK converter. It also introduces how to verify this method on the TPS65261.

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Trademarks

1 Introduction

PCM (Peak Current Mode) architecture is widely used in DC/DC converters. PCM architecture provides good performance and ease of compensation. Power stage gain and slope compensation play important roles in the PCM BUCK converter. They can suppress subharmonic oscillation and keep the control loop stable. With these parameters, you can deeply optimize power supply and ensure performance in mass production. Usually, the typical power stage gain value is provided in the datasheet, but the slope compensation is seldom provided since it is integrated.

2 Unified PCM BUCK Converter

Figure 1 shows a PCM Buck converter, which is usually composed of several key blocks. It includes the following:

- Error Amplifier (EA)
- PWM Comparator (PWM)
- Slope Compensation (SLP)
- Current Sensing (CS)
- Clock (CLK)
- Power Stage
- Output Stage

The RC network after error amplifier compensates for the output pole and increases loop gain for stability. Typically, Figure 1 can explain PCM BUCK converters.

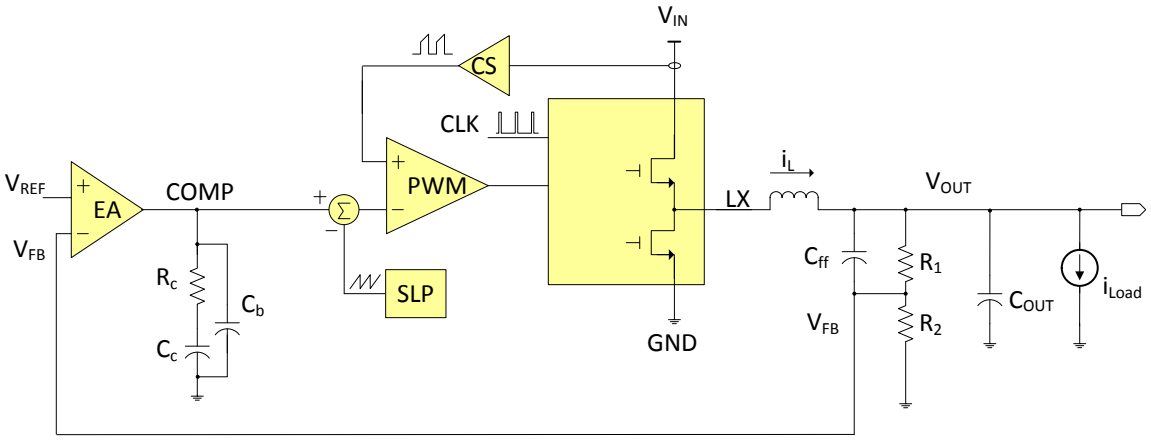

Figure 1. PCM BUCK Converter Block Diagram

During normal operation, the voltage difference between the internal reference voltage (V_{ref}) and the feedback voltage (V_{FB}) is amplified and outputs at COMP node. The clock signal (CLK) turns on high-side FET. The sensed current (CS) compares with the COMP voltage minus slope compensation (SLP) and the output logic is set to turn off high-side FET. The low-side FET turns on for the rest of the period.

Assuming the operating frequency is fixed, the slope compensation is linear, and the COMP is a pin that you can use to measure its voltage at this node. The whole application is explained based on this unified PCM model in CCM (Continuous Current Mode).

3 Power Stage Gain Measurement

Power Stage Gain (G_{M-PS}) is defined as the gain from COMP voltage (V_{COMP}) to inductor current (i_L). Equation 1 calculates the Power Stage Gain, where R_i is the current sensing gain.

$$G_{M\text{-}PS} = \frac{1}{R_i} = \frac{\Delta i_L}{\Delta V_{COMP}} \tag{1}$$

3.1 Simplified Small Signal Model for Power Stage Gain

Ignoring the inductor current ripple, the load current (i_{Load}) is equal to the inductor current (i_L) in CCM. Figure 2 shows a simplified whole system small signal model.

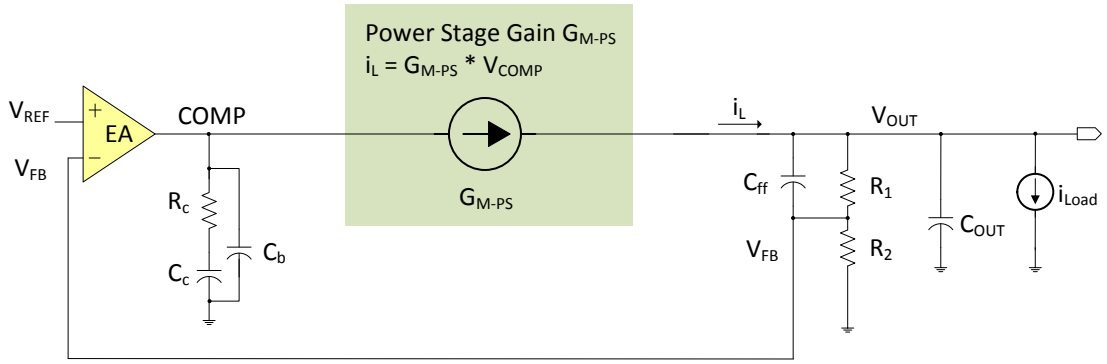

Figure 2. Simplified Small Signal Model for PCM BUCK Converter

Equation 2 calculates the AC small signal relationship between V_{COMP} and i_{Load}.

$$i_{Load} = i_L = G_{M-PS} * V_{COMP} \quad (2)$$

Equation 3 expresses the G_{M-PS}.

$$G_{M-PS} = \frac{i_{Load}}{V_{COMP}} \quad (3)$$

They are the small signal differential data where V_{COMP} and i_{LOAD} are not the directly measured data.

3.2 Power Stage Gain Measurement Method

G_{M-PS} is the AC small signal parameter. It must be measured by differentiated method. Table 1 shows step-by-step G_{M-PS} calculation guidelines.

1. Measure V_{COMP} at different loads in CCM from low current to high current.
2. Subtract V_{COMP} and load current with next data.
3. Equation 3 calculates G_{M-PS} for each condition.

Table 1. G_{M-PS} Calculation Guidelines

STEP 1		STEP 2		STEP 3
V_{COMP}	i_{Load}	Delta V_{COMP}	Delta i_{Load}	G_{M-PS}
V_{COMP1}	i_{Load1}			
V_{COMP2}	i_{Load2}	V_{COMP2} - V_{COMP1}	i_{Load2} - i_{Load1}	(i_{Load2} - i_{Load1}) / (V_{COMP2} - V_{COMP1})
V_{COMP3}	i_{Load3}	V_{COMP3} - V_{COMP2}	i_{Load3} - i_{Load2}	(i_{Load3} - i_{Load2}) / (V_{COMP3} - V_{COMP2})
...	...	...	...	...
$V_{COMP(N)}$	$i_{Load(N)}$	$V_{COMP(N)}$ - $V_{COMP(N-1)}$	$i_{Load(N)}$ - $i_{Load(N-1)}$	($i_{Load(N)}$ - $i_{Load(N-1)}$) / ($V_{COMP(N)}$ - $V_{COMP(N-1)}$)

4 Slope Compensation Measurement

Slope Compensation (S_e) is an added artificial signal in the control loop. It dampens the inner current loop gain and eliminates subharmonic oscillation when duty is over 50%. A common rule is to keep the compensation slope above or equal to half of inductor current falling slope, S_f.

4.1 Relationship Between V_{COMP} and S_e

Since the PWM comparator is a high gain element, it is reasonable to consider the positive input equal to the negative input when the high-side FET is turned off. Figure 3 shows the steady-state. Equation 4 calculates the small signal relationship between V_{COMP}, i_L, and S_e.

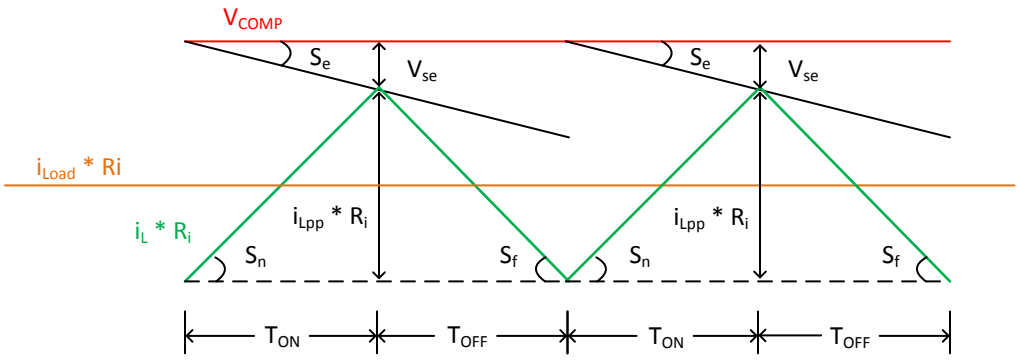

Figure 3. PWM Comparator Input Signals

$$V_{COMP} - V_{se} = V_{COMP} - S_e * T_{ON} = (i_{Load} + \frac{1}{2} * i_{Lpp}) * R_i \quad (4)$$

where

- i_{Lpp} is the inductor ripple current. Equation 5 calculates i_{Lpp}.

$$i_{Lpp} = \frac{V_{IN} - V_{OUT}}{L} * \frac{V_{OUT}}{V_{IN}} * \frac{1}{F_{SW}} \quad (5)$$

where

- R_i is the current sensing gain. Equation 1 and Equation 3 calculate R_i.
- T_{ON} is high-side FET ON time. Equation 6 calculates T_{ON}. You can also use an oscilloscope to measure the value.
- T_{OFF} is high-side FET OFF time

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} * \frac{1}{F_{SW}} \quad (6)$$

where

- S_n is the inductor current rising slope
- S_f is inductor current falling slope

In addition, the other parameters including the V_{COMP}, switching frequency (F_{SW}), input voltage (V_{IN}), and output voltage (V_{OUT}) can be measured in the lab.

4.2 Slope Compensation Measurement Method

Slope compensation (S_e) or V_{se} cannot be measured directly. It cannot be measured like G_{M-PS} at a different loading since V_{se} does not change with the loading, but changes with duty. Equation 7 calculates V_{se} in a steady-state for a different duty under the same loading, but different V_{IN} condition. Figure 4 illustrates V_{se}.

$$V_{se} = S_e * T_{ON} = V_{COMP} - (i_{Load} + \frac{1}{2} * i_{Lpp}) * R_i \quad (7)$$

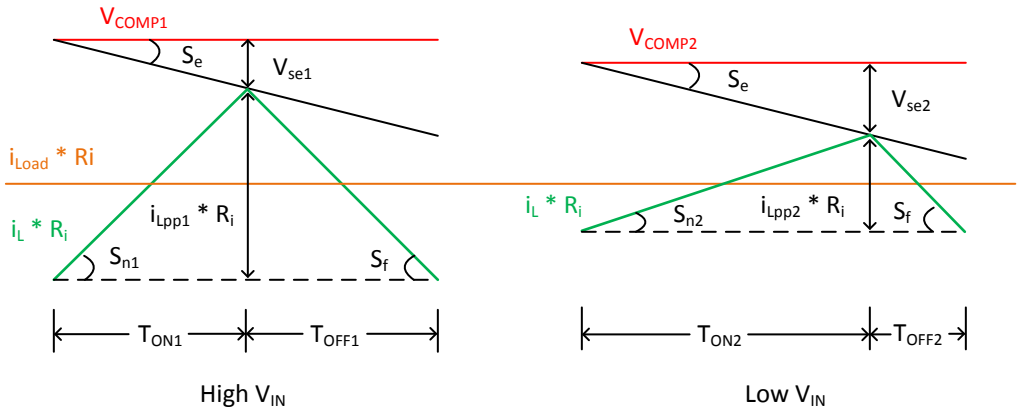

Figure 4. V_{se} for A Different Duty

Since directly measured V_{COMP} contains DC bias voltage, which introduces error, the S_e must be calculated by a differentiated method.

Equation 8 and Equation 9 calculate the different V_{se1} and V_{se2}.

$$V_{se1} = S_e * T_{ON1} = V_{COMP1} - (i_{Load} + \frac{1}{2} * i_{Lpp1}) * R_i \quad (8)$$

$$V_{se2} = S_e * T_{ON2} = V_{COMP2} - (i_{Load} + \frac{1}{2} * i_{Lpp2}) * R_i \quad (9)$$

Equation 10 calculates S_e. Subtract Equation 9 from Equation 8 and reform it.

$$S_e = \frac{V_{COMP2} - V_{COMP1} + \frac{1}{2} * (i_{Lpp2} - i_{Lpp1}) * R_i}{T_{ON2} - T_{ON1}} \quad (10)$$

where

- F_{SW} and R_i stay constant relative to V_{IN}

Table 2 shows step-by-step S_e calculation guidelines.

1. Measure V_{COMP} at different V_{IN} values in the CCM from low V_{IN} to high V_{IN}.
2. Use Equation 5 to calculate T_{ON} for each condition. Use Equation 4 to calculate $i_{Lpp}$for each condition.
3. Subtract V_{COMP}, V_{IN}, and i_{Lpp} with the next data.
4. Use Equation 10 to calculate S_e for each condition.

For some parts, the F_{SW} and R_i are not constant. More accuracy S_e values can be obtained by measuring F_{SW} for each condition and measuring current sensing gain R_i. Section 3 describes this process.

Table 2. S_e Calculation Guidelines

STEP 1		STEP 2		STEP 3			STEP 4
V_{COMP}	V_{IN}	T_{ON}	i_{Lpp}	Delta V_{COMP}	Delta V_{IN}	Delta i_{Lpp}	S_e
V_{COMP1}	V_{IN1}	T_{ON1}	i_{Lpp1}				
V_{COMP2}	V_{IN2}	T_{ON2}	i_{Lpp2}	V_{COMP2} - V_{COMP1}	V_{IN2} - V_{IN1}	i_{Lpp2} - i_{Lpp1}	Equation 10
V_{COMP3}	V_{IN3}	T_{ON3}	i_{Lpp3}	V_{COMP3} - V_{COMP2}	V_{IN3} - V_{IN2}	i_{Lpp3} - i_{Lpp2}	Equation 10
...	...	...	...	...	...	...	...
$V_{COMP(N)}$	$V_{IN(N)}$	$T_{ON(N)}$	$i_{Lpp(N)}$	$V_{COMP(N)}$ - $V_{COMP(N-1)}$	$V_{IN(N)}$ - $V_{IN(N-1)}$	$i_{Lpp(N)}$ - $i_{Lpp(N-1)}$	Equation 10

5 Measurement Results Verification

This section verifies the measurement method for G_{M-PS} and S_e on the TPS65261.

5.1 TPS65261 Measured G_{M-PS} and S_e

TPS65261 is a triple synchronous BUCK converter that is widely used in the market. The BUCK1 is selected to perform this verification. Set the application condition to the following:

- 12 V V_{IN}
- 3.3 V V_{OUT}
- 3 A loading
- 609 KHz F_{SW}
- 4.7 µH inductor
- 2 × 22 µF C_{OUT}

Figure 5 shows the TPS65261 typical application circuit. R263 is changed to 10 kΩ and R262 is changed to 45.3 kΩ for the V_{OUT} = 3.3 V setting. Due to the influence of parasitic parameters and measurement accuracy, the results shift slightly, so the average value is used for general purpose analysis.

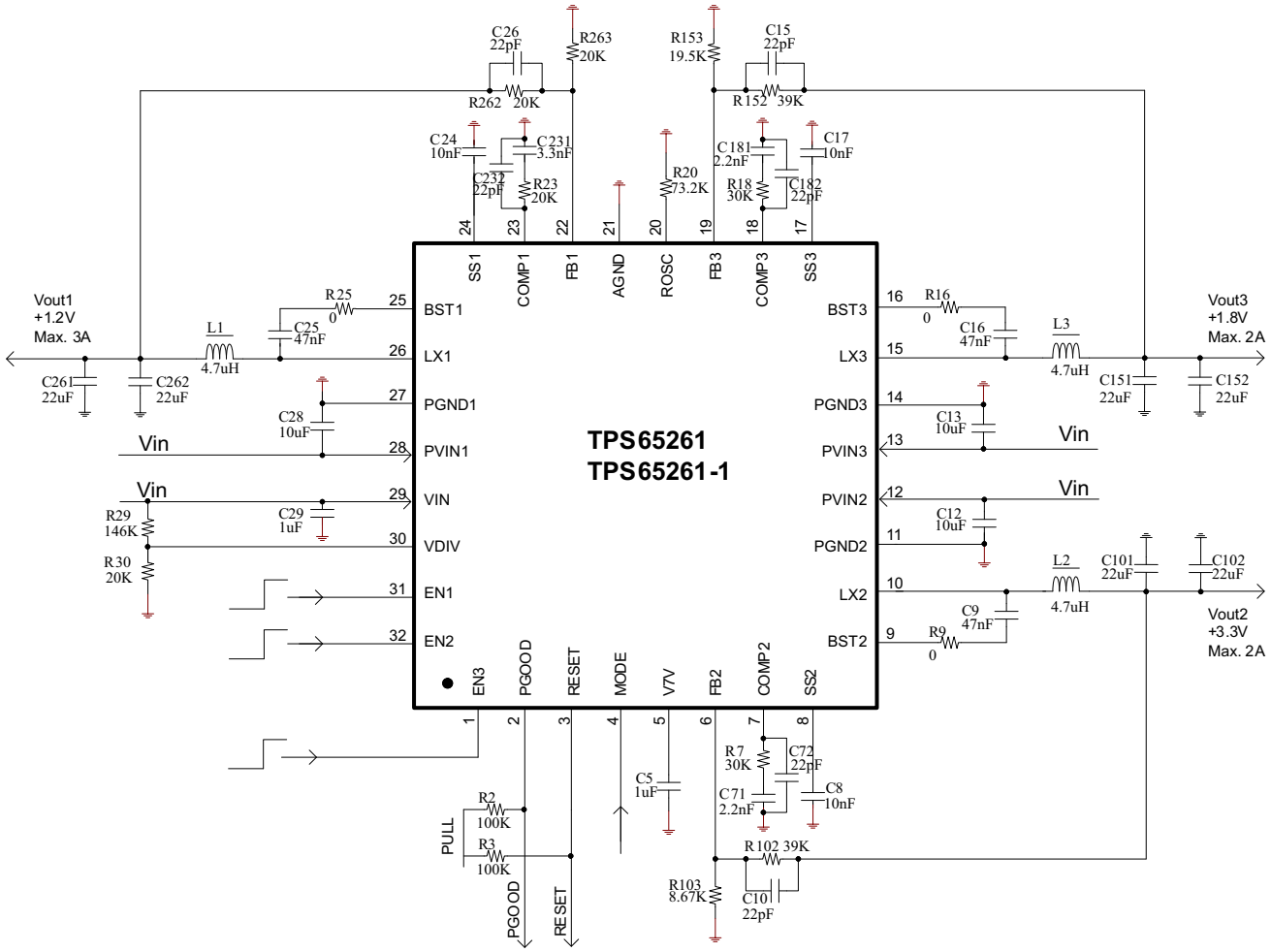

Figure 5. TPS65261 Typical Application Circuit

Table 3 shows a step-by-step power stage gain (G_{M-PS}) calculation. The average G_{M-PS} is 7.59 A/V and it is approximately equal to 7.4 A/V provided in the *TPS6526x 4.5 V to 18 V Input Voltage, 3A/2A/2A Output Current Triple Synchronous Step-Down Converter Data Sheet* .

Table 3. G_{M-PS} Calculation

STEP 1		STEP 2		STEP 3
V_{COMP}(V)	i_{Load}(A)	Delta V_{COMP}(V)	Delta i_{Load}(A)	G_{M-PS}(A/V)
0.6075	0.50			
0.6400	0.75	0.0325	0.25	7.692
0.6719	1.00	0.0319	0.25	7.837
0.7040	1.25	0.0321	0.25	7.788
0.7356	1.50	0.0316	0.25	7.911
0.7680	1.75	0.0324	0.25	7.716
0.8009	2.00	0.0329	0.25	7.599
0.8343	2.25	0.0334	0.25	7.485
0.8678	2.50	0.0335	0.25	7.463
0.9023	2.75	0.0345	0.25	7.246
0.9372	3.00	0.0349	0.25	7.163
Average Power Stage Gain G_{M-PS}				7.590

Table 4 shows a step-by-step slope compensation (S_e) calculation. The average S_e is 1.86E+05 V/S.

Table 4. S_e Calculation

STEP 1		STEP 2		STEP 3			STEP 4
V_{IN}(V)	V_{COMP}(V)	Calculated T_{ON}(uS)	Calculated i_{Lpp}(A)	Delta V_{COMP}(V)	Delta V_{IN}(V)	Delta i_{Lpp}(A)	Calculated S_e(V/S)
4.5	0.9727	1.204	0.307				
5	0.9409	1.084	0.392	-0.0318	0.5	0.042	2.18E+05
5.5	0.9165	0.985	0.461	-0.0244	0.5	0.035	2.01E+05
6	0.8972	0.903	0.519	-0.0193	0.5	0.029	1.89E+05
6.5	0.8812	0.834	0.568	-0.0160	0.5	0.024	1.84E+05
7	0.8668	0.774	0.609	-0.0144	0.5	0.021	1.96E+05
7.5	0.8541	0.722	0.646	-0.0127	0.5	0.018	2.00E+05
8	0.8432	0.677	0.677	-0.0109	0.5	0.016	1.95E+05
8.5	0.8340	0.637	0.705	-0.0092	0.5	0.014	1.85E+05
9	0.8259	0.602	0.730	-0.0081	0.5	0.012	1.82E+05
9.5	0.8187	0.570	0.752	-0.0072	0.5	0.011	1.81E+05
10	0.8119	0.542	0.772	-0.0068	0.5	0.010	1.92E+05
10.5	0.8061	0.516	0.791	-0.0058	0.5	0.009	1.79E+05
11	0.8009	0.493	0.807	-0.0052	0.5	0.008	1.75E+05
11.5	0.7961	0.471	0.822	-0.0048	0.5	0.008	1.78E+05
12	0.7918	0.452	0.836	-0.0043	0.5	0.007	1.73E+05
12.5	0.7878	0.433	0.849	-0.0040	0.5	0.006	1.75E+05
13	0.7842	0.417	0.860	-0.0036	0.5	0.006	1.70E+05
13.5	0.7807	0.401	0.871	-0.0035	0.5	0.005	1.80E+05
14	0.7774	0.387	0.881	-0.0033	0.5	0.005	1.84E+05
Average Slope Compensation S_e							1.86E+05

5.2 Measured Bode Plot vs. Calculated Bode Plot

Figure 6 shows the measured Bode Plot versus a simulated Bode Plot under a 2 A loading condition. This is performed by the TPS65261 SIMPLIS model with the above measured, calculated parameters G_{M-PS}, and S_e. The measured result is well-matched with a simulated result. The simulated GBW is 41 KHz and phase margin is 68 degrees. The lab-measured GBW is 42 KHz and phase margin is 66 degrees.

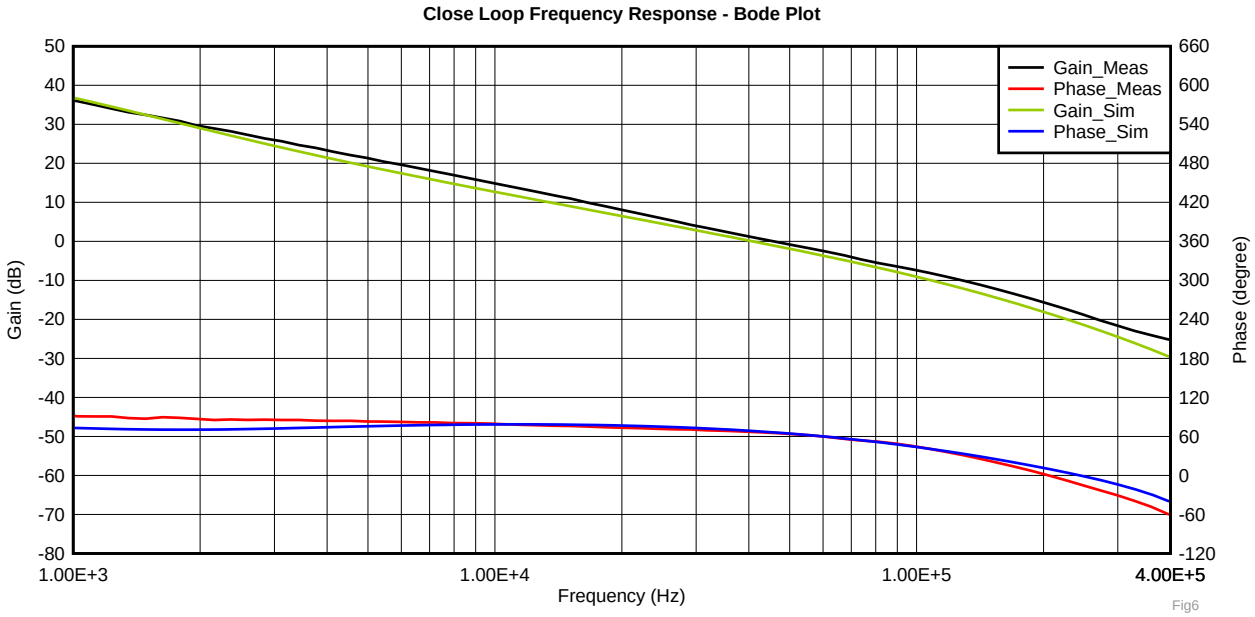

Figure 6. Measured Bode Plot vs. Calculated Bode Plot

6 Summary

This application report presents a method of measuring power stage gain (G_{M-PS}) and slope compensation (S_e) in a peak current mode (PCM) BUCK converter. This method is also validated in other PCM architecture converters, such as BOOST, BUCK-BOOST, and so forth. You can build the simulation model by using these internal parameters. Based on the model, the maximum optimization loop stability can be achieved.

7 References

1. Texas Instruments, *TPS6526x 4.5 V to 18 V Input Voltage, 3A/2A/2A Output Current Triple Synchronous Step-Down Converter Data Sheet*
2. Texas Instruments, *TPS65261EVM-650 PMIC 3-A, 2-A, 2-A Output Current Evaluation Module User's Guide*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2018) to A Revision	Page
• Edited application report for clarity.	1

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