Application Note

Achieve Output Discharge Function Using Power Good Indicator

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ABSTRACT

In some applications that require exact power sequencing for various circuits, output discharge function is necessary to improve system reliability in unexpected power events. This application note presents a method about how to achieve output discharge function by using PG indicator of TPS61033x boost converter. This document provides the parameter design method and gives an experimental result.

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Trademarks

1 Introduction

TPS61033x is a highly integrated boost converter, which can support 5 V output voltage and up to 2 A load current from a Li+ battery input. PG indicator of TPS61033x can provide the status of output voltage. But TPS61033x doesn't have output discharge function, which is a important feature many applications require for correct power sequence.

This application note introduces a method to achieve output discharge function with PG indicator. Using TPS61033 as an example, theoretical analysis and bench test result are presented to verify the proposed circuit.

2 Power Good Indicator

The power good signal is generated by a power supply when the supply voltage has reached target voltage and been stable. The most of electronic circuits or components can only operate normally when the supply voltage is within a certain range, if the supply voltage is out of this range, those circuits and components can't operate properly and even be damaged.

In this condition, a power good signal is used to make sure that all the supply voltages are always stable. A MCU or other kind of processors can be designed to monitor the power good signal. Only the supply voltage reaches proper voltage and is stable, the power good signal is generated and inform the processor that supply voltage is normal and can be supplied to other circuits and components. Once a failure power situation is detected, this signal can also inform processor immediately so that the processor can reset or stop operating.

For those power supply devices that doesn’t have power good signal, engineer needs to use comparators or ADCs to achieve this function. TPS61033 integrates a power good indicator to simplify sequencing and supervision. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connect to a stable voltage supply.

The PG indicator of TPS61033 is controlled by output voltage or enable. The PG pin goes high with a typical 1.3 ms delay time after VOUT is between 93% (typical) and 107% (typical) of the target output voltage. When the output voltage is out of the target output voltage window, the PG pin immediately goes low with a 33 µs deglitch filter delay. This deglitch filter also prevents any false pull-down of the PGOOD due to transients. When EN is pulled low, the PG pin is also forced low with a 33 µs deglitch filter delay.

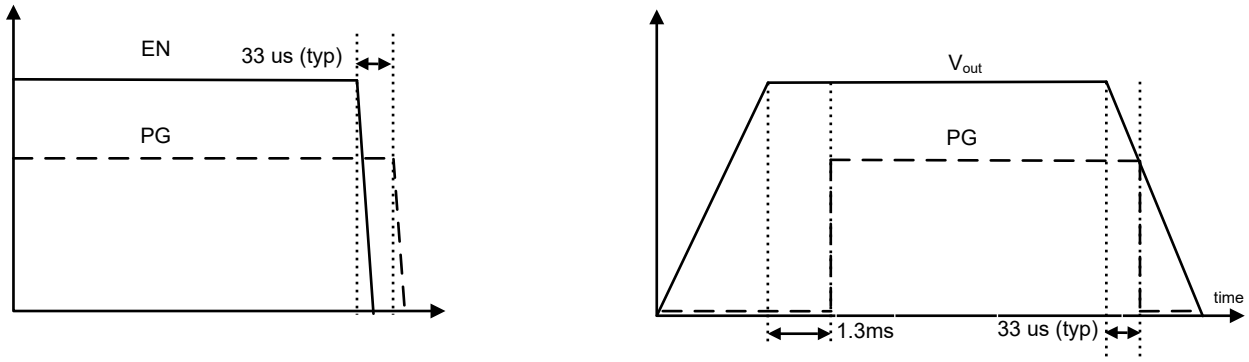

Figure 2-1. TPS61033 PG Indicator Scheme

3 Output Discharge Function

3.1 Why We Need Output Discharge Function

Output discharge function is used to make sure that output voltage discharge quickly when the device is disabled. This is necessary when the power system requires exact power sequencing for different circuits and components. Without output discharging function, some power rails are left floating when the system is disabled, and this probably cause some issues when the system is enabled again.

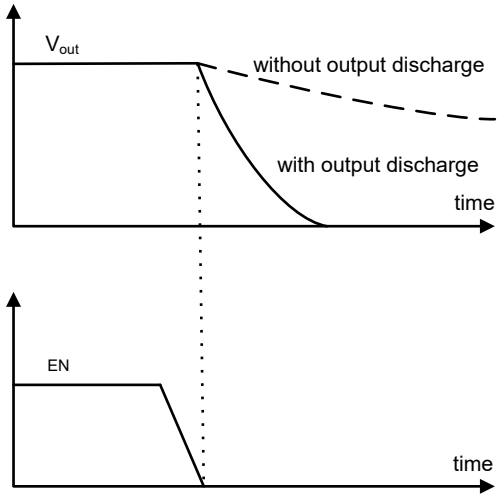

Figure 3-1. Output Discharge

TPS61033 can implement output discharge function by PG function that requires a pull-up resistor connected between PG pin and Vout pin, this pull-up resistor is also called dummy resistor (R_{Dummy}). As mentioned above, PG of TPS61033 is an open drain NMOS architecture with up to 50 mA current capability, the PG pin becomes logic high when the output voltage reaches the target value, so the dummy load resistor doesn't lead any power loss during normal operation. When the EN pin gets low, the TPS61033 is disabled and meanwhile the PG pin gets low with a typical 33 µs glitch time (tglitch). With PG pin keep low, the dummy resistor works as a dummy load to discharge output voltage. Changing R_{Dummy} can adjust the output discharge time and discharge current.

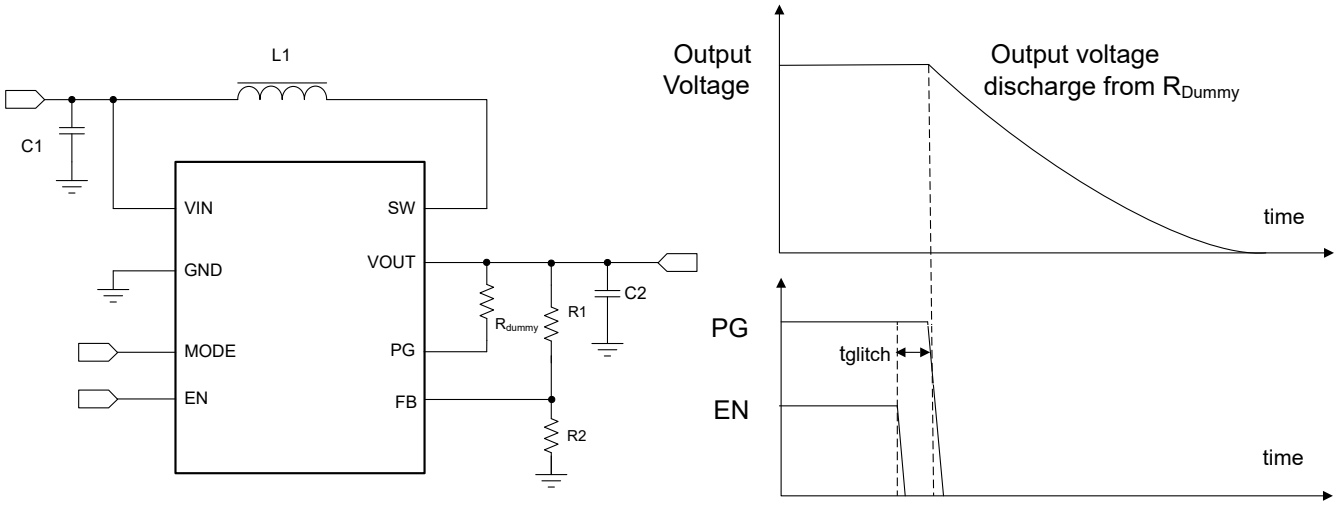

Figure 3-2. Output Discharge Using PG Indicator

3.2 How to Choose Dummy Resistor

The value of dummy resistor has impact on both output discharge time and maximum discharge current.

Considering the worst case, when the system is disabled, the load current is 0 A, then the output discharge time is calculated by:

$$t = \left(R_{Dummy} + R_{FET}\right)*C_{OUT}*\ln\left(\frac{1}{r}\right) \approx R_{Dummy}*C_{OUT}*\ln\left(\frac{1}{r}\right) \quad (1)$$

where

- R_{Dummy} is the dummy resistor
- R_{FET} is the Rds_on of open drain NMOS in PG pin, generally this is much smaller than dummy resistor, so can be ignored.
- C_{OUT} is the output capacitance.
- r is the ratio of the discharge terminal voltage (V_{TERMI}) to nominal output voltage (V_{OUT}).

$$r = \frac{V_{TERMI}}{V_{OUT}} \quad (2)$$

One thing needed to be noted that, if engineer uses aluminum electrolytic capacitor or tantalum capacitor, the C_{OUT} is the nominal capacitance, but if engineer uses ceramic capacitors, take care when evaluating the derating of a ceramic capacitor under dc bias voltage, the dc bias voltage can significantly reduce the effective capacitance. For example, for a 22 uF/10 V/0603 package ceramic capacitor, when dc bias is 5 V the effective capacitance is only about 5.5 uF. Therefore when using ceramic capacitors, we recommend to use the average value of nominal capacitance and effective capacitance when estimating the discharge time.

For example, when using two 22 uF/10 V/0603 package ceramic capacitors, we get C_{OUT} = 27.5 uF, if system requires the supply voltage needs to discharge to 20% nominal voltage (r = 0.2) within 50 ms, then

$$t = R_{Dummy}*C_{OUT}*\ln\left(\frac{1}{r}\right) < 50\ ms \quad (3)$$

So the maximum Rdummy resistor is 1.11k Ω.

Figure 3-3 shows a comparison between calculation discharging time and test discharge time (based on C_{OUT} = 27.5 uF, r = 0.2 condition).

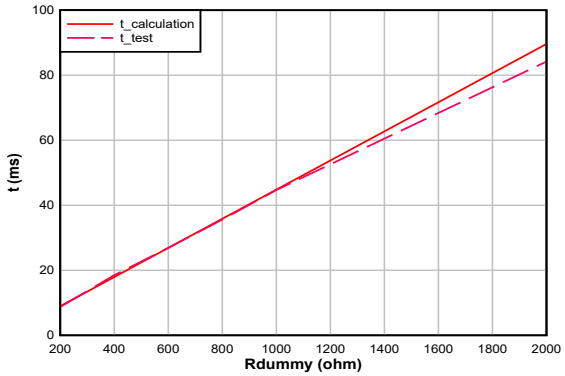

Figure 3-3. Comparison Between Calculation Discharging Time and Test Discharge Time

The maximum discharge current is calculated below. Engineer needs to make sure that this maximum current does not exceed 50 mA to avoid possible damage to internal open drain NMOS.

$$I_{DischargeMax} = V_{OUT}/R_{Dummy} \quad (4)$$

4 Experimental Results

The following is an example of proposed circuit. Figure 4-1 lists the external components. The test circuit is based on TPS61033 EVM. The output voltage is set to 5.0 V, output capacitor is 2×22 µF/0603/10 V ceramic capacitor, and the dummy resistor is set to 200 Ω.

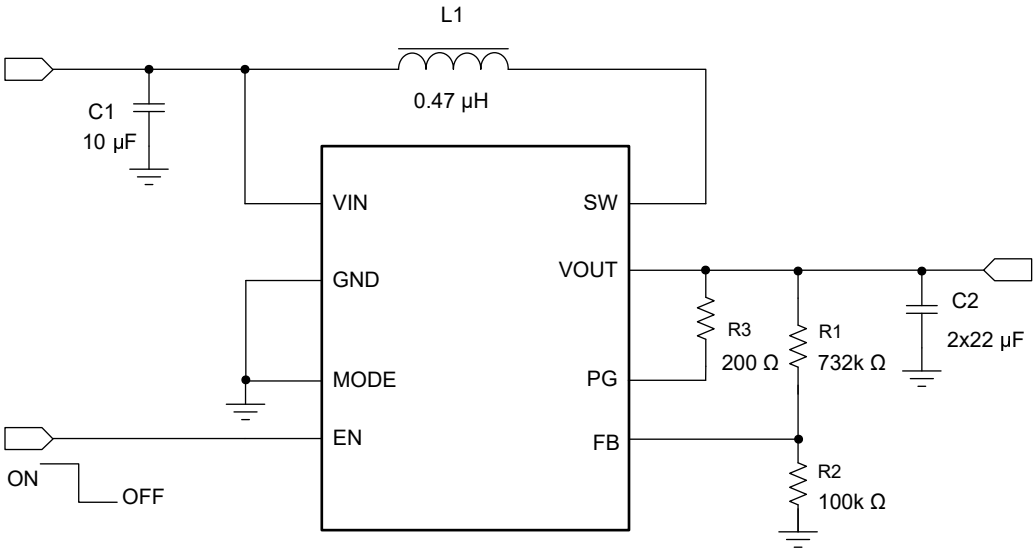

Figure 4-1. Test Circuit

Figure 4-2 shows the test results about output discharge function with the circuit above. The discharge time is about 25 ms when the output voltage is discharged to 10% nominal voltage (500 mV).

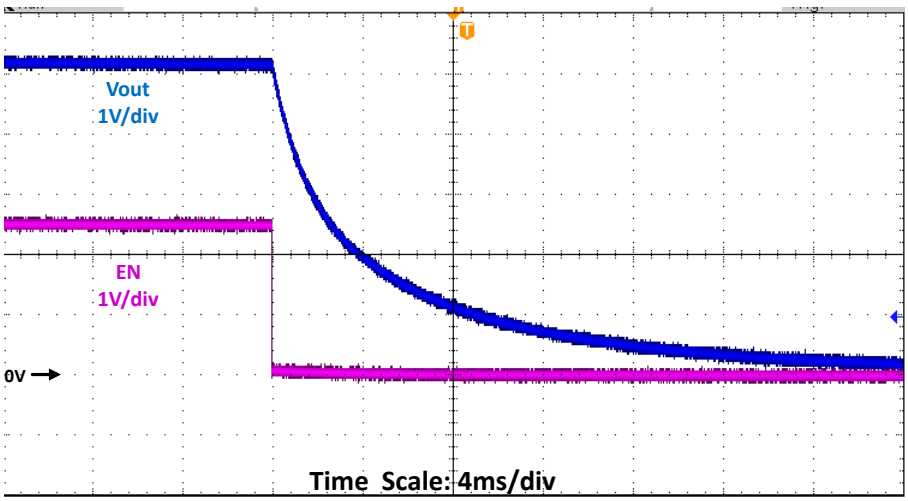

Figure 4-2. Output Discharge Function of TPS61033

5 Summary

Output discharge function is important to provide correct power sequencing, improve system reliability in unexpected power events. This application note gives a simple method to implement the output discharge function, and a way to estimate the discharge time and how to select the dummy resistor are also listed.

6 References

- Texas Instruments, *TPS61033X 5.5-V 5.5-A 2.4-MHz Fully-Integrated Synchronous Boost Converter, with Output Discharge Function*, data sheet.
- Texas Instruments, *TPS61033EVM-105 Evaluation Module*, user's guide.
- *Power Good Signal*.
- Texas Instruments, *Don’t leave it floating! Power off your outputs with quick output discharge*.

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