

DLA Approved Optimizations for QML Products



Bhavika Kagathi

Introduction

The [MIL-PRF-38535](#) is a military specification standard for hermetic and non-hermetic integrated circuits. This specification covers manufacturing general, quality, and reliability requirements for aerospace and defense applications. The goal is to establish a process flow baseline for quality and performance in these high reliability scenarios. Texas Instruments developed specifications and requirements for QML products to meet a level of quality that are defined in accordance with MIL-PRF-38535. The TI supplied and DLA agreed on optimizations for QML are listed in [Table 1](#).

QML Classes

Class N – Items which have been subjected to and passed all applicable requirements of [MIL-PRF-38535](#) including TI defined qualification testing, screening testing, and Technology Conformance Inspection and Quality Conformance Inspection (TCI/QCI), and are encapsulated in plastic (TI supplied).

Class V – Products which have been subjected to and passed all applicable requirements of [MIL-PRF-38535](#) including qualification testing, screening testing, and TCI/QCI inspections, and have been subjected to, and passed all applicable requirements of [MIL-PRF-38535](#) in [Table 1](#) (TI supplied).

Class P – A non-hermetic Plastic Encapsulated Microcircuit (PEM), which meets all applicable requirements of MIL-PRF-38535 including qualification, screening and TCI/QCI inspections, and all applicable requirements in [Table 1](#) (TI supplied).

Class Y – A microcircuit employing a non-hermetic package, which meets all applicable requirements of MIL-PRF-38535 including qualification, screening and TCI/QCI inspections, and all applicable requirements in [Table 1](#) (TI supplied).

Class Q – Items which have been subjected to and passed all applicable requirements of MIL-PRF-38535 including qualification testing, screening testing, and TCI/QCI inspections (TI supplied).

QML Optimizations

Table 1. QML Optimizations

Manufacturer	Specification	Test Optimized	Date
Texas Instruments	MIL-PRF-38535	D-8, lid torque eliminated (all cerdip, cerflat glass sealed packages all classes)	Oct-93
Texas Instruments	MIL-PRF-38535	100% burn-in eliminated (all TTL, LS, STTL products line. All package configurations.) Level B/Q only	Jun-94
Texas Instruments	MIL-PRF-38535	Constant acceleration eliminated (all products in the 8, 14, 16, 20, pin DIP) Level B/Q only	Jun-94
Texas Instruments	MIL-PRF-38535	Temperature cycles eliminated (all products in the 8, 14, 16, 20 pin DIP)	Jun-94
Texas Instruments	MIL-PRF-38535	100% high magnification inspection eliminated (TTL, LS, STTL, ALS HCMOS, F, AS, and 55 series products lines. All packages configurations) Level B/Q only	Jun-94

Table 1. QML Optimizations (continued)

Manufacturer	Specification	Test Optimized	Date
Texas Instruments	MIL-PRF-38535	100% burn-in on certain linear product eliminated (contact TI or DLA Land and Maritime for specific linear products) Level B/Q only	Sep-94
Texas Instruments	MIL-PRF-38535	Group A sample testing of alpha V10, alpha I10 and various noise tests on certain linear products eliminated (contact TI or DLA Land and Maritime for specific linear products)	Sep-94
Texas Instruments	MIL-PRF-38535	Final electrical, 25°C (ALS, AS, FAST, 54ABT32316 parent device types eliminated) Level B/Q only	Nov-95
Texas Instruments	MIL-PRF-38535	100% burn-in (HCMOS, all packages) eliminated Level B/Q only	Feb-95
Texas Instruments	MIL-PRF-38535	100% burn-in (ALS, AS, FAST) eliminated Level B/Q only	Aug-95
Texas Instruments	MIL-PRF-38535	100% temperature cycle (all CPAK) eliminated Level B/Q only	Aug-95
Texas Instruments	MIL-PRF-38535	100% constant acceleration (all CPAK) eliminated Level B/Q only	Aug-95
Texas Instruments	MIL-PRF-38535	100% -55°C screening and group A (HC and HCT) eliminated Level B/Q only	Mar-95
Texas Instruments	MIL-PRF-38535	100% -55°C screening (ABT, AC, ACT, BCT) eliminated Level B/Q only	Aug-96
Texas Instruments	MIL-PRF-38535	Burn-in reduction on 4 Meg DRAM Level B/Q only	Aug-96
Texas Instruments	MIL-PRF-38535	Physical dimensions (D1), moisture resistance (D3), insulation resistance (D3) (for all ceramic packages in Taiwan and Singapore facilities) eliminated	Oct-96
Texas Instruments	MIL-PRF-38535	Class V, P, Y Eliminated read and record data	May-00
Texas Instruments	MIL-PRF-38535	Class V X-ray (monitor only, for glass-frit seal)	May-00
Texas Instruments	MIL-PRF-38535	Class V Eliminated Non-Destructive Bond Pull	May-00
Texas Instruments	MIL-PRF-38535	Class V Eliminated PIND and Centrifuge on all flip chip mounted die	May-00
Texas Instruments	MIL-PRF-38535	100% burn-in (selected DSP/MCU) eliminated Level B/Q only	Jun-96
Texas Instruments	MIL-PRF-38535	100% -55°C screening (selected DSP/MCU) eliminated Level B/Q only	Jun-98
Texas Instruments	MIL-PRF-38535	100% X-ray eliminated on welded lid parts	Oct-07
Texas Instruments	MIL-PRF-38535	QCI Group B Subgroup 1 Class V Physical Dimensions and Internal Water Vapor Performed as part of Generic Group D QCI by package family within 36 week window	Aug-00
Texas Instruments	MIL-PRF-38535	QCI Group B Subgroup 2 Class V Resistance to Solvents, Bond Strength and Die shear are done as part of Generic group B QCI by package family by week of seal. Main body 38535 group B. Internal visual and mechanical is covered by 100% pre-cap inspection.	Aug-00

Table 1. QML Optimizations (continued)

Manufacturer	Specification	Test Optimized	Date
Texas Instruments	MIL-PRF-38535	QCI Group B Subgroup 3 Class V Solder-ability performed as part of Generic Group B QCI by package family per week of seal.	Aug-00
Texas Instruments	MIL-PRF-38535	QCI Group B Subgroup 4 Class V Lead Integrity, Seal are performed as part of generic group D CQI by package family within 36-week window. Lid torque testing eliminated for all package families	Aug-00
Texas Instruments	MIL-PRF-38535	QCI Group B Subgroup 5 Class V End point electrical, Steady State Life and End point electrical performed as part of Wafer Lot acceptance by wafer lot	Aug-00
Texas Instruments	MIL-PRF-38535	QCI Group B Subgroup 6 Class V End-point electrical, temp cycle, constant acceleration, seal and endpoint electrical parameters performed as part of generic Group D QCI by package family within 36 week window	Aug-00
Legacy (National Semiconductor)	MIL-PRF-38535	DS16F95 DS26F31 and 32 DS96F172 through 175 Level S/V only Minimum percentage of the metallization cross sectional area required over the passivation steps in Method 2018, SEM Inspection, reduced from 50% to 30% for Method 5007, Wafer Lot Acceptance	Jun-97
Legacy (National Semiconductor)	MIL-PRF-38535	All part numbers for Level S/V only Method 5007, parts a. and c., Thermal Stability test (C-V plot) reduced from each wafer lot to pre-designated maintenance events of the sputter metal deposition system (for example, venting, and so on.)	Oct-99
Legacy (National Semiconductor)	MIL-PRF-38535	Metal can packages (TO-3, 5, 39, 46) Level B/Q only M2001, Constant Acceleration eliminated for screen	Jun-96
Legacy (National Semiconductor)	MIL-PRF-38535	Specific part numbers for Level S/V only Ultrasonic inspection per Method 2030 is being performed instead of Radiography on ceramic package with a copper-tungsten heat slug	Nov-06
Legacy (National Semiconductor)	MIL-PRF-38535	DS26LS31 for Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Jul-00
Legacy (National Semiconductor)	MIL-PRF-38535	LM124 LM139 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Aug-00 Jan-01
Legacy (National Semiconductor)	MIL-PRF-38535	LM124, LM124A Level B/Q only Screen for A-2, A-3 final electricals moved prior to burn-in	Oct-02

Table 1. QML Optimizations (continued)

Manufacturer	Specification	Test Optimized	Date
Legacy (National Semiconductor)	MIL-PRF-38535	JL111, LM111 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Jun-02
Legacy (National Semiconductor)	MIL-PRF-38535	LM158 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Nov-02
Legacy (National Semiconductor)	MIL-PRF-38535	DS96F173 and 175 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Aug-02
Legacy (National Semiconductor)	MIL-PRF-38535	JL148, LM148 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Nov-02
Legacy (National Semiconductor)	MIL-PRF-38535	LM139, LM139A Level B/Q only Screen for A-2, A-3 final electricals moved prior to burn-in	Jan-03
Legacy (National Semiconductor)	MIL-PRF-38535	LM741 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Jun-03
Legacy (National Semiconductor)	MIL-PRF-38535	LM136A Level B/Q only Screen for A-2, A-3 final electricals moved prior to burn-in LM136 Screen for 25°C, -55°C, +125°C and temperature coefficient testing can be performed prior to burn-in. LM148 Screen for -55°C, 125°C moved prior to burn-in	Oct-05 May-06 Jun-06
Legacy (National Semiconductor)	MIL-PRF-38535	LM723 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Nov-03
Legacy (National Semiconductor)	MIL-PRF-38535	DS26LS31 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	Dec-05

Table 1. QML Optimizations (continued)

Manufacturer	Specification	Test Optimized	Date
Legacy (National Semiconductor)	MIL-PRF-38535	LM117, JL117 LM119 Level B/Q only Burn-in reduced from inspection lot screen to fab lot sample. Life test frequency increased from yearly to quarterly and can use non-burned-in parts.	May-08
Texas Instruments	MIL-PRF-38535	TI systems do not support Marking as described in Section 3.1 (p.13-14): Marking for plastic packages. Follow TI Standard Marking/Symbolization. Actual product symbolization can be documented in the SMD.	Aug-23
Texas Instruments	MIL-PRF-38535 Table IA: Screening procedure (p. 20)	Allow 1X Reflow in lieu of temp cycle in Table IA.TM1010, Condition B, -55/125C, 15cy – nonstandard flow. When TC is performed, it can be in accordance with JESD22-A104.	Aug-23
Texas Instruments	MIL-PRF-38535 Table V: Group D (p 37-43) D3 / TM1010	Perform TC with accordance to JESD22- A104 to align with Appendix H and standard factory specifications.	Aug-23
Texas Instruments	MIL-PRF-38535 Table V: Group D (p 37-43) D3 / Clarification	Clarification: Perform UHAST per one of the following conditions: 130C, 85%RH – 96 Hours 110C, 85%RH – 264 Hours. Allowed per Note 18. TI can perform UHAST, not BHAST for QCI. Allowed per MIL-PRF-38535.	Aug-23
Texas Instruments	MIL-PRF-38535 Table V: Group D (p 37-43) D3 / Clarification	Clarification: TI can use separate units for UHAST and TC. Allowed option per Note 17.	Aug-23
Texas Instruments	MIL-PRF-38535 Table V: Group D (p 37-43) D3 / Moisture resistance condition	Moisture resistance per JESD22-A118 Unbiased HAST condition A or B.	Aug-23
Texas Instruments	MIL-PRF-38535 Table V: Group D (p 37-43) D7 / Adhesion of lead finish	TI uses internal procedure (QSS 009- 109).	Aug-23
Texas Instruments	MIL-PRF-38535 Table A-III (p 80) Coating Thickness	Clarified NiPdAu thickness. TI devices meet NiPdAu thickness indicated below. Over plating thickness (micronch/micrometer): Min 20/0.51 Max NS	Aug-23
Texas Instruments	MIL-PRF-38535 Table H-I. Assembly process technology testing for flip chip packages containing Pb free bump [p196]	Flip Chip containing PB free bumps: Biased Humidity option to run JESD22- A101 (THB) or A110 (Biased HAST) Conditions: <ul style="list-style-type: none"> • 85C/ 85% relative humidity, 1000 hours or • 130C/85% relative Humidity, 96 hours, or • 110C/85% relative humidity, 264 hours Thermal Shock is not applicable to organic substrates.	Aug-23

Table 1. QML Optimizations (continued)

Manufacturer	Specification	Test Optimized	Date
Texas Instruments	MIL-PRF-38535 Table H-IA. Assembly process technology testing for hermetic (classes Q, V) and non-hermetic packages (class Y). [197-198]	Class Q, V, Y (flip chip): Final Package testing High temperature Storage TM 1008 (1,000 hours at +150°C) or JESD 22 A103 (1,000 hours at +150°C or equivalent).	Aug-23
Texas Instruments	MIL-PRF-38535 Table H-IIA. Technology characterization testing for hermetic (classes Q, V) and non-hermetic packages (class Y) [200-202]	Class Q, V, Y (flip chip): Group 2: a. Thermal shocks N/A b. Temperature cycles TM 1010, condition C, 100 cycles or JESD22-A104 c. HAST(Biased) JESD22-A110 or THB JESD22-A101 d. Visual inspection TM 1010 and TM 1004 visual criteria e. Not applicable	Aug-23
Texas Instruments	MIL-PRF-38535 Table H-IB. Assembly process technology testing for plastic packages (classes N, P)	Class N, P: Group #3 Temperature Cycling per one of the following: - 55/125C, 700 cycle (product release), 1000 cycle (technology release) or 65/150C, 500 cycle (product release), 1000 cycle (technology release). Group #5 High Temp Storage performed per JESD 22 A103 Bake 150C, 1000 Hours or equivalent.	Aug-23
Texas Instruments	MIL-PRF-38535 Table H-IIB. Technology characterization testing for plastic packages (classes N, P)	Class N, P: Group#2 Moisture sensitivity level per manufacturer's specification or JEDEC JSTD- 020/ JESD 22-A113 Group #3 b. Biased HAST (130C/85%RH/96, 192hr) or (110C/85% RH/264, 528hr) or (85C/85%RH/1000, 2000hr) per JESD22-A110/JESD22-A101 Group #6 Lead Integrity - For plastic packages, TI uses internal test method, QSS 009-134. TM is not applicable for plastic packages. For trim and form leaded packages this is N/A per Test Method 2004 section 3.2 Group #7 - Can perform MSL testing per J-STD-020/JESD 22-A113 instead of this test. Group #9 - Does not perform Fungus testing. Group #12 – Thermal characteristics based on Modeling.	Aug-23
Texas Instruments	MIL-STD-883 TM5007	Alternate method of inline measurements can be used in lieu of cross section (applies to planar technologies only).	Dec 23

Trademarks

All trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated