Radiation Report

LMK04832-SP Single-Event Effects Report

ABSTRACT

The LMK04832-SP (5962R1723701VXC) was tested under heavy ions and monitored for various Single-Event Effects (SEE). Testing was performed under five different operating conditions to ensure all areas of the part were tested. No incidences of Single-Event Latchup (SEL) and Single-Event Function (SEFI) were detected up to 121 MeV-cm^2/mg, the highest effective linear energy transfer (LETeff) tested. SEL testing was performed at the highest operating voltage (3.45 V) and temperature (125°C). Single-Event Upsets (SEU) were detected, with most lasting one clock cycle or less. The longest SEU detected lasted 22 clock cycles and the longest outage time for an event was under 0.4 µs. The SEU Figure of Merit (FOM) for the most sensitive operating condition was 4.7×10^{-4} events per day. The worst case event rate predicted for a GEO orbit using the "worst week" solar activity was 9.5×10^{-2} events per day.

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Trademarks

1 Product Description

The LMK04832-SP[1] is a radiation hardened version of Texas Instruments' commercial grade LMK04832, JESD204B compliant clock jitter cleaner with a dual loop. LMK04832-SP is the generic part number (GPN) for the product. The flight grade orderable part number is 5962R1723701VXC[2]. A prototype, which does not receive full space grade processing and testing, LMK04832W/EM, can be ordered for engineering evaluation.

A simplified block diagram of the LMK04832-SP is shown in Figure 1-1, and a more detailed block diagram is shown in Figure 1-2. The LMK04832-SP can provide very low jitter clocking signals up to 3.2 GHz on 14 individually programmable outputs. It can be configured for operation in dual PLL, single PLL, or clock distribution modes with or without SYSREF generation or reclocking. PLL2 may operate with either internal or external VCOs[1].

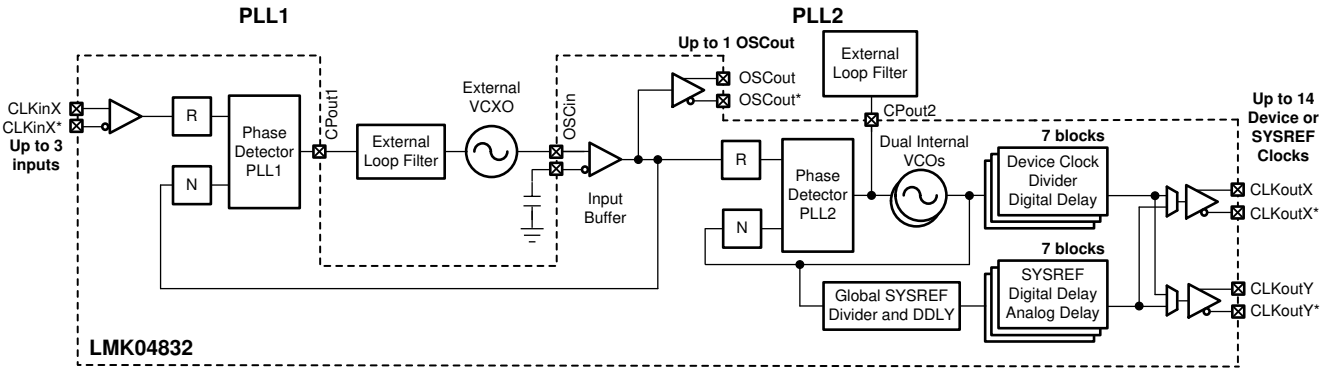

Figure 1-1. LMK04832-SP Configured in Dual Loop Mode

The 14 clock outputs from PLL2 can be configured to drive seven JESD204B compliant data converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. JESD204B is a serial interface standard used between data converters and logic devices with serial data rates up to 12.5 Gbps[3]. SYSREF is a timing phase reference synchronous with the output signal.

Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high performance outputs for traditional clocking systems. The outputs of the LMK04832-SP can be individually configured in many different output formats: CML, LVPECL, LCPECL, HSDS, LVDS, or 2xLVCMOS. The output frequency and delay can be individually set for each output. The product pinout is shown in Figure 1-3.

The part is configured through a serial peripheral interface (SPI) and the configuration is stored in registers. The state of the registers can be accessed through a register read. The operating voltage of the LMK04832-SP is 3.15 to 3.45 V.

The LMK04832-SP is manufactured on a TI BiCMOS process with SiGe NPN bipolar transistors.

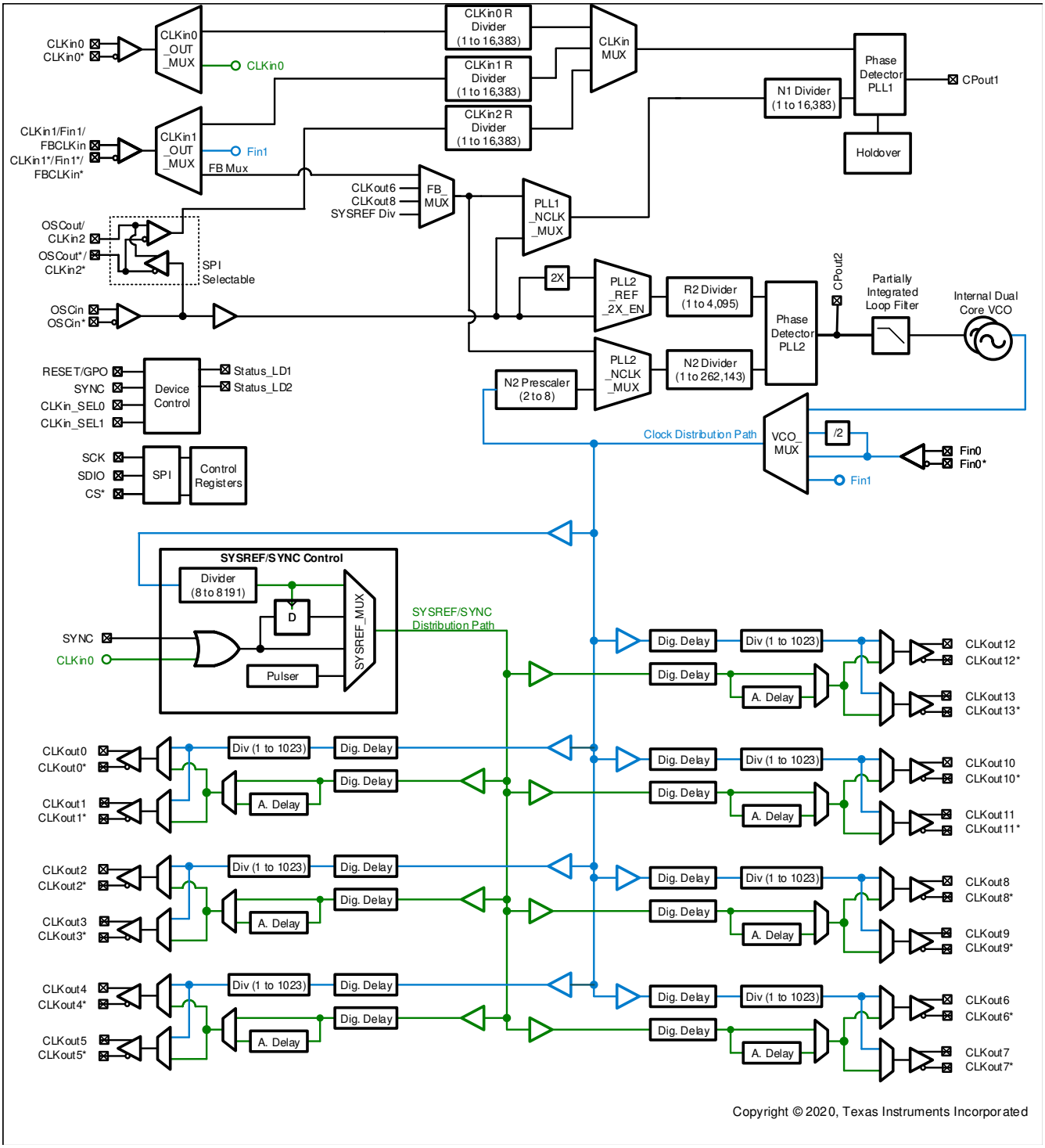

Figure 1-2. LMK04832-SP Detailed Block Diagram

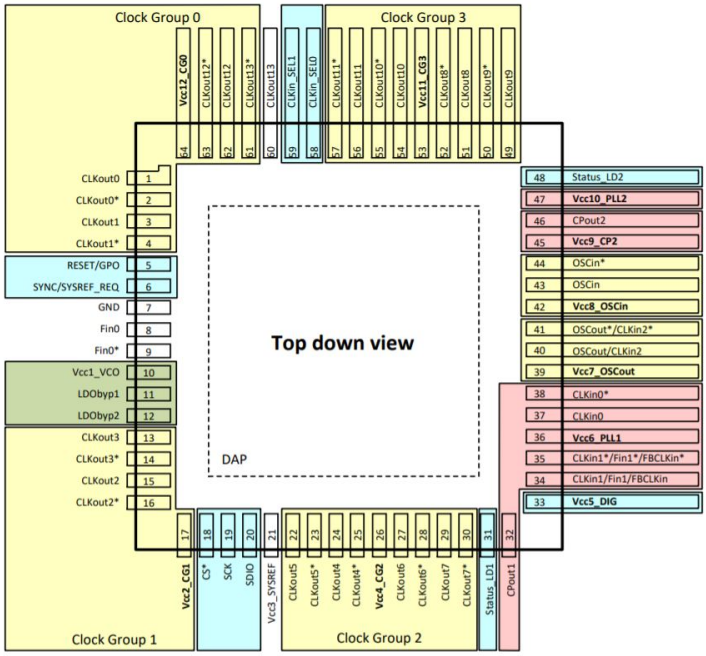

Figure 1-3. LMK04832-SP Pinout

2 Test Setup

The LMK04832-SP was monitored for Single-Event Latchup (SEL), Single-Event Functional Interrupt (SEFI) and Single-Event Upset (SEU).

The device under test (DUT) was soldered to a custom evaluation board similar to the LMK04832EVM-CVAL evaluation board (Figure 2-1)[4]. The metal lid was removed from the DUT to expose the die surface to the ion beam. The active components on the board were bypassed and the power and input signals to the DUT were supplied externally. Figure 2-2 shows a block diagram of the test setup.

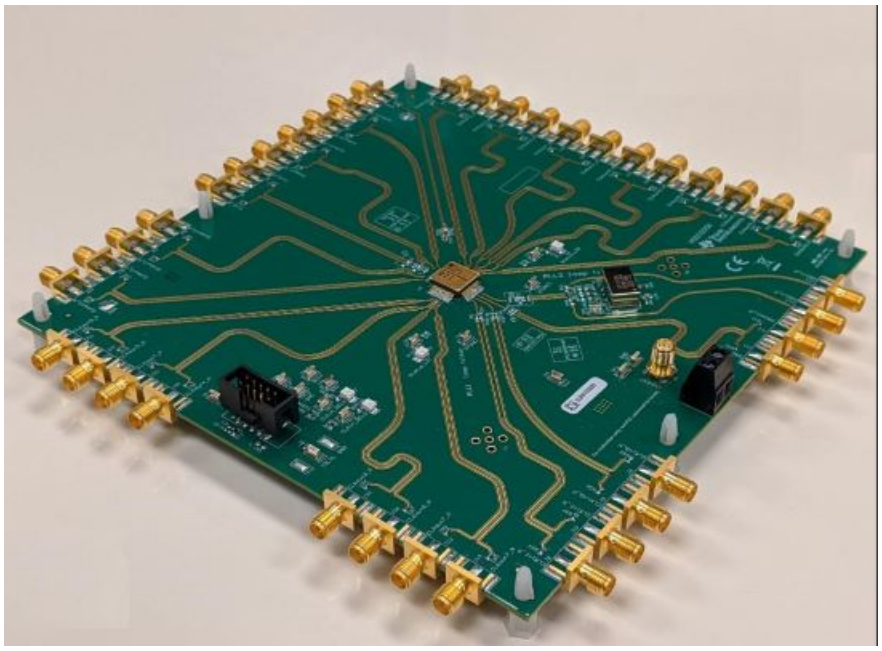

Figure 2-1. LMK04832EVM-CVAL Evaluation Board

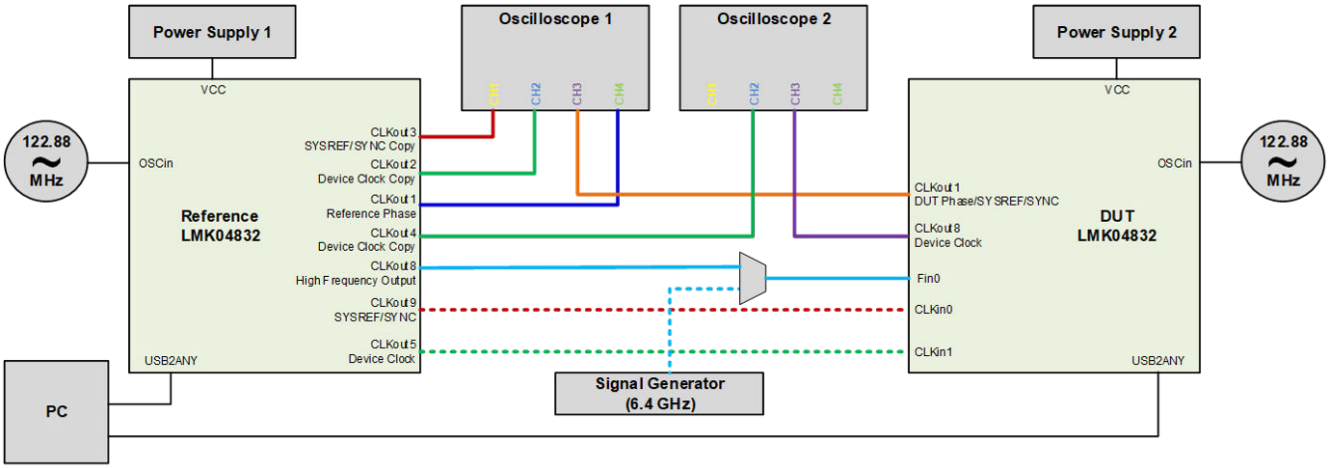

Figure 2-2. Block Diagram of Test Setup

Power to the DUT board was supplied by an Agile 6702 quad supply. The 6702 was controlled and the output current to the DUT board was monitored by an NI-PXIe-8135 controller using a custom Lab View® GUI (PXI Rad Test) developed by Texas Instruments for SEE testing. The voltage was set to 3.45 V as measured at the DUT board. The supply current was monitored on every ion run.

The input signal to the DUT was supplied by a second, “reference” LMK04832EVM-CVAL as shown in Figure 2-2. The registers of the DUT and reference were written and read back using Texas Instruments’ USB2ANY PC interface and TICS PRO software[4].

CLKout8 output was monitored with the output in LVDS mode with a Tektronix DPO7354 oscilloscope.

To ensure all circuits of the DUT were tested, the DUT was tested under 5 different operating modes, exercising the different inputs, PLLs, VCOs and signal paths through the part. The conditions of each operating mode are shown in Table 2-1.

Table 2-1. DUT Configuration

Functional Mode	Dual Loop	Dual Loop Nested 0-Delay	Single Loop 0-Delay	Distribution	Dual Loop, Holdover
SYSREF Enabled	No	Yes	Yes	Yes	Yes
Feedback MUX	No	SYSREF -> PLL1 N Divider	CLKout8 -> PLL2 N Divider	No	No
Holdover	No	No	No	No	Yes
Input	CLKin1	CLKin0	CLKin1	Fin0	CLKin1
Input Freq (MHz)	122.88	1.024	122.88	3200	122.88
PLL1 Enabled	Yes	Yes	No	No	Yes
PLL1 R and N Divider	120	1	N/A	N/A	120
External VCXO Freq (MHz)	122.88	122.88	N/A	N/A	122.88
PLL2 Enabled	Yes	Yes	Yes	No	Yes
PLL2 R Divider	1	1	4	N/A	1
PLL2 N Divider	13	12	4	N/A	10
PLL2 N Cal Divider	N/A	12	48	N/A	N/A
PLL2 N Prescaler	2	2	2	N/A	2
VCO Freq (MHz)	3194.88	2949.12	2949.12	N/A	2457.6
Output CLK Divider	24	24	24	24	20
Output Freq (MHz)	133.12	122.88	122.88	66.66	122.88
Test	SEL, SEU	SEFI, SEU	SEL, SEFI, SEU	SEL, SEFI, SEU	SEL, SEFI

2.1 SEL Test

A thermistor was attached to the DUT board up against the DUT to monitor the temperature. The DUT was heated with a heat gun so that the thermistor read at least 125°C. Based on the power dissipation of the DUT and the thermal modeling of the ceramic package, the junction temperature will be approximately 20°C higher than the thermistor reading.

The supply current was monitored on a display in real time and also recorded by the PXI controller.

2.2 SEFI Test

SEFI was tested in two ways:

1. At least one output of the device was monitored during each ion run. If the function of the DUT changed permanently and the registers had to be rewritten, this would be considered a SEFI.
2. On some ion runs, the registers read before and after the ion run and the results were compared using the Beyond Compare software. If any programmable register bit changed at the end of the ion run, this would also be considered a SEFI.

2.3 SEU Test

Output CLKout8 was configured in LVDS mode and the CLKout8* pin was monitored with the oscilloscope. The scope trigger was set on “width” mode so that if the falling edge of the output clock was outside the expected time window, an error would be counted and the clock output would be captured.

After a few ion runs, the scope window range and trigger location would be adjusted to ensure the whole length of the event would be captured in the scope capture window.

2.4 Test Facility

Heavy ion irradiation was done using the 15-A MeV cocktail and K500 beam line at the Texas A&M University Cyclotron Institute Radiation Effects Facility (TAMU)[5]. The SEL and SEFI testing were performed on May 12 - 13, 2020. SEU testing was done on June 1 - 2, 2020. During the SEU testing, monitoring continued for SEL and SEFI. Figure 2-3 shows the DUT board situated in front of the heavy ion beam export window and the hot air gun.

Testing was done with several different ions with different linear energy transfers (LETs) Incident angles were used to increase the effective LET (LETeff) on some ion runs as shown in Table 2-2. The highest LETeff used was 121 MeV-cm^2/mg for SEL and SEFI testing.

Table 2-2. Ions and Incident Angles

Ion	LET	Incident Angle	LETeff
	(MeV-cm^2/mg)	(Degree)	(MeV-cm^2/mg)
Ne	2.8		
Ar	8.7		
Cu	29.5		
Ag	48	45	70
Au	88	40	121

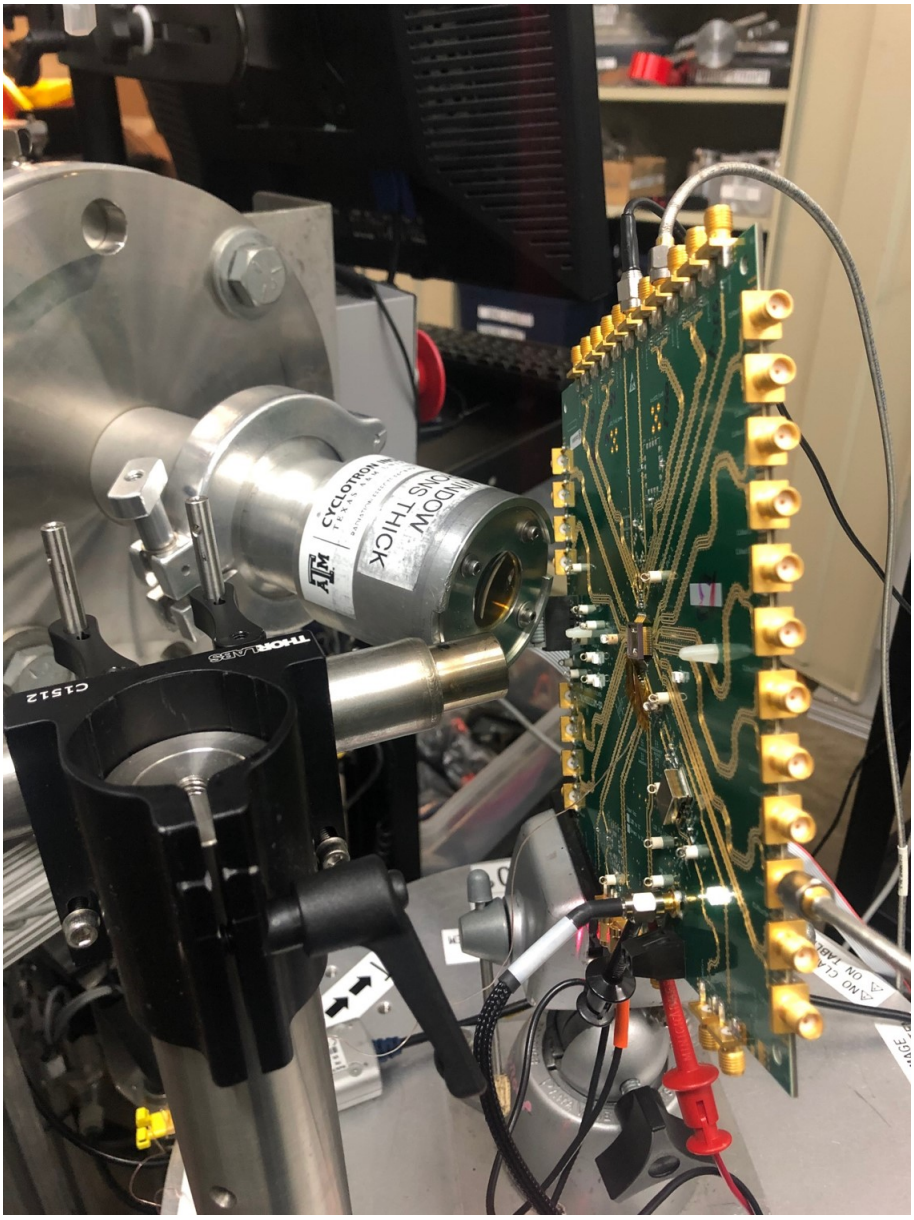

Figure 2-3. DUT Board Set Up with Heat Gun for SEL Testing at TAMU. The Board is Positioned So the DUT Will Have a 44° Incident Angle to the Ion Beam.

3 Results

3.1 SEL Results

No incidences of SEL were detected on any ion runs. The supply current had some fluctuations due to ion strikes but did not change by more than 0.4%. Any momentary increase in current was less than 1 mA. Occasionally the supply current would drop by up to 4 mA but would recover within microseconds. Supply current from three ions runs at 121 MeV-cm/mg with the DUT board heated to 125°C or higher are plotted in Figure 3-1 to Figure 3-3.

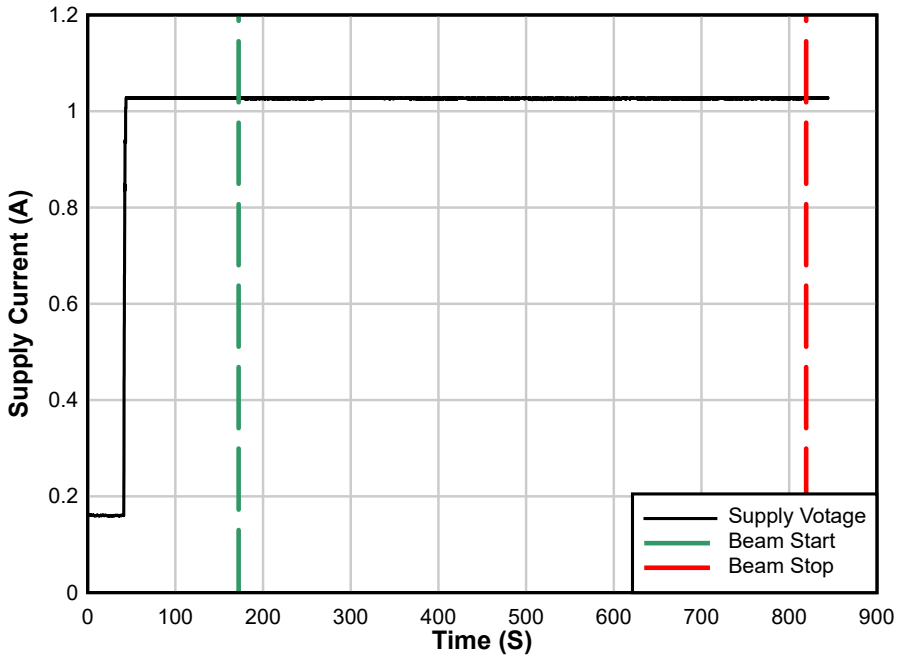

Figure 3-1. Supply Current for Ion Run #1 with DUT in Dual Loop Mode, LETeff at 121 MeV-cm^2/mg and DUT Board Thermister Reading of 133°C

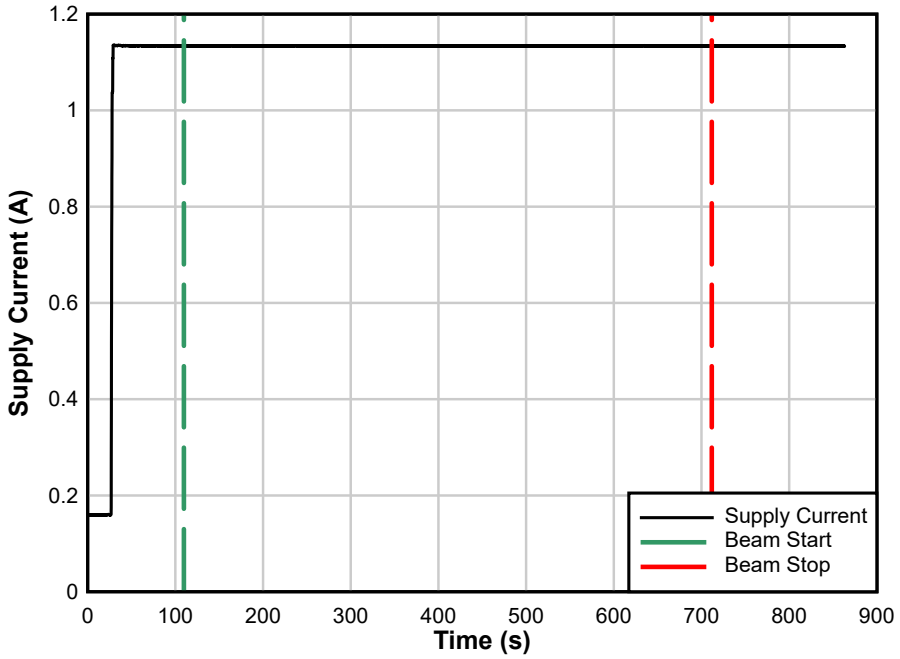

Figure 3-2. Supply Current for Ion Run #2 with DUT in Dual Loop, Holdover Mode, LETeff at 121 MeV-cm^2/mg and DUT Board Thermister Reading of 126°C

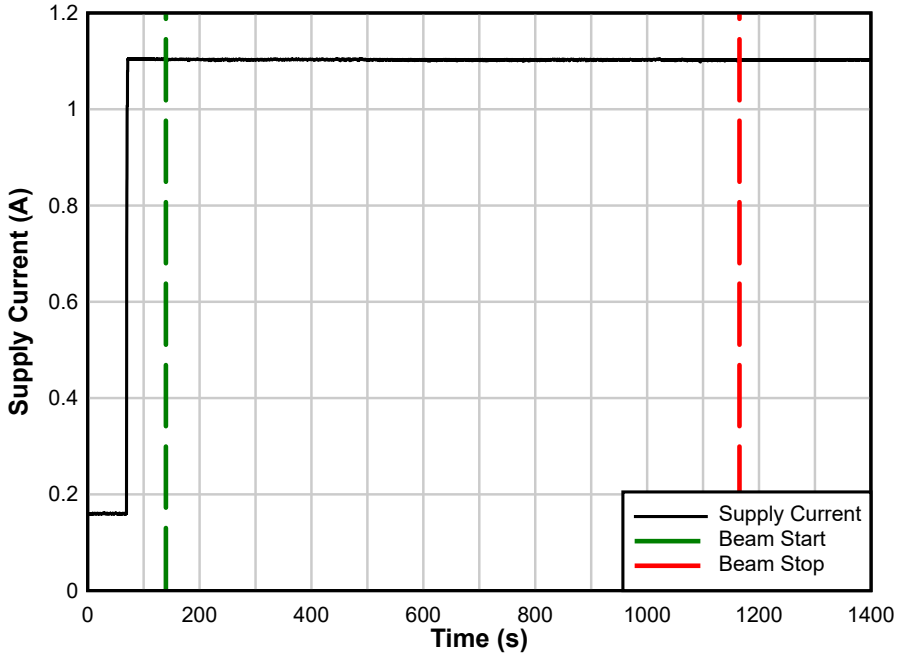

Figure 3-3. Supply Current for Ion Run #3 with DUT in Single Loop, 0-Delay Mode, LETeff at 121 MeV-cm^2/mg and DUT Board Thermister Reading of 125°C

3.2 SEFI Results

No incidences of SEFIs were seen on any ion run. During an ion run, the output of the DUT could be momentarily upset, but the output always returned to the frequency programmed into the DUT. The DUT operated properly after each ion run and the registers did not need to be rewritten.

On the ion runs with LETeff = 121 MeV-cm^2/mg, the registers were read before and after the ion run. The register readings were compared using Beyond Compare software (Figure 3-4). No changes were seen in any of the programmable registers. On some ion runs, status registers R387, R388 and R389 did change. The change in register R387 indicated that PLL2 went through a relock during the ion run. The changes in registers R388 and R389 indicated that the Vtune DACs changed settings to keep Vtune within the specified value.

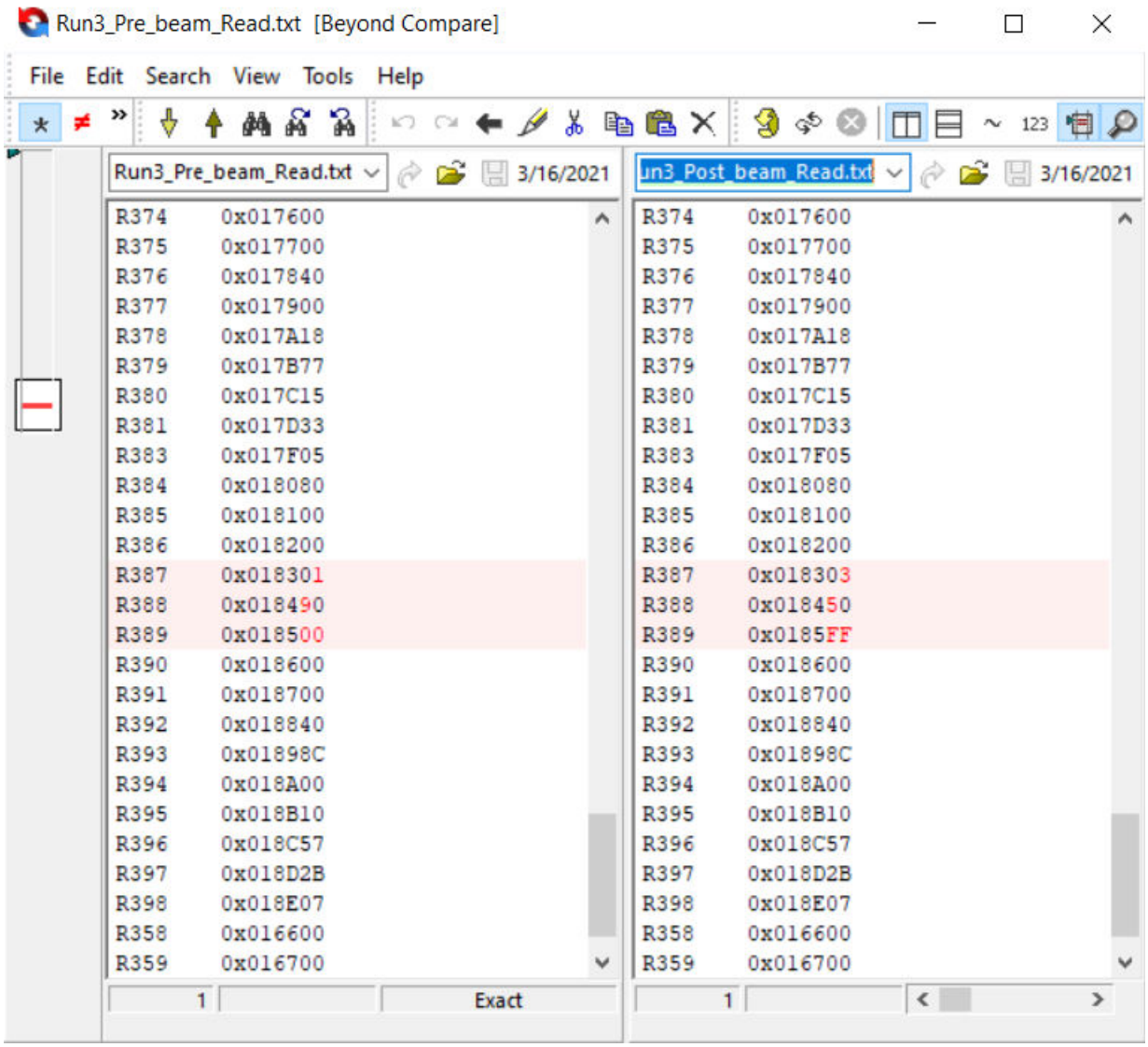

Figure 3-4. Screen Capture of Beyond Compare Comparing Registers Pre and Post Ion Run #3

3.3 SEU Results

Two SEU signatures of the clock output were seen, one where the event lasted one clock cycle or less (Figure 3-5) and the other where the event lasted several clock cycles (Figure 3-6). After an event, the output would always return to the programmed output frequency but sometimes would be out of phase with the frequency prior to the event. The longest events lasted 22 clock cycles. Approximately 33% of the SEUs lasted longer than one clock cycle. Figure 3-7 to Figure 3-10 show histograms of the length of the events in clock cycles for select ion runs with different opearting modes and LETs. Table 3-1 through Table 3-4 list the number of events detected at each LETeff for each of the four operating modes used for SEU testing and the percentage of events that were longer than one clock cycle. As can be seen from the histograms and tables, the number of clock cycles an event lasted does not appear to have much dependence upon the operating mode, output frequency or ion energy.

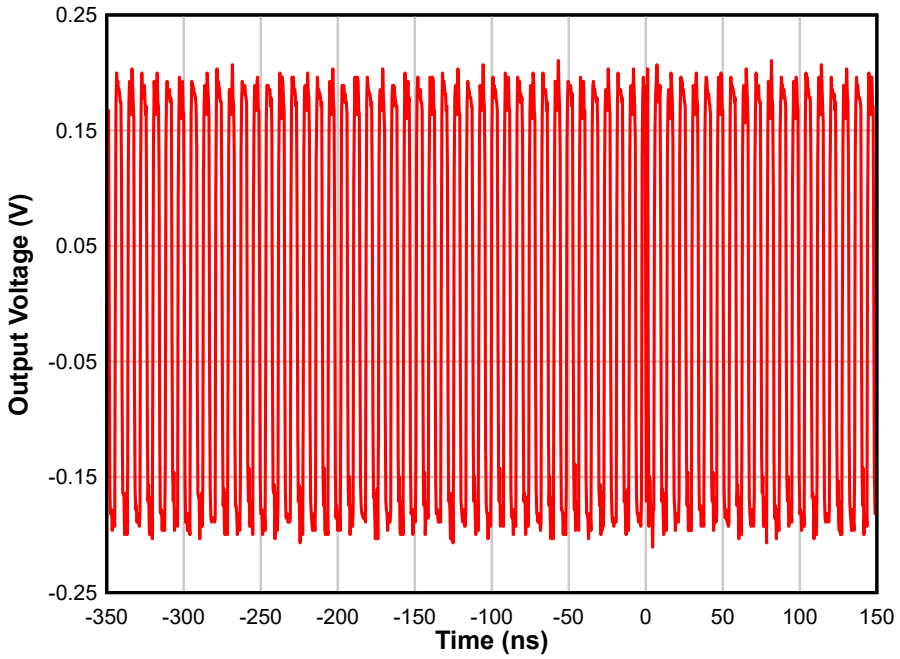

Figure 3-5. Example of an SEU That Lasted 1 Clock Cycle From Ion Run #36, with an LETeff of 70 MeV-cm^2/mg and the DUT in Dual Loop Mode

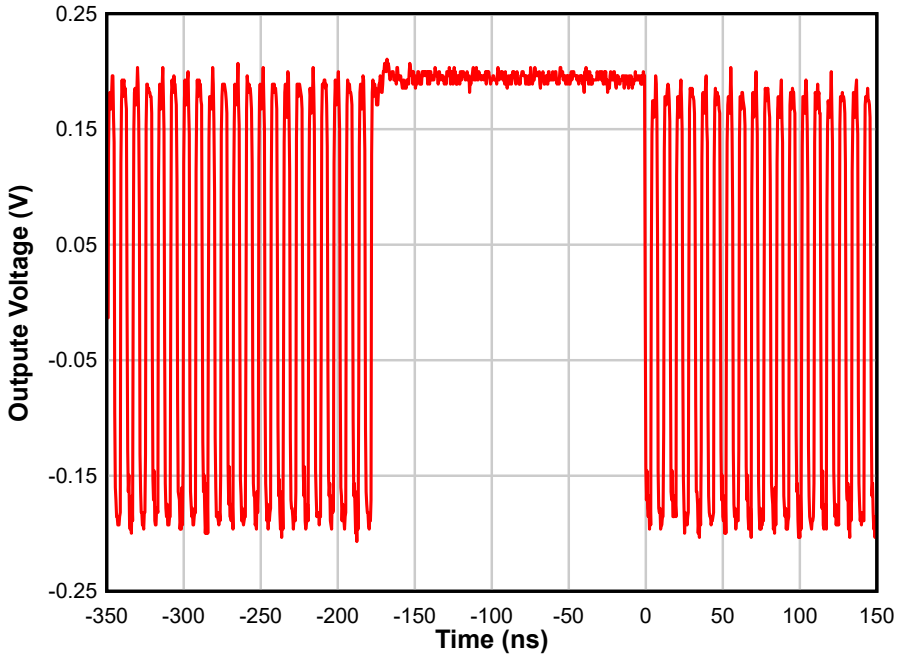

Figure 3-6. Example of an SEU that Lasted Multiple Clock Cycles From Ion Run #36, with an LETeff of 70 MeV-cm^2/mg and the DUT in Dual Loop Mode

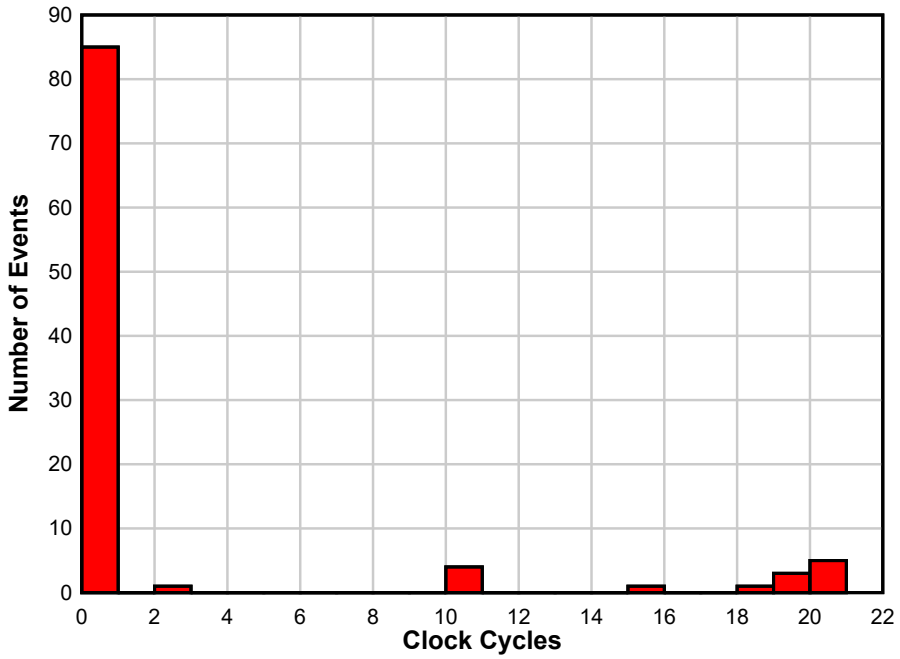

Figure 3-7. Histogram of the Length of Events in Clock Cycles for Ion Run #18 at an LETeff of 8.7 MeV-cm^2/mg and the DUT in Distribution Mode. There Were a Total of 100 Events in This Ion Run.

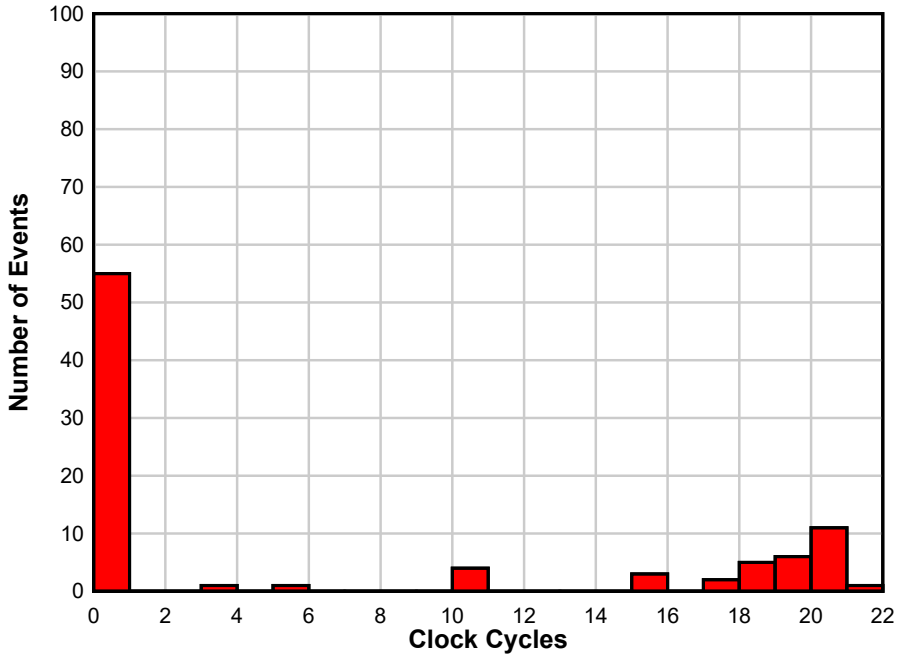

Figure 3-8. Histogram of the Length of Events in Clock Cycles for Ion Run #27 at an LETeff of 29.5 MeV-cm^2/mg and the DUT in Dual Loop, Nested, 0-Delay Mode. There Were a Total of 89 Events in this Ion Run.

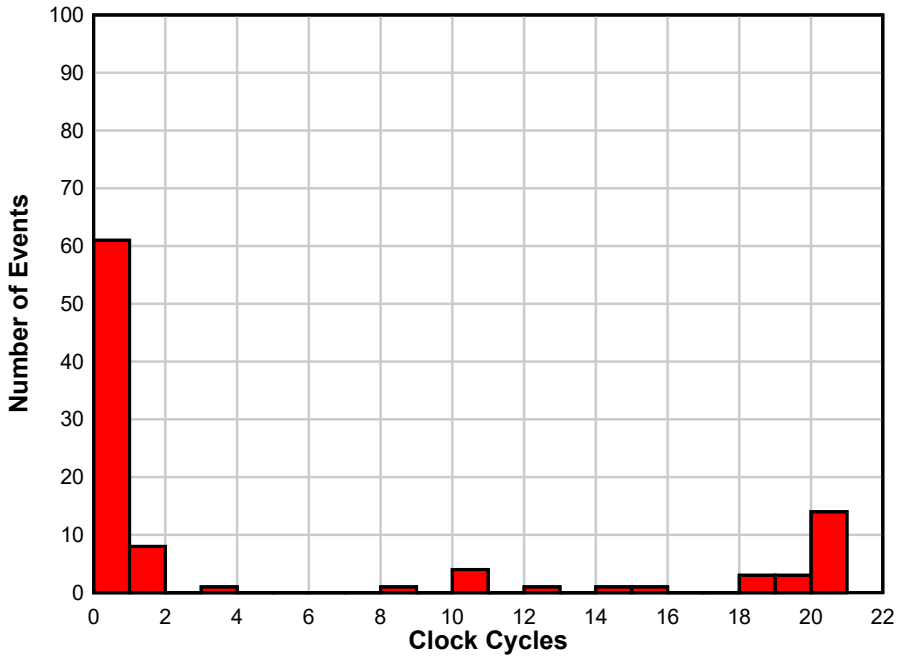

Figure 3-9. Histogram of the Length of Events in Clock Cycles for Ion Run #28 at an LETeff of 48 MeV-cm^2/mg and the DUT in Single Loop 0-Delay Mode. There Were a Total of 98 Events in This Ion Run.

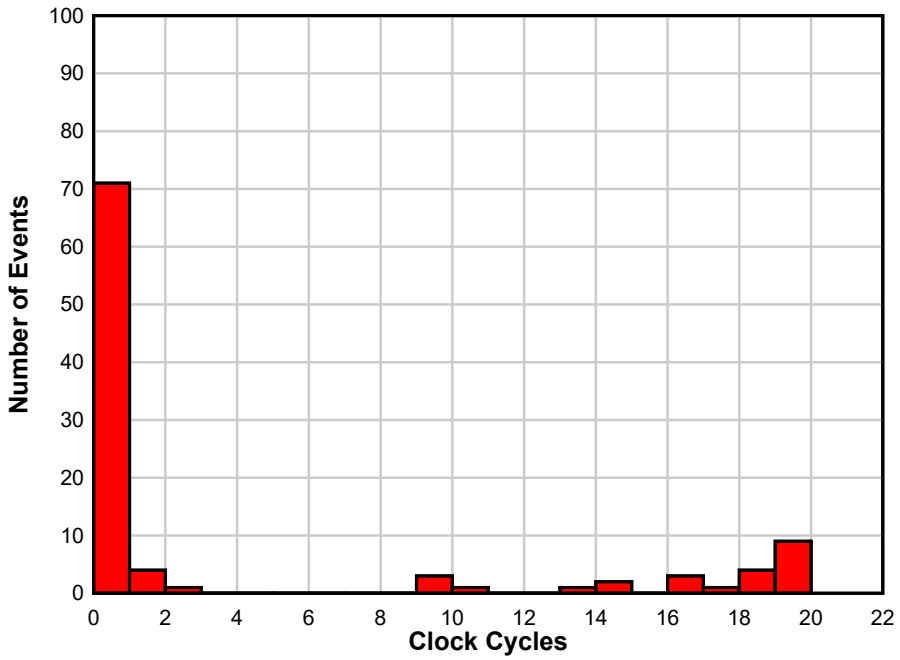

Figure 3-10. Histogram of the Length of Events in Clock Cycles for Ion Run #34 at an LETeff of 70 MeV-cm^2/mg and the DUT in Dual Loop Mode. There Were a Total of 100 Events in This Ion Run.

The outage time or length of time it took for the output to recover from a multi-clock cycle event was dependent upon the output frequency. The longest event detected lasted 22 clock cycles and was seen each of the different operating modes. The Distribution mode had the lowest output frequency at 66.66 MHz and would take the longest to recover. An event lasting 22 clock cycles would take 0.33 µs for the output to recover. For the Dual Loop mode, with an output frequency of 133.12 MHz, an event lasting 22 clock cycles would only take 0.16 µs for the output to recover.

Table 3-1. Dual Loop Mode SEU Test Results

LETeff	Fluence	Events		Cross Section
(MeV-cm^2/mg)	(ions/cm^2)	Total	> 1 Clock Cycle	(cm^2)
2.8	1.00×10^7	51	33%	5.1×10^{-6}
8.7	5.50×10^6	104	32%	1.9×10^{-5}
29.5	3.57×10^6	100	34%	2.8×10^{-5}
48	2.36×10^6	104	28%	4.4×10^{-5}
70	1.23×10^6	105	29%	8.5×10^{-5}

Table 3-2. Dual Loop Nested 0-Delay Mode SEU Test Results

LETeff	Fluence	Events		Cross Section
(MeV-cm^2/mg)	(ions/cm^2)	Total	> 1 Clock Cycle	(cm^2)
2.8	1.00×10^7	51	33%	5.1×10^{-6}
8.7	6.03×10^6	108	43%	1.8×10^{-5}
29.5	3.70×10^6	89	38%	2.4×10^{-5}
48	2.69×10^6	102	31%	3.8×10^{-5}
70	1.39×10^6	103	25%	7.4×10^{-5}

Table 3-3. Single Loop 0-Delay Mode SEU Test Results

LETeff	Fluence	Events		Cross Section
(MeV-cm^2/mg)	(ions/cm^2)	Total	> 1 Clock Cycle	(cm^2)
2.8	1.00×10^7	49	31%	4.9×10^{-6}
8.7	6.01×10^6	100	34%	1.7×10^{-5}
29.5	2.37×10^6	66	36%	2.8×10^{-5}
48	2.03×10^6	98	38%	4.8×10^{-5}
70	2.53×10^6	167	38%	6.6×10^{-5}

Table 3-4. Distribution Mode SEU Test Results

LETeff	Fluence	Events		Cross Section
(MeV-cm^2/mg)	(ions/cm^2)	Total	> 1 Clock Cycle	(cm^2)
2.8	1.00×10^7	47	15%	4.7×10^{-06}
8.7	2.10×10^6	100	17%	4.8×10^{-5}
29.5	9.45×10^5	100	44%	1.1×10^{-4}
48	6.77×10^5	115	32%	1.7×10^{-4}
70	4.86×10^5	108	37%	2.2×10^{-4}

Figure 3-11 through Figure 3-14 are plots of the SEU cross sections vs. LET for the four different operating modes used during SEU testing. Two sigma error bars, representing a confidence level of approximately 95%[6], are plotted around each data point. A Weibull plot has been fitted to the data in Equation 1 [7] with the fit parameters listed in Table 3-5. Events were seen at the lowest LET tested (2.8 MeV-cm^2/mg) and 1 MeV-cm^2/mg was used for the threshold LET. The cross sections at the highest LETeff tested (70 MeV-cm^2/mg) were used for the limiting cross sections.

$$F(L) = A\left(1 - exp\left\{-\left[\frac{L-L_0}{W}\right]^S\right\}\right); L > L_0$$

where, ***F(L)*** is the event cross-section for a particular LET
A is the limiting cross-section
W is the width of the distribution
L_0 is the threshold LET
S is the shape parameter

(1)

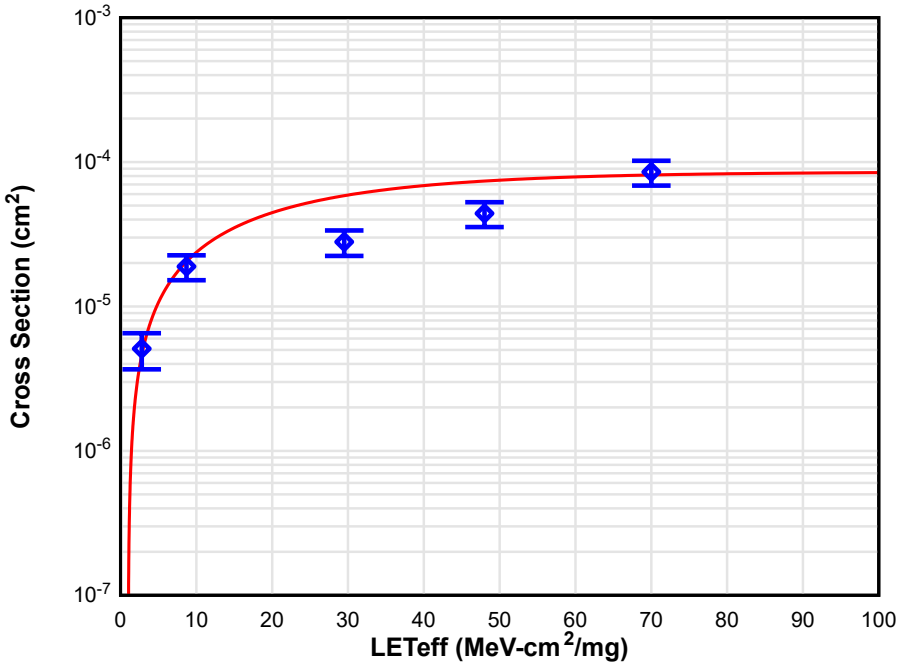

Figure 3-11. SEU Cross Section vs. LETeff for Dual Loop Mode with a Weibull Plot Fitted to the Data

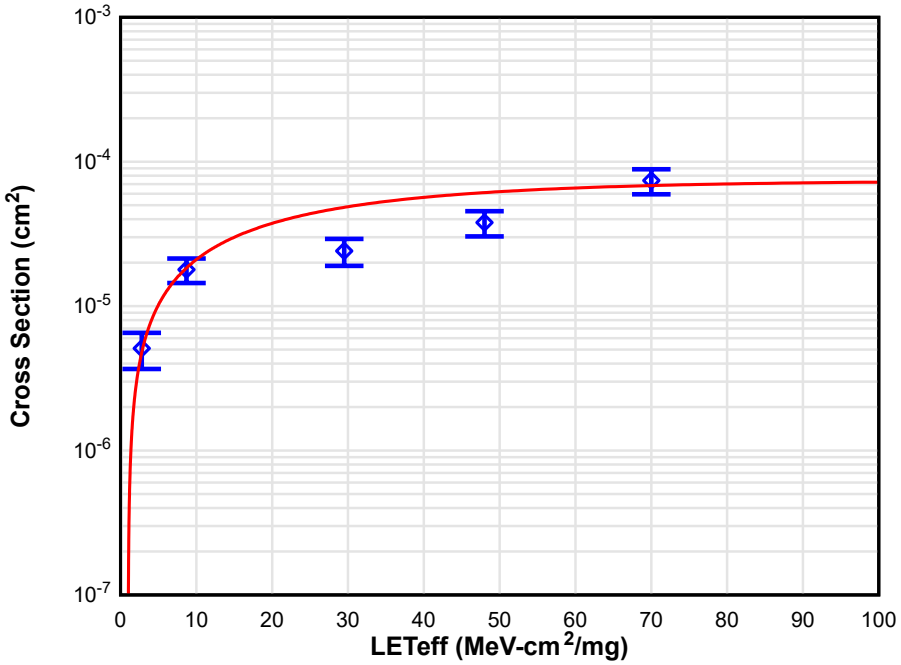

Figure 3-12. SEU Cross Section vs. LETeff for Dual Loop, Nested 0-Delay Mode with a Weibull Plot Fitted to the Data

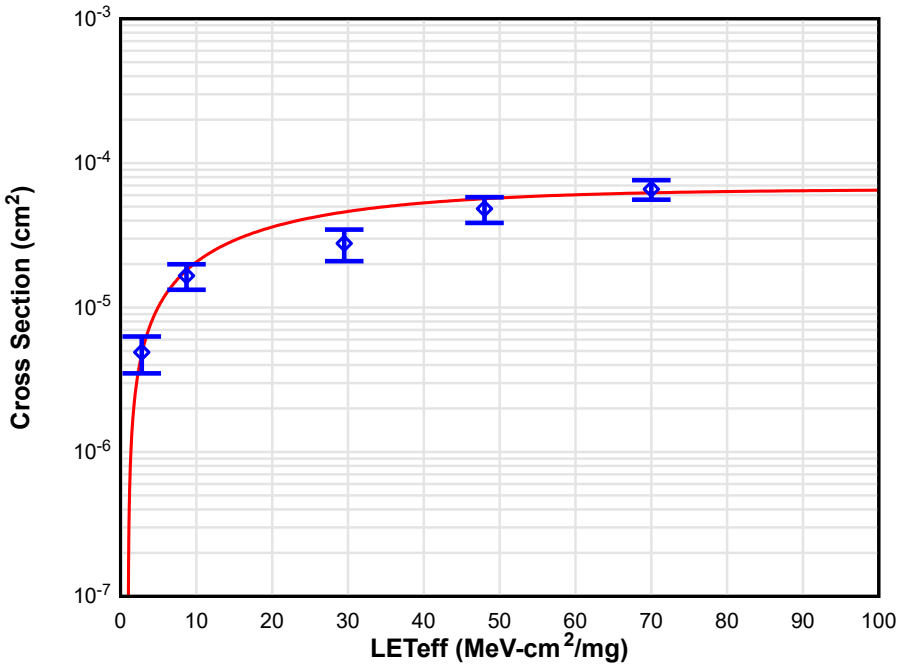

Figure 3-13. SEU Cross Section vs. LETeff for Single Loop Mode with a Weibull Plot Fitted to the Data

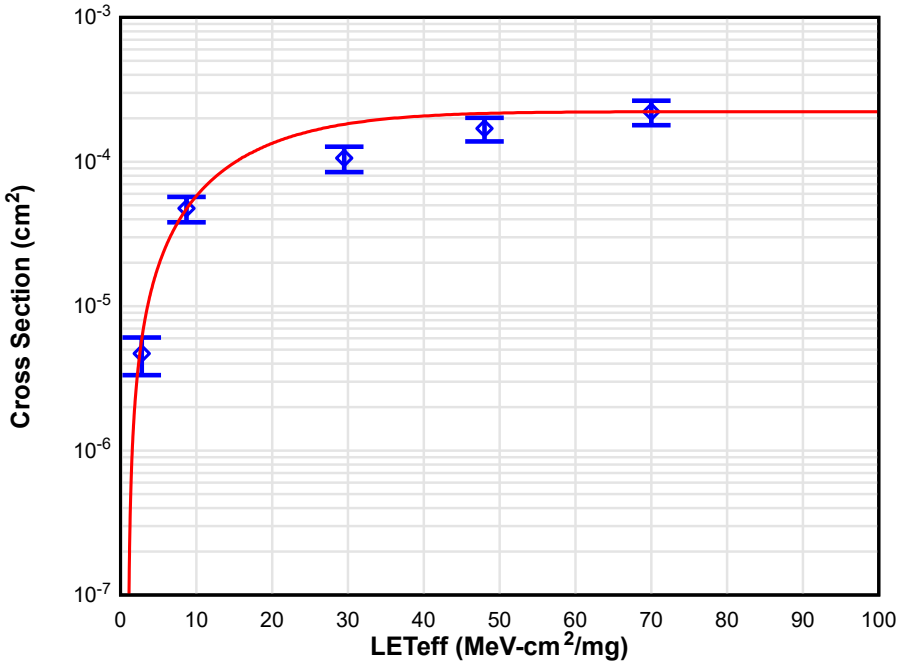

Figure 3-14. SEU Cross Section vs. LETeff for Distribution Mode with a Weibull Plot Fitted to the Data

Event rates (Table 3-5) were calculated for LEO(ISS) and GEO environments using the CREME96 orbital integral flux estimations assuming a minimum shielding configuration of 100 mils (2.54 mm) of aluminum, and “worst-week” solar activity (similar to a 99% upper bound for the environment) described in "Heavy Ion Orbital Environment Single-Event Effects Estimations"[8]. Instead of using the simple "square approximation" the flux data was integrated with the SEU cross sections determined by the Weibull fits. Also included is a Figure of Merit (FOM) Equation 2 [7] calculation for each of the four operating modes tested. The cross sections at the highest LETeff tested (70 MeV-cm2 /mg) were used for the limiting cross sections. $L_{0.25}$, the LET where the cross section is one fourth of the limiting cross section, is found from the Weibull plot.

$$FOM = 200 \times \frac{A}{L_{0.25}^2}$$

where, A is the limiting cross-section
$L_{0.25}$ is the LET at 25% of the limiting cross-section

(2)

Table 3-5. SEU Weibull Fit Parameters, Event Rate Predictions for Worst Solar Week, and Figure of Merit Calculations for the Operating Modes Tested

	Weibull Fit Parameters				Event Rate (Event/Day)		
	A	Lo	W	s	LEO (ISS)	GEO	FOM
Dual Loop	8.54×10^{-5}	1	25	1.1	5.89×10^{-3}	5.85×10^{-2}	2.08×10^{-4}
Dual Loop Nested 0-Delay	7.41×10^{-5}	1	27	1.0	5.89×10^{-3}	5.95×10^{-2}	1.92×10^{-4}
Single Loop 0-Delay	6.60×10^{-5}	1	25	1.0	5.62×10^{-3}	5.69×10^{-2}	1.96×10^{-4}
Distribution	2.22×10^{-4}	1	20	1.5	1.00×10^{-2}	9.50×10^{-2}	4.70×10^{-4}

4 Summary

Under heavy ion testing, the LMK04832-SP was found to be SEL and SEFI immune up to 121 MeV-cm^2/mg. SEL testing was performed at maximum operating voltage (3.45 V) and with the junction at greater than the maximum operating temperature (125°C). SEU was characterized. The majority of events lasted less than one clock cycle and maximum length of any events was 22 clock cycles. Upset rates were calculated for the worst case solar week for LEO (ISS) and GEO orbits and a commonly used FOM was calculated. Testing was performed under multiple operating conditions so that all functional block types were functional sometime during the testing.

5 References

1. Texas Instruments, Dallas, TX, “LMK04832-SP Space Grade Ultra-Low-Noise JESD204B Dual-Loop Clock Jitter Cleaner,” May 2020, SNAS698
2. Standard Microcircuit Drawing 5962-17237, Depart. of Defense, DLA Land and Maritime, Columbus OH, https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Smd/17237.pdf
3. Texas Instruments, Dallas, TX, “JESD204B Overview,” July 2016, http://www.ti.com/lit/ml/slap161/slap161.pdf
4. Texas Instruments, Dallas, TX, “LMK04832EVMCVAL User's Guide,” June 2020, SNAU252
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