TEXAS INSTRUMENTS

SLVP101, SLVP102, and SLVP103 Buck Converter Design Using the TL5001

User's Guide

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Mailing Address:

Texas Instruments
Post Office Box 655303
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Preface

Read This First

About This Manual

This User's Guide describes the design, construction, and operation of the SLVP101, SLVP102, and SLVP103 Buck Converters using the TL5001 PWM Controller.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 Hardware describes the circuits, test setups, board layouts, materials, and test results for the buck converter modules.
- Chapter 2 Design Procedure describes the operating specifications and design procedure for the modules.

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This book may contain cautions and warnings.

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Related Documentation From Texas Instruments

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Designing with the TL5001C PWM Controller Application Report (Literature number SLVA034).

Examples of Applications with the Pulse Width Modulator TL5001 User's Guide (Literature number SLVAE05)

SLVP089 Synchronous Buck Converter Evaluation Module User's Guide (Literature number SLVU001)

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Contents

Figures

Tables

Chapter 1

Hardware

The SLVP101, SLVP102, and SLVP103 buck regulator dc/dc converter modules provide a cost-effective solution for supplying power to a high performance digital signal processor (DSP) such as the Texas Instruments TMS320C6201. The SLVP101 is a nominal 5-V-input-to-3.3-V-output regulator. The SLVP102 is a 5-V-to-2.5-V regulator, and the SLVP103 is a 5-V-to-1.8-V regulator. These converter modules use several devices manufactured by Texas Instruments for use in low-cost power supply circuits while maintaining excellent overall performance. This document explains basic power conversion circuit construction including the design of the buck power stage topology, the TL5001 control chip functions, and output voltage feedback loop frequency compensation. This guide also describes the application of the TL1431 reference IC, the TPS2817 MOSFET driver IC, and the TLV2231 operational amplifier in these modules.

These converter modules provide I/O power (3.3 V) and internal core power (2.5V, 1.8 V for revision 3 devices) to the Texas Instruments TMS320C6201 DSP. These modules satisfy all requirements for powering this high performance DSP such as low cost, low parts count, good transient response, and excellent output voltage accuracy.

To power the ’C6201 DSP, separate supplies must supply the I/O and core power, and proper power sequencing must be provided. Both power supplies should be brought up simultaneously to protect the device. If this is not possible, the I/O supply (DVdd) must not exceed the core supply (CVdd) by more than 2 V, and the CVdd must not exceed DVdd by more than 0.5 V. Both power supplies must achieve 95% of their voltage level within a 25 ms window, and must be able to handle an output current of 3 A (maximum consumption by the device). External circuits must be added to ensure that these sequencing requirements are met.

This chapter includes the following topics:

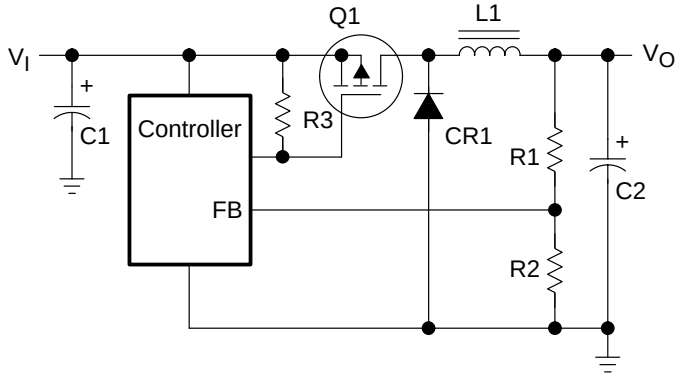
Topic **Page**

1.1 Introduction

Low cost and simplicity of design make buck converters popular solutions in dc/dc step-down applications where lack of isolation from the input source is not a concern.

Figure 1–1 shows a diagram of a typical buck converter. The converter passes a duty-cycle modulated pulse waveform through a low-pass output filter (L1, C2) to produce a dc voltage. An error amplifier senses the output voltage, compares it to a reference voltage and adjusts the width of the power switch (Q1) on time, to maintain the desired output voltage. A commutating diode (CR1) provides a path for inductor current to continue to flow when the power switch is turned off.

Figure 1–1. Typical Buck Converter Block Diagram



The SLVP101, SLVP102, and SLVP103 buck converters use the Texas Instruments TL5001 PWM controller to give power supply outputs of 3.3 V, 2.5 V, and 1.8 V at 0 to 3 A. Also featured in this design are the TL1431 reference IC, the TPS2817 MOSFET driver IC, and the TLV2231 operational amplifier. These converters operate over an input voltage range of 4.5 V to 9 V with typical efficiences of 90 percent for 3.3 V out and 80 percent for 1.8 V out.

Chapter 2 lists full design specifications. The TL5001 controller provides the oscillator, the PWM comparator, undervoltage lock-out, and short circuit protection for the power supply. The oscillator sets the switching frequency. The PWM comparator compares the error amplifier output to a ramp voltage to produce the required pulse width for output voltage regulation. Undervoltage lock-out prevents the power supply from operating when the input voltage is too low for proper operation. Short circuit protection prevents accidental short circuits applied to the output from destroying the power supply.

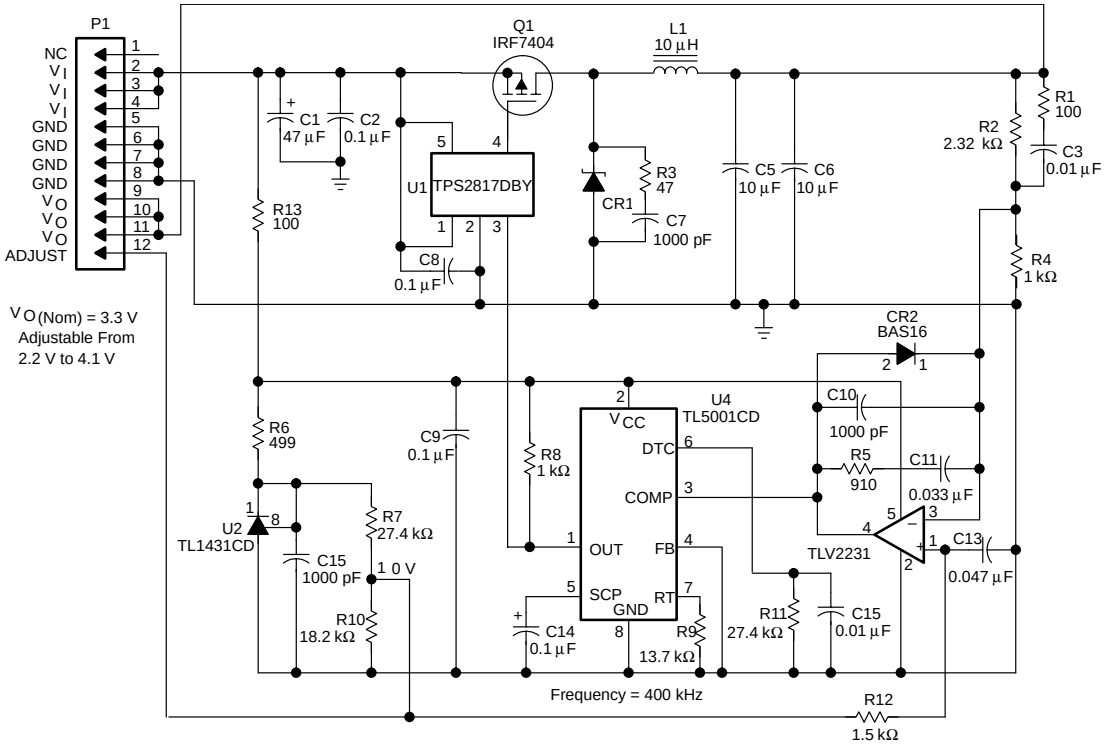
Short circuit protection

Short circuit protection protects against short circuits only. If the output load current is increased beyond the rated value, damage may occur to the power supply. Short circuit protection does not imply overload protection.

1.2 Schematic

Figure 1–2 shows the SLVP101 schematic diagram. The schematic diagrams for the SLVP102 and SLVP103 are identical except for a different value for resistor R4.

Figure 1–2. SLVP101 Schematic



1.3 Test Setup

Do the following steps for initial power-up of the SLVP101:

1) If necessary for improved load transient response, connect an external electrolytic capacitor of at least 100 μF from the SLVP101 output to ground. The external capacitor is not necessary for proper operation.

2) Connect an electronic load adjusted to draw approximately 1 A at 3.3 V. The exact current is not critical; any nominal current is sufficient. A fixed resistor can also be used in place of the electronic load. The output current drawn by the resistor is

   $I_O = \frac{3.3\ V}{R}$ where R is the value of the load resistor. The power rating of the resistor, P_R should be at least $\frac{3.3^2}{R}$.

3) No connection to the adjustment pin is necessary at this time.

4) Connect a lab power supply to the input of the SLVP101. Make sure that the current limit is set for at least 2 A. Turn the voltage up to 5 V.

5) Verify that the SLVP101 output voltage (measured at the module output pins) is 3.3 V ±0.07 V.

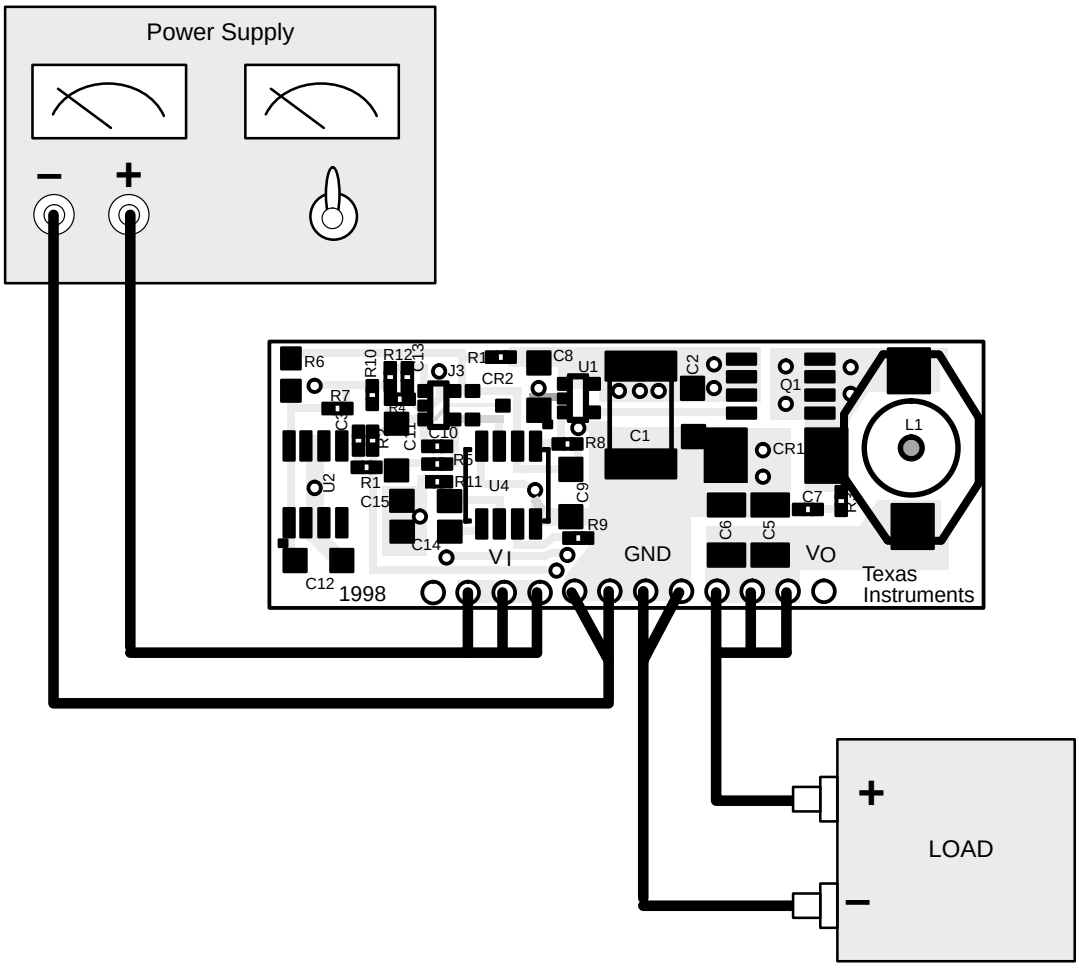
6) For subsequent testing, make sure the lab supply output current capacity and current limit are at least 3.5 A, so that the SLVP101 can be operated at a maximum load of 3 A.

7) Refer to section 1.6 for selected typical waveforms and operating conditions for verification of proper module operation.

For initial power-up of the other modules, simply replace any reference to 3.3 V in the above discussion with a reference to the appropriate output voltage.

Figure 1–3 shows the SLVP101 test setup.

Figure 1–3. Test Setup



1.4 Board Layout

Figures 1–4 through 1–6 show the board layout for the SLVP101, SLVP102, and SLVP103.

Figure 1–4. Component Placement Showing Component-Side Copper

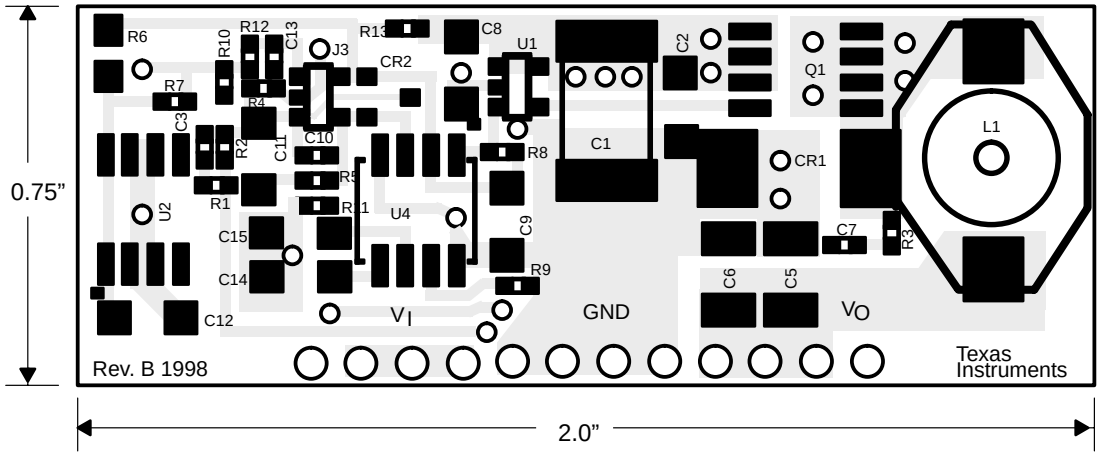


Figure 1–5. Component-Side Copper

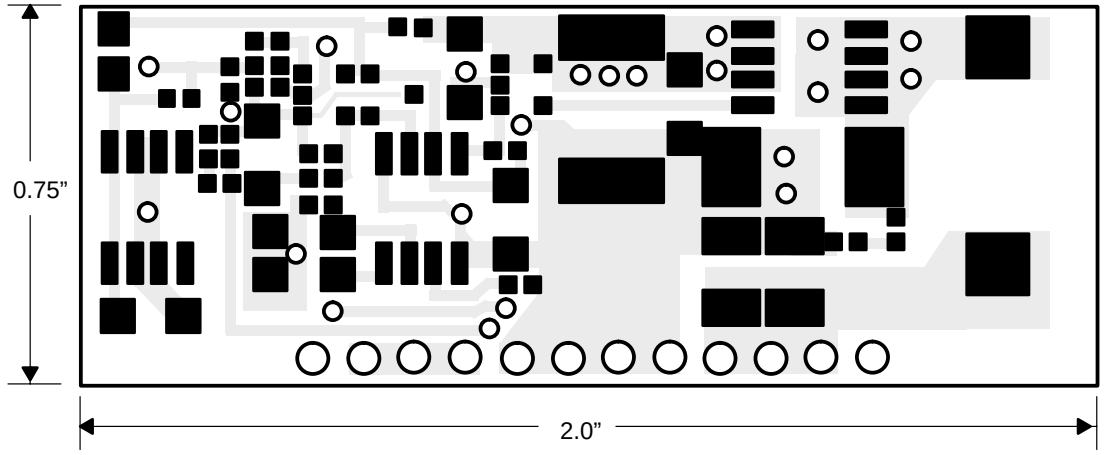
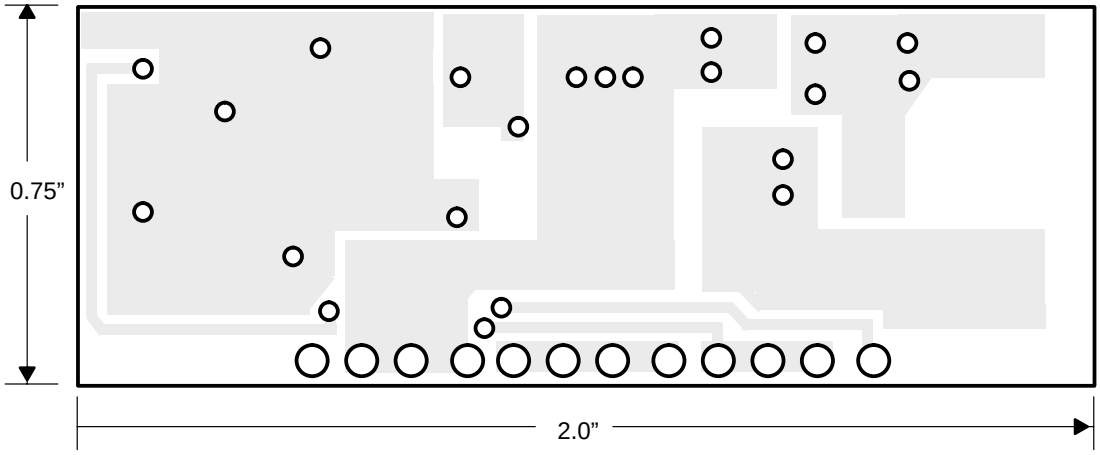


Figure 1–6. Solder-Side Copper



1.5 Bill of Materials

Table 1–1 lists materials required for the SLVP101.

Table 1–1. Bill of Materials

Reference	Part Number	Mfr	Description	Size
C1	ECS-T1AD476R	Panasonic	Capacitor, Tantalum, 47 μF, 10 V	D case
C2		Panasonic	Capacitor, Ceramic, 0.1 μF, 50 V, X7R	603
C3		Panasonic	Capacitor, Ceramic, 0.01 μF, 25 V, X7R	603
C4 (ext.)			Capacitor, Tantalum, 100 μF, 6.3 V	
C5	GRM235Y5V106Z016AL	Murata	Capacitor, Ceramic, 10 μF, 16 V	1210
C6	GRM235Y5V106Z016AL	Murata	Capacitor, Ceramic, 10 μF, 16 V	1210
C7		Panasonic	Capacitor, Ceramic, 1000 pF, 50 V, X7R	603
C8		Panasonic	Capacitor, Ceramic, 0.1 μF, 50 V, X7R	1206
C9		Panasonic	Capacitor, Ceramic, 0.1 μF, 50 V, X7R	1206
C10		Panasonic	Capacitor, Ceramic, 1000 pF, 50 V, X7R	603
C11		Panasonic	Capacitor, Ceramic, 0.033 μF, 50 V, X7R	1206
C12		Panasonic	Capacitor, Ceramic, 1000 pF, 50 V, X7R	1206
C13		Panasonic	Capacitor, Ceramic, 0.047 μF, 50 V, X7R	603
C14		Panasonic	Capacitor, Ceramic, 0.1 μF, 50 V, X7R	1206
C15		Panasonic	Capacitor, Ceramic, 0.01 μF, 50 V, X7R	1206
CR1	MBRS340T3	Mot	Diode, Schottky, 3 A, 40 V	SMC
L1	DO3316P-103	Coilcraft	Inductor, 10 μH, 3.9 A, 0.025 Ω	0.51 × 0.37
Q1	IRF7404	IR	MOSFET, P-Ch, 20 V, 0.040 Ω	SO-8
R1	ERJ-3GSYJ101	Panasonic	Resistor, CF, 100 Ω, 5%	603
R2	ERJ-3EKF2321	Panasonic	Resistor, MF, 2.32 kΩ, 1%	603
R3	ERJ-3GSYJ470	Panasonic	Resistor, CF, 47 Ω, 5%	603
R4*	ERJ-3EKF1001	Panasonic	Resistor, MF, 1.00 kΩ, 1%	603
R5	ERJ-3GSYJ911	Panasonic	Resistor, CF, 910 Ω, 5%	603
R6	ERJ-6ENF4990	Panasonic	Resistor, MF, 499 Ω, 1%	805
R7	ERJ-3EKF2742	Panasonic	Resistor, MF, 27.4 kΩ, 1%	603
R8	ERJ-3GSYJ102	Panasonic	Resistor, CF, 1.0 kΩ, 5%	603
R9	ERJ-3EKF1372	Panasonic	Resistor, MF, 13.7 kΩ, 1%	603
R10	ERJ-3EKF1822	Panasonic	Resistor, MF, 18.2 kΩ, 1%	603
R11	ERJ-3EKF2742	Panasonic	Resistor, MF, 27.4 kΩ, 1%	603
R12	ERJ-3GSYJ152	Panasonic	Resistor, CF, 1.5 kΩ, 5%	603
R13	ERJ-3GSYJ101	Panasonic	Resistor, CF, 100 Ω, 5%	603
U1	TPS2817DBV	TI	Driver, high-speed, single channel	SOT23-5
U2	TL1431CD	TI	Shunt regulator, 37 V, 100 mA	SO-8
U3	TLV2231DBV	TI	Op amp, single channel	SOT23-5
U4	TL5001CD	TI	PWM controller	SO-8
P1			Header, 12-pin, 0.1 in centers	

* The value of R4 for the SLVP102 is 1.54 kΩ; the value for the SLVP103 is 2.91 kΩ.

1.6 Test Results

Table 1–2 lists measured line/load regulation for the SLVP101, and Figures 1–7 through 1–13 show test results for the SLVP101 and SLVP103.

Table 1–2. Measured SLVP101 (3.3 V Output) Line/Load Regulation

Line/Load	0.5 A	1.0 A	1.5 A	2.0 A	2.5 A	3.0 A	Load Reg.
4.5 V Vo(V)	3.336	3.336	3.336	3.336	3.336	3.336	0.0%
5.0 V Vo(V)	3.336	3.336	3.336	3.336	3.336	3.336	0.0%
6.0 V Vo(V)	3.337	3.337	3.337	3.337	3.337	3.337	0.0%
Line Reg.	**0.3%**	**0.3%**	**0.3%**	**0.3%**	**0.3%**	**0.3%**	

Note: The calculation for load regulation only accounts for the worst case of load variation under a particular input voltage condition. All voltages were measured at the PCB header pins.

Figure 1–7. Measured SLVP101 (3.3 V Output) Efficiency vs. Load and Line

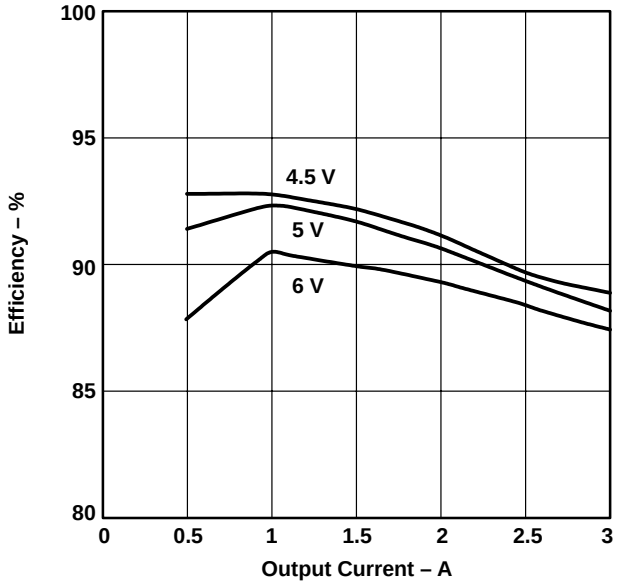


Figure 1–8. Measured SLVP103 (1.8 V Output) Efficiency vs. Load

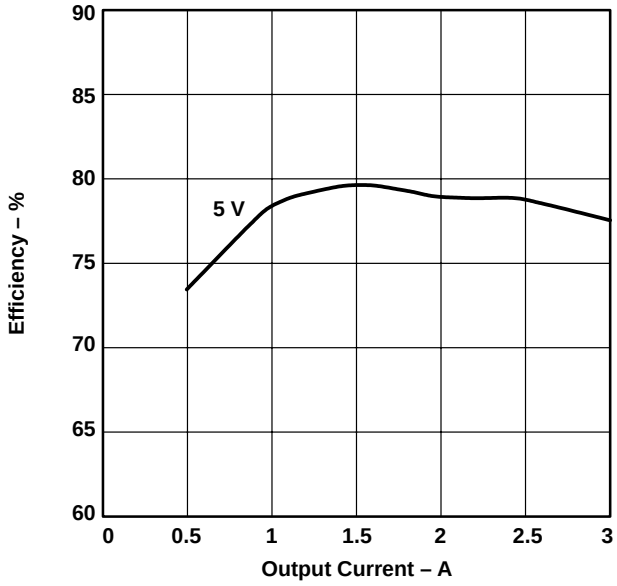


Figure 1–9. SLVP101 (3.3 V Output) Startup (Resistive Load)

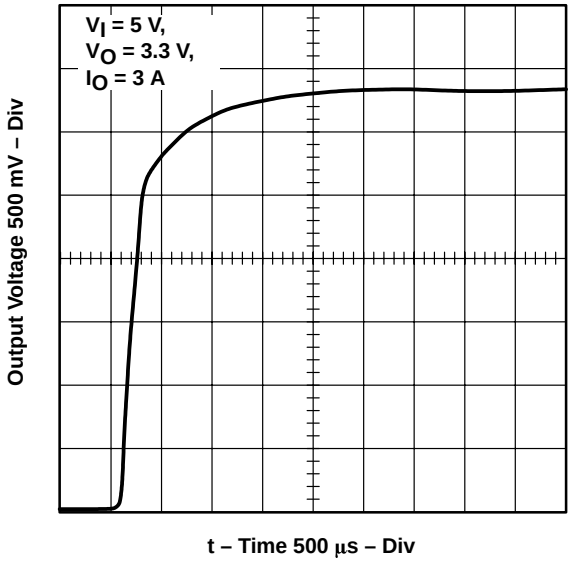


Figure 1–10. SLVP101 (3.3 V Output) Startup (No Load)

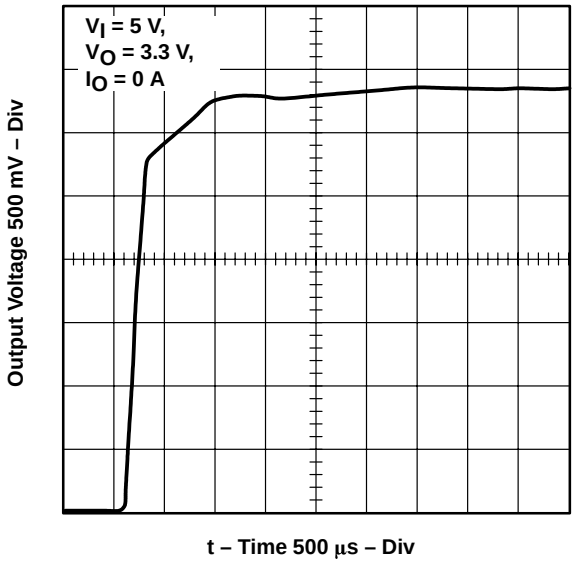


Figure 1–11. SLVP101 (3.3 V Output) 100% Load Output Voltage Ripple

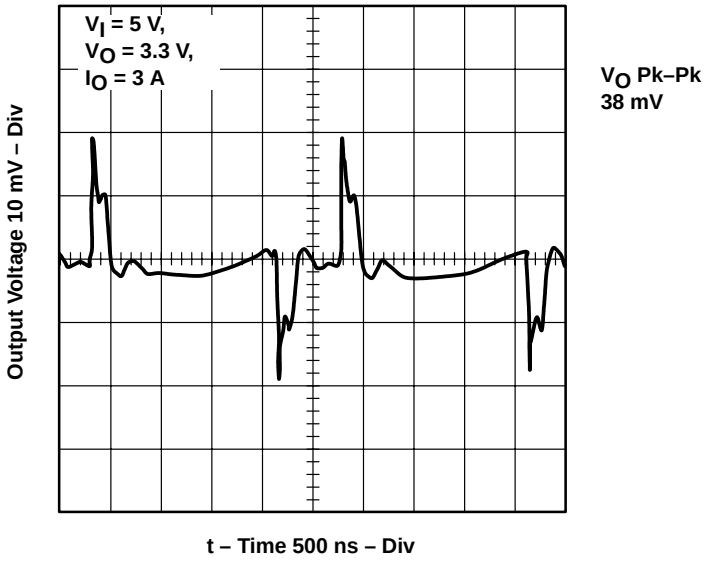


Figure 1–12. SLVP101 (3.3 V Output) 50% Load Output Voltage Ripple

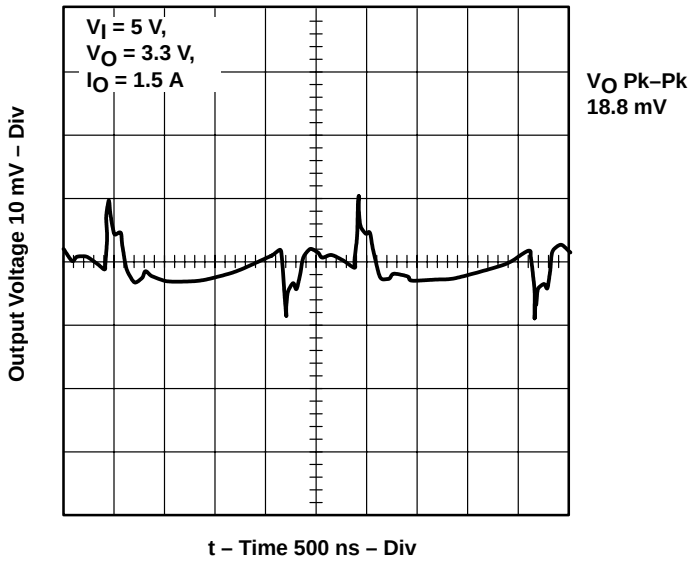


Figure 1–13. SLVP101 (3.3 V Output) Pulse Load Response

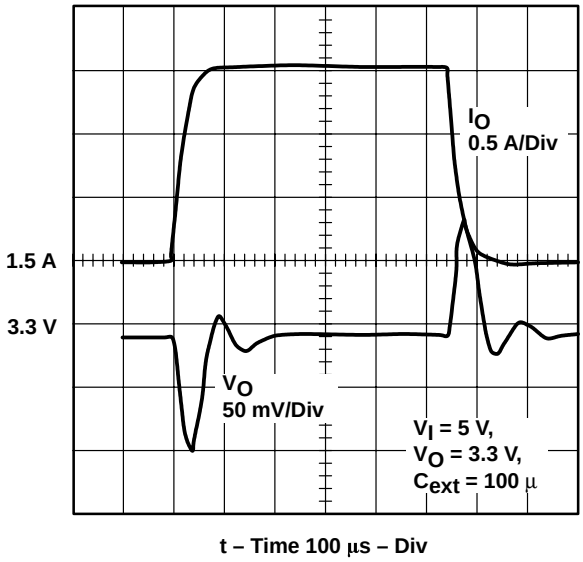


Figure 1–14. SLVP101 (3.3 V Output) CR1 Cathode Switching Waveform

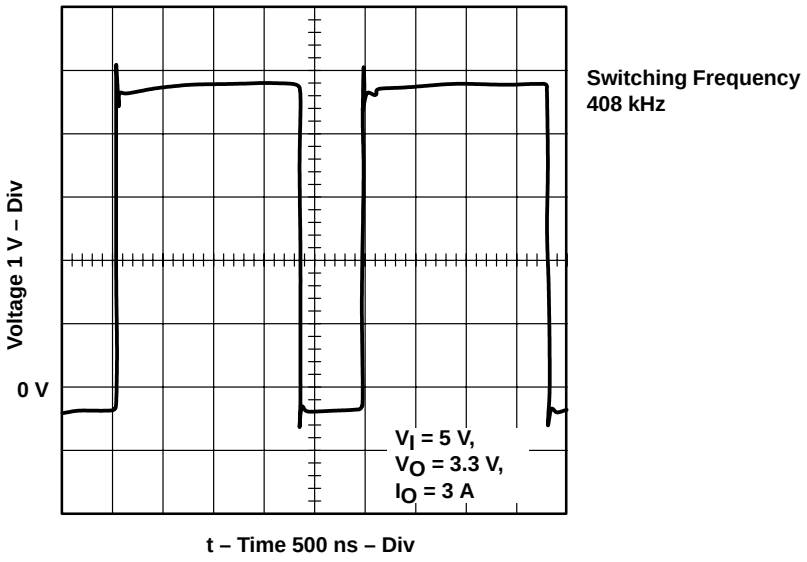


Figure 1–15. SLVP101 (3.3 V Output) TL5001 PWM Output Switching Waveform

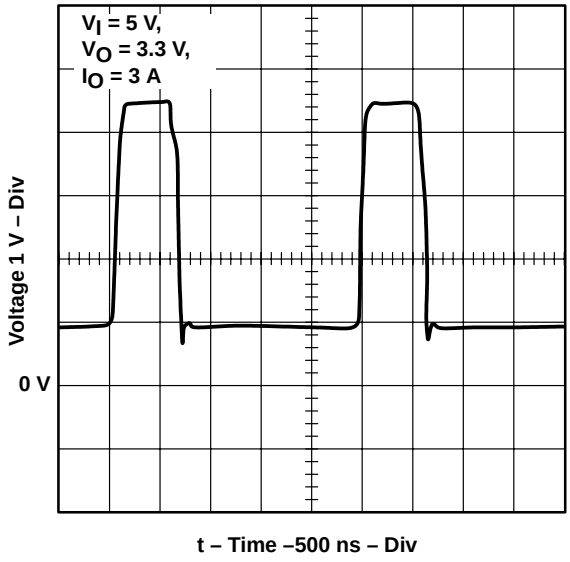


Figure 1–16. SLVP103 (1.8 V Output) Startup (No Load)

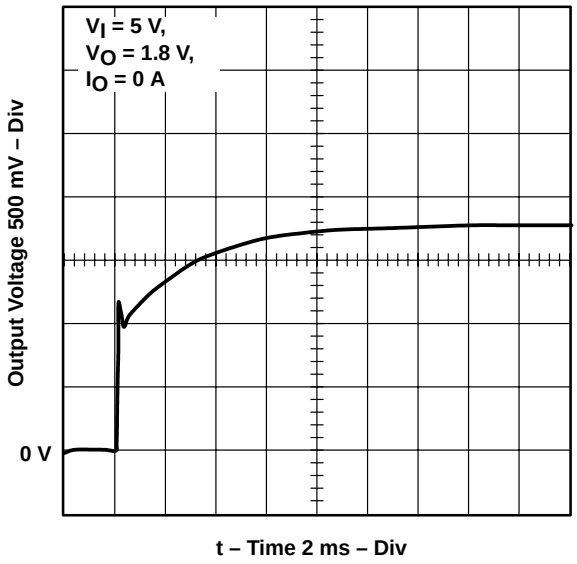
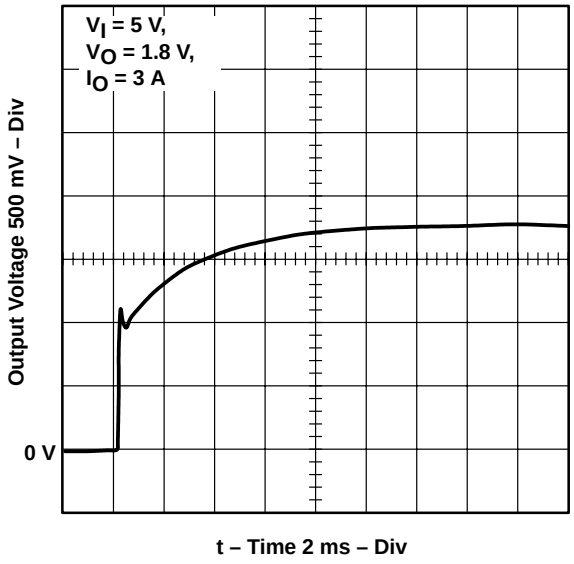


Figure 1–17. SLVP103 Startup (1.8 V Output) (Resistive Load)



Chapter 2

Design Procedure

The SLVP101, SLVP102, and SLVP103 buck regulator dc/dc converter modules provide a method for evaluating the performance of the TPS2817 MOSFET driver and the TL5001 PWM controller. The TPS2817 contains all of the circuitry necessary to drive large power MOSFET transistors and includes a voltage regulator for higher voltage applications. This section explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. This chapter includes the following topics:

Topic **Page**

2.1 Introduction

The SLVP101, SLVP102, and SLVP103 are dc-dc buck converter modules that provide a regulated output voltage at up to 3 A with an input voltage range of 4.5–9 V. The controller is a TL5001 PWM operating at a nominal frequency of 400 kHz. To obtain the required output voltage accuracy and stability necessary for critical DSP applications, a TL1431 adjustable shunt regulator provides a ±0.8% reference voltage. The feedback control loop uses a TLV2231 operational amplifier as the error amplifier because the TL5001 internal amplifier is not accessible. The TL5001 is configured for a maximum duty cycle of 100 percent and has soft-start and short-circuit protection built in. The output voltage is adjustable by connecting a resistor from the adjust pin to either ground or V_O. The adjustment range is 2.2 V to 4.1 V for the SLVP101, depending on the value of the adjustment resistor. The recommended values of adjustment resistor are shown in Table 2–2.

2.2 Operating Specifications

Table 2–1 lists the operating specifications for the SLVP101, SLVP102, and SLVP103.

Table 2–1. Operating Specifications (see Note 1)

Specification		Min	Typ	Max	Units
Input Voltage Range		4.5		9	V
Static Voltage Tolerance (see Note 2)					
SLVP101		3.2	3.3	3.4	V
SLVP102		2.4	2.5	2.6	V
SLVP103		1.7	1.8	1.9	V
Line Regulation (see Note 3)			±25	±50	mV
Load Regulation (see Note 4)			±25	±50	mV
Transient Response (see Note 5)	Deviation		±200		mV pk
	Recovery Time		200		μs
Output Voltage Range (see Note 6)					
SLVP101		2.2	3.3	4.1	V
SLVP102		2	2.5	3	V
SLVP103		1.3	1.8	2.3	V
Output Current Range (see Note 7)		0		3	A
Current Limit (see Note 7)			N/A		
Operating Frequency (see Note 1)			400		kHz
Output Ripple (see Note 1)			66		mV p-p
Efficiency, 3-A Load					
SLVP101			88%		
SLVP102			82%		
SLVP103			77%		
Efficiency, 1.5-A Load					
SLVP101			92%		
SLVP102			85%		
SLVP103			79%		

Notes:
1) Unless otherwise specified, all test conditions are T_A = 25°C, V_I = 5 V, I_O = 3 A, V_O = nominal
2) V_I = 5 V, I_O = 3 A.
3) I_O = 3 A.
4) V_I = 5 V.
5) V_I = 5 V, I_O stepped repetitively from 1.5 A to 3 A.
6) See Table 2–2 for required values of adjustment resistor.
7) Output current rating is limited by thermal considerations. Load currents above this rating may cause damage to the power supply.

Tables 2–2, 2–3, and 2–4 list the recommended adjustment resistor values.

Table 2–2. SLVP101 (3.3 V Output) Adjustment Resistor Values

Voltage	Resistance	Connection
2.2	21.5 kΩ	A
2.3	24.9 kΩ	A
2.4	28.7 kΩ	A
2.5	34.0 kΩ	A
2.6	40.2 kΩ	A
2.7	48.7 kΩ	A
2.8	60.4 kΩ	A
2.9	76.8 kΩ	A
3.0	105 kΩ	A
3.1	158 kΩ	A
3.2	309 kΩ	A
3.3		
3.4	976 kΩ	B
3.5	475 kΩ	B
3.6	316 kΩ	B
3.7	243 kΩ	B
3.8	196 kΩ	B
3.9	169 kΩ	B
4.0	147 kΩ	B
4.1	133 kΩ	B

Table 2–3. SLVP102 (2.5 V Output) Adjustment Resistor Values

Voltage	Resistance	Connection
2.0	44.2 kΩ	A
2.1	59.0 kΩ	A
2.2	82.5 kΩ	A
2.3	130 kΩ	A
2.4	280 kΩ	A
2.5		
2.6	402 kΩ	B
2.7	215 kΩ	B
2.8	150 kΩ	B
2.9	118 kΩ	B
3.0	97.6 kΩ	B

Table 2–4. SLVP103 (1.5 V Output) Adjustment Resistor Values

Voltage	Resistance	Connection
1.3	7.15 kΩ	A
1.4	8.06 kΩ	A
1.5	9.09 kΩ	A
1.6	10.2 kΩ	A
1.7	11.5 kΩ	A
1.8		
1.9	158 kΩ	B
2.0	84.5 kΩ	B
2.1	60.4 kΩ	B
2.2	47.5 kΩ	B
2.3	40.2 kΩ	B

Notes: Connect adjustment resistance from adjustment pin to GND for connection A
Connect adjustment resistance from adjustment pin to V_O for connection B.

2.3 Design Procedures

Detailed steps in the design of a buck-mode converter may be found in *Designing With the TL5001C PWM Controller* (literature number SLVA034) from Texas Instruments. This section shows the basic steps involved in this design, for a nominal 3.3-V output.

2.3.1 Duty Cycle Estimate

The duty cycle, D, is the ratio of the power switch conduction time to the period of one switching cycle. An estimate of the duty cycle is used frequently in the following sections. The duty cycle for a continuous-mode step-down converter is approximately:

$$D = \frac{V_O + V_d}{V_I - V_{SAT}}$$

From the manufacturer's data sheet for the commutating diode, the forward voltage is V_d = 0.45 V at 3 A forward current. Similarly, from the IFR7404 data sheet, the switch ON voltage, V_{SAT}, can be estimated by multiplying the drain-source on resistance, $R_{DS(on)}$, of 40 mΩ by the on state drain current, I_D, of 3 A, giving 0.12 V. The duty cycle for V_I = 4.5, 5, and 9 V is 0.86, 0.77, and 0.42, respectively.

2.3.2 Output Filter

A buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 10 percent of the rated output load at maximum input voltage:

$$\Delta I_O = 2 \times 0.10 \times I_O = 2 \times 0.10 \times 3 = 0.6 \text{ A}$$

The inductor value needed is:

$$L = \frac{\left(V_I - V_{SAT} - V_O\right) \times D \times t}{\Delta I_O}$$

$$= \frac{(9 - 0.12 - 3.3) \times 0.42 \times \left(2.5 \times 10^{-6}\right)}{0.6} = 9.8 \ \mu\text{H}$$

The two criteria for selecting the output capacitor are the amount of capacitance needed and the capacitor's equivalent series resistance (ESR). After the capacitance and ESR requirements are determined, the capacitor can be selected.

Assuming that all of the inductor ripple current flows through the capacitor and the effective ESR is zero, the capacitance needed is:

$$C = \frac{\Delta I_O}{8 \times f \times \left(\Delta V_O\right)} = \frac{0.6}{8 \times \left(400 \times 10^3\right) \times 0.05} = 3.75 \ \mu\text{F}$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.6} = 0.083\ \Omega$$

To provide margin, the output filter capacitor should be rated greater than the calculated capacitance and have lower ESR than calculated. Due to available volume, this design uses two 10 μF ceramic capacitors. This capacitance provides adequate filtering, but for improved load transient response, it is recommended that a 100 μF electrolytic capacitor be installed external to the module and as close as possible to the output pins.

2.3.3 Power Switch

The design uses a p-channel MOSFET to simplify the drive-circuit design and minimize component count. The IRF7406 p-channel power MOSFET is selected for it's low $r_{DS(on)}$ of 40 mΩ and drain-to-source breakdown voltage of 20 V.

Power dissipation, which includes conduction and switching losses, is given by:

$$P_D = \left(I_O^2 \times r_{DS(on)} \times D\right) + \left(0.5 \times V_I \times I_O \times t_{r+f} \times f\right)$$

The example power MOSFET power dissipation calculation below is made with these assumptions:

- Total switching time, t_{r+f}, = 100 ns
- High temperature adjustment factor, $r_{DS(on)}$, = 1.25
- Maximum ambient temperature = 55°C
- V_I = 5 V
- I_O = 3 A

$$P_D = \left[3^2 \times (0.040 \times 1.25) \times 0.77\right] + \left[0.5 \times 5 \times 3 \times \left(100 \times 10^{-9}\right) \times \left(400 \times 10^3\right)\right] = 0.347 + 0.30 = 0.647\ W$$

The thermal impedance $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_j = T_A + (R_{\theta JA} \times P_D) = 55 + (90 \times 0.647) = 113.2°C$$

Conduction losses are nearly equal to switching losses in this application but may not be in others. It is good practice to check dissipation at the extreme limits of input voltage to find the worst case.

2.3.4 Rectifier

The catch rectifier conducts during the time interval when the MOSFET is off. The MRBS340T3 is a 3.0-A, 40-V rectifier in a surface-mount SMC package. For the same operating conditions as above, the rectifier power dissipation is:

$$P_D = I_O \times V_D(1 - D) = 3.0 \times 0.45 \times 0.23 = 0.31\ W$$

2.3.5 Snubber Network

A snubber network is usually needed to suppress the ringing at the node where the power switch drain, output inductor, and the rectifier connect. The snubber design is dependent on PWB layout and component parasitics, but as a starting point, select a snubber capacitor with a value that is 4–10 times larger than the estimated capacitance of the catch rectifier. The power dissipated in the snubber resistor is directly proportional to this capacitor value, so this value should be chosen with care. The MBRS340TC has a capacitance of about 150 pF at a reverse voltage of 5 V. For this design, a capacitor value of 1000 pF was selected. A 47-Ω resistor was then selected. The resistor value selection is often a trial-and-error sequence of steps, but it should be chosen so that the snubber RC time constant times 3 is less than the minimum on time of the power switch. This allows the snubber capacitor to fully charge and discharge each portion of the switching period.

2.3.6 Controller Functions

The TL5001 controller functions, oscillator frequency, soft-start, dead-time control, and short-circuit protection, are discussed in this section.

The oscillator frequency is set by selecting the resistance value from the graph in Figure 6 of the TL5001 data sheet. For 400 kHz, a value of 13.7 kΩ is selected.

Dead-time control provides a minimum off-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 100 percent is chosen. Then R is calculated as:

$$R_{DT} = \left(R_{OSC} + 1.25\ k\Omega\right) \times \left[D \times \left(V_{OSC(100\%)} - V_{OSC(0\%)}\right) + V_{OSC(0\%)}\right]$$
$$= (13.7\ k\Omega + 1.25\ k\Omega) \times [1 \times (1.5 - 0.5) + 0.5] = 22.4\ k\Omega$$

Any value higher than the calculated value will be satisfactory since the duty cycle limit is 100 percent. A value of 27.4 kΩ is used in this design.

Soft-start is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor. In this design, a soft-start time of 100 μs is used:

$$C \approx \frac{3 \times t_R}{R_{DT}} = \frac{3 \times 100 \times 10^{-6}}{27.4\ k\Omega} = 0.011\ \mu F \Rightarrow 0.01\ \mu F$$

The TL5001 has short circuit protection (SCP) instead of a current sense circuit. If not used, the SCP terminal must be connected to ground to allow the converter to start up. If used, a timing capacitor is connected to SCP that should have a time constant that is greater than the soft-start time constant. This time constant is chosen to be 10 ms:

$$C(\mu F) = 12.46 \times t_{SCP} = 12.46 \times 0.01\ s = 0.125\ \mu F \Rightarrow 0.1\ \mu F$$

The power supply is rated for a maximum output current of 3 A due to thermal considerations. Although the power supply has short circuit protection, it does not have overload protection. If load current exceeds 3 A, the power supply may fail or have a reduced lifetime.

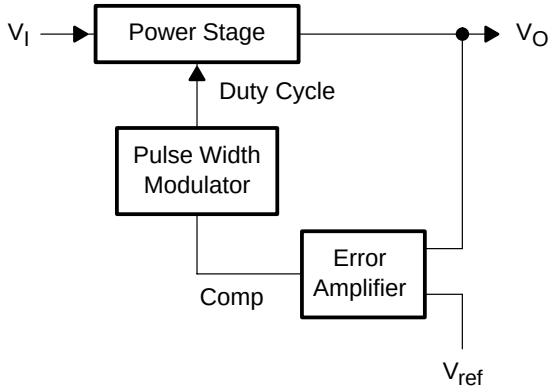
In addition, if a short circuit is applied to the power supply, the short circuit protection internal to the TL5001 will latch the power supply into an off state. To reset the latch, power must be removed from the input of the power supply and reapplied after the output short circuit is removed.

2.3.7 Loop Compensation

The control loop for this converter consists of three transfer functions: the power stage (G_{PS}), the error amplifier ($G_{E/A}$), and the internal TL5001 PWM modulator (G_{PWM}). Figure 2–1 shows a simplified block diagram of the control loop. Negative feedback stabilizes the output voltage against changes in line or load without destroying the control-loop's ability to respond to line and/or load transients. To maintain good performance and stability, it is necessary to tailor the open-loop frequency response of the converter. The frequency response of the error amplifier is shaped by judicious selection of external components to obtain a desired overall open-loop response. This tailoring of the converter frequency response is called loop compensation. A detailed

treatment of dc-to-dc converter stability analysis and design is beyond the scope of this report; however, several references on the subject are available.

Figure 2–1. Control Loop Simplified Block Diagram



The following is a simplified approach to designing networks to stabilize continuous mode buck converters. It works well when the open-loop gain is below unity at a frequency less than one-half of the switching frequency of the power supply.

Before the error-amplifier frequency response can be designed, the frequency response of the rest of the control loop must be determined. As mentioned above, this consists of the power stage transfer function and the pulse width modulator transfer function.

The first component of the control loop to be determined is the power stage. A gain block and a damped LC filter with a double complex pole can approximate the frequency response of the buck power stage operating in continuous conduction mode. There is also a zero due to the ESR of the external output capacitance. The low frequency magnitude of the gain is the change in output voltage divided by the change in the duty cycle. Without going

through the detailed derivation, a simplified expression for the transfer function of this continuous mode buck power stage is:

$$G_{PS}(s) = \frac{\Delta V_O}{\Delta D}$$

$$= V_i \times \frac{R}{R + R_L}$$

$$\times \frac{1 + s \times R_C \times C_O}{\left[1 + s \times \left(R_C \times C_O + \frac{L}{R}\right) + s^2 \times \left(L \times C_O\left(1 + \frac{R_C}{R}\right)\right)\right]}$$

$$\times \frac{1}{1 + s \times C_{CER} \times \frac{R \times R_C}{R + R_C}}$$

Where:

R = load resistance
C_O = total output capacitance
R_C = ESR of external aluminum electrolytic capacitance
C_{CER} = 20 μF internal ceramic capacitance
L = 10 μH internal output inductor value
R_L = equivalent resistance of internal inductor and FET $R_{DS(on)}$

The double pole from the LC filter (with 100 μF external capacitance) is at a frequency of:

$$\frac{1}{2 \times \Pi \times \sqrt{L \times C_O \times \left(1 + \frac{R_C}{R}\right)}} = 3.8 \text{ kHz}$$

The double pole from the LC filter (with no external capacitance) is at a frequency of:

$$\frac{1}{2 \times \Pi \times \sqrt{L \times C_O \times \left(1 + \frac{R_C}{R}\right)}} = 9.3 \text{ kHz}$$

The above two equations are important so that the control loop can be stabilized with or without external capacitance.

The zero due to the output capacitance and its ESR is at a frequency of:

$$\frac{1}{2 \times \Pi \times R_C \times C_O} = 2.65 \text{ kHz}$$

The second component of the control loop to be determined is the pulse width modulator. The response of a voltage mode pulse-width modulator can be modeled as a simple gain block. The magnitude of the gain is the change in

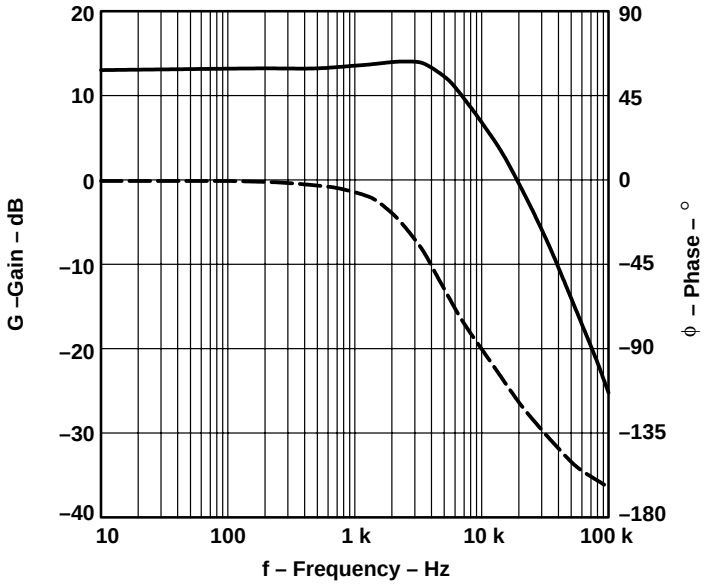
PWM output duty cycle for a change in the pulse-width-modulator input voltage (error-amplifier COMP voltage). From the TL5001 data sheet, Figure 11, PWM Triangle Wave Amplitude versus Frequency, the maximum triangle wave voltage at 400 kHz is approximately 1.5 V and the minimum is 0.5 V. As the error-amplifier voltage swings from 0.5 V to 1.5 V, the PWM output duty cycle changes from 0% to 100%.

Thus, G_{PWM}, is:

$$G_{PWM} = \frac{\Delta D}{\Delta V_{O(COMP)}} = \frac{1 - 0}{1.5 - 0.5} = 1.0 \Rightarrow 0 \text{ dB}$$

The product (sum in dB) of the transfer functions of these two control loop components (the power stage, G_{PS}, and the pulsewidth-modulator, G_{PWM}) makes up the uncompensated open-loop response. Figure 2–2 is a gain (solid line) and phase (dashed line) graph of the uncompensated open loop response of the converter obtained from a MathCad analysis. The operating conditions for the graph below are: V_i = 5 V, I_O = 3 A, C_O = 120 μF, and R_C = 0.5 Ω.

Figure 2–2. Uncompensated Open-Loop Response



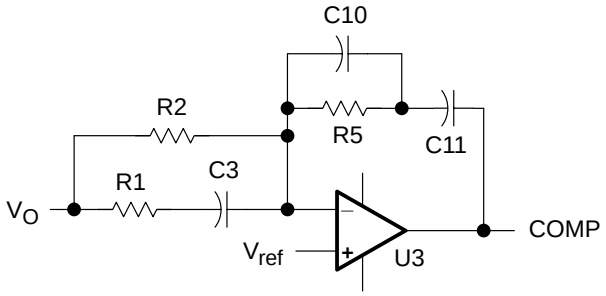
Now that the known parts of the control loop are determined, the error-amplifier frequency response can be designed. Unless the designer is trying to meet an unusual requirement, such as very wideband response, many of the decisions regarding gains, compensation pole and zero locations, and unity-gain bandwidth are at the discretion of the designer. Generally, the total open-loop response favored for stability is a 20-dB-per-decade rolloff with a desired phase margin of at least 45 degrees for all conditions. High gain at low frequencies is desired to minimize error in the output voltage and sufficient bandwidth must be designed into the circuit to assure that the converter has good transient response. These requirements can be met by adding compensation components around the error amplifier to modify the total loop response.

Therefore, the error amplifier design should provide the following:

- A pole at dc to give high low-frequency gain
- Two zeroes near the filter poles to correct for phase shift due to the power stage frequency response
- Two additional poles to roll off high frequency gain

The compensation circuit shown in Figure 2–3 is used to implement the above functions.

Figure 2–3. Error-Amplifier Compensation Network



The first step in the design of the error-amplifier frequency response is the design of the output sense divider. This sets the output voltage, and the top resistor, R2, determines the relative impedance of the rest of the compensation design. A 2.32 kΩ resistor for the top of the divider gives a divider current of 0.99 mA for an output setting of 3.3 V. The bottom of the divider (omitted from Figure 2–3 for clarity) is calculated as:

$$R4 = V_{ref} \times \frac{R2}{V_O - V_{ref}} = 1\ V \times \frac{2.32\ k\Omega}{V_O - 1} = 1.008\ k\Omega \Rightarrow 1\ k\Omega$$

The transfer function for the circuit in Figure 2–3 is:

$$\frac{V_{COMP}}{V_O} = (-1) \times \frac{[1 + s \times R5 \times (C11 + C10)] \times [1 + s \times C3 \times (R1 + R2)]}{s \times C11 \times R2 \times [1 + s \times C10 \times R5] \times [1 + s \times C3 \times R1]}$$

$$= \frac{\left(f_{Z1}\right) \times \left(f_{Z2}\right)}{\left(f_{P1}\right) \times \left(f_{P2}\right) \times \left(f_{P3}\right)}$$

The capacitor C11 along with R2 provides the error amplifier pole at dc and also positions the gain at low frequencies. The frequency of the first error amplifier zero, f_{Z1}, is given by:

$$f_{Z1} = \frac{1}{2 \times \Pi \times R5 \times (C11 + C10)} = 5.2\ kHz$$

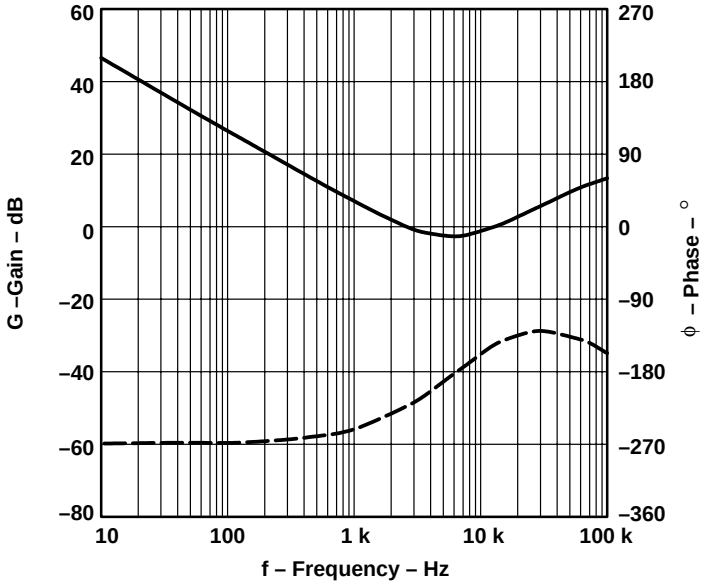
The frequency of the second error amplifier zero, f_{Z2}, is given by:

$$f_{Z2} = \frac{1}{2 \times \Pi \times C3 \times (R1 + R2)} = 6.6\ kHz$$

The two high frequency poles are placed well after the crossover frequency but less than the switching frequency.

For the operating conditions given for Figure 2–2, the unity gain frequency for the control loop is chosen to be approximately 20 kHz. The gain at 20 kHz of the uncompensated loop is about 0 dB. This means that the error-amplifier gain at 20 kHz needs to be 0 dB so that their sum equals 0 dB at 20 kHz. As shown by the graph of the error-amplifier response in Figure 2–4, the error-amplifier design satisfies all the requirements listed on the previous page. The solid line is the gain and the dashed line is the phase.

Figure 2–4. Error-Amplifier Frequency Response



The overall open loop frequency response of the converter is the product of the uncompensated open loop response (Figure 2–2) and the error amplifier response (Figure 2–4). A Bode plot of the overall open loop frequency response of the converter is shown in Figure 2–5. Again, the solid line is the gain and the dashed line is the phase. As seen in the graph, the gain crosses 0 dB in the vicinity of 20 kHz and the phase margin is approximately 100 degrees.

It should be emphasized that the power stage gain and hence the overall loop gain is dependent on input voltage, output voltage, output load resistance, and parasitic resistances present in the power state and external components. Figure 2–5 represents a typical operating condition. However, it is good design practice to check for stability at the line voltage extremes and limits of output voltage settings and loads to ensure that variations do not cause problems.

Figure 2–5. Error-Amplifier Frequency Response