User's Guide

TPS54550 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains background information for the TPS54550 as well as support documentation for the TPS54550EVM-158 evaluation module (HPA158). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54550EVM-158.

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Trademarks

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1 Background

The TPS54550 DC/DC converter is designed to provide up to a 6-A output from an input voltage source of 4.5 V to 20 V. Rated input voltage and output current range for the evaluation module is given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54550 regulator. The maximum EVM input voltage of 17 V, is the result of the 3.3-V output voltage. The switching frequency is internally set at a nominal 700 kHz. The high-side MOSFET is incorporated inside the TPS54550 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54550 to achieve high efficiencies and helps to keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. External compensation components accommodate a wide range of output filter components. Additionally, the TPS54550 provides an enable input. The absolute maximum input voltage is 20 V.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54550EVM-158	VIN = 6 V to 17 V	0 A to 5 A

2 Performance Specification Summary

A summary of the TPS54550EVM-158 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54550EVM-158 is designed and tested for V_{IN} = 6 V to 17 V. The ambient temperature is 25°C for all measurements, unless otherwise noted. Maximum input voltage for the TPS54550EVM-158 is 20 V.

Table 2-1. TPS54550EVM-158 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN voltage range			6	12 or 15	17	V
Output voltage set point				3.3		V
Output current range		V_{IN} = 10 V to 17 V	0		5	A
Line regulation		I_O = 0 2.5 A, V_{IN} = 10 V - 17 V		+0.08 -0.03%		
Load regulation		V_{IN} = 12 V, I_O = 0 A to 5 A		+0.07 -0.01%		
Load transient response	Voltage change	I_O = 1.25 A to 3.75 A		-72.5		mV
	Recovery time			450		µs
	Voltage change	I_O = 3.75 A to 1.25 A		+72.5		mV
	Recovery time			450		µs
Loop bandwidth		V_{IN}= 12 V, I_O = 2.5 A		27		kHz
Phase margin		V_{IN} = 12 V, I_O = 2.5 A		62		°
Input ripple voltage		V_{IN} = 7 V, I_O = 5 A		276	300	mVpp
Output ripple voltage		V_{IN} = 7 V, I_O = 5 A		7		mVpp
Output rise time				5		ms
Operating frequency				700		kHz
Max efficiency		V_{IN} = 6 V, V_O = 3.3 V, I_O = 1.25 A		93.5%		

3 Modifications

The TPS54550EVM-158 is designed to demonstrate the small size that can be attained when designing with the TPS54550. A few changes can be made to this module.

3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R2. Changing the value of R2 can change the output voltage above 0.891 V. The value of R2 for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V} \quad (1)$$

Table 3-1 lists the R2 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 220 ns, and the maximum duty cycle is less than 80%. The values given in Table 3-1 are standard values, not the exact value calculated using Equation 1.

Table 3-1. Output Voltages Available

OUTPUT VOLTAGE (V)	R_2 VALUE (kΩ)
1.8	9.76
2.5	5.49
3.3	3.74
5	2.15

3.2 Input Voltage Range

The EVM is designed to operate from a nominal 12 V or 15 V with a working operating range of 6-V to 17-V input voltage. The TPS54550 is specified to operate over an input voltage range of 4.5 V to 20 V. The upper voltage limit of 17 V is due to minimum on time restrictions to guarantee 3.3-V output.

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54550EVM-158 evaluation module. The section also includes test results typical for the TPS54550EVM-158 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

4.1 Input / Output Connections

The TPS54550EVM-158 is provided with input/output connectors and test points as shown in Table 4-1. Connect a power supply capable of supplying 3 A to J1 through a pair of 20 AWG wires. The load should be connected to J3 through a pair of 20 AWG wires. The maximum load current capability should be 5 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the VIN input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

Table 4-1. EVM Connectors and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	VIN, 12 V nominal, 6 V to 17 V
J2	OUT, 5 V at 5 A maximum
J3	2-pin header for bi-directional synchronization signal.
J4	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	VIN test point at VIN connector
TP2	GND test point at VIN
TP3	Output voltage test point at OUT connector
TP4	GND test point at OUT connector
TP5	Test point between voltage divider network and R3. Used for loop response measurements.
TP6	Test point on power-good pullup resistor. Tie to 3.3 V or 5 V if power-good signal is used.
TP7	Test point for power good.
TP8	Test point for external UVLO.
TP9	Test point for timing resistor.

4.2 Efficiency

The TPS54550EVM-158 efficiency peaks at load current of about 1 A to 3 A, depending on input voltage, and then decreases as the load current increases towards full load. Figure 4-1 shows the efficiency for the TPS54550EVM-158 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs.

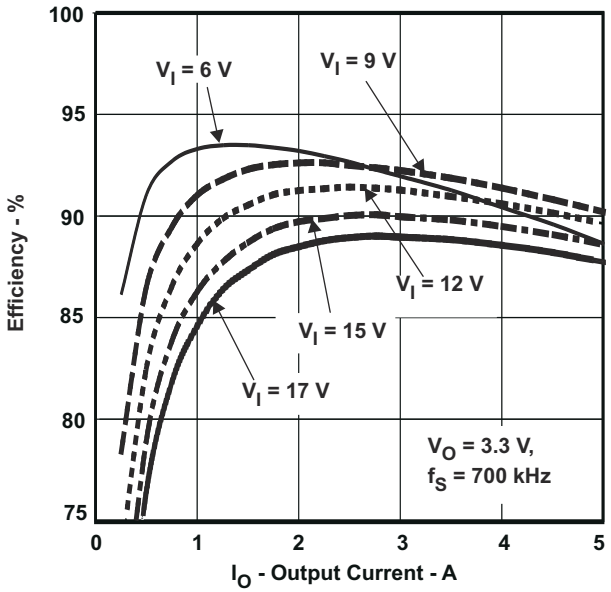

Figure 4-1. Measured Efficiency, TPS54550

4.3 Output Voltage Regulation

The output voltage load regulation of the TPS54550EVM-158 is shown in Figure 4-2; the output voltage line regulation is shown in Figure 4-3. Measurements are given for an ambient temperature of 25°C.

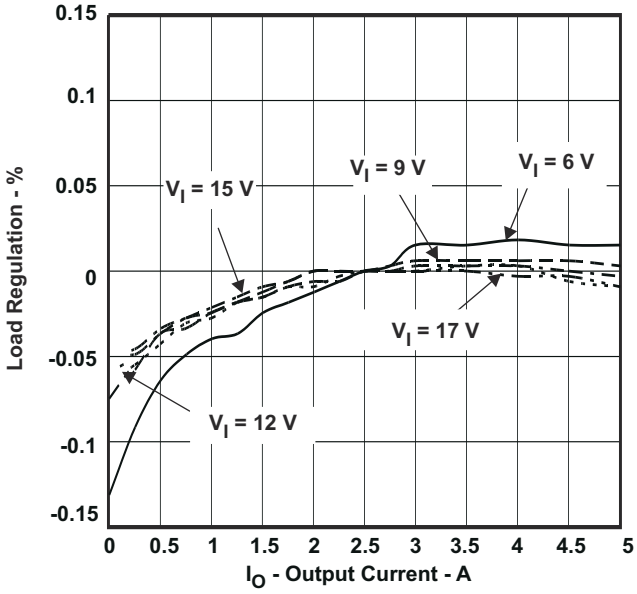

Figure 4-2. Load Regulation

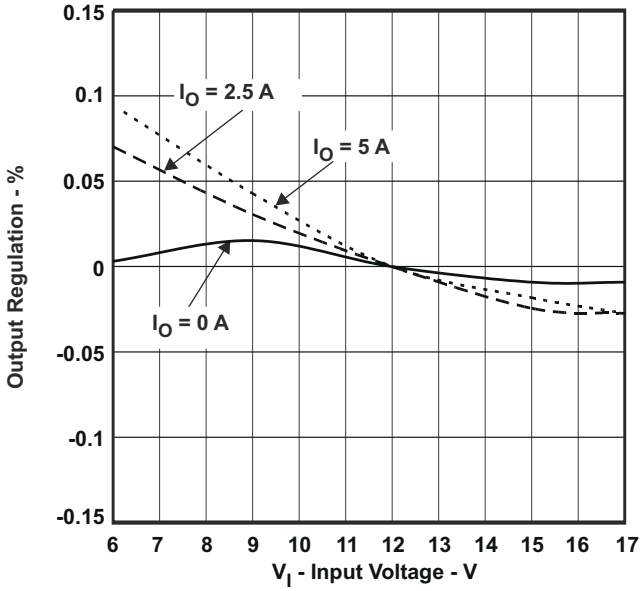

Figure 4-3. Line Regulation

4.4 Load Transients

The TPS54550EVM-158 response to load transients is shown in Figure 4-4. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

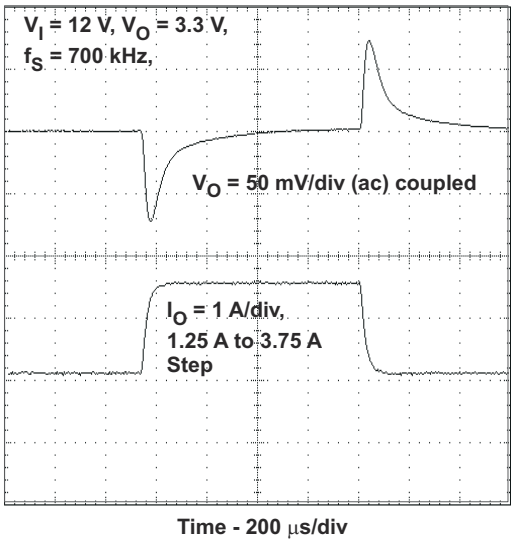

Figure 4-4. Load Transient Response, TPS54550

4.5 Loop Characteristics

The TPS54550EVM-158 loop-response characteristics are shown in Figure 4-5. Gain and phase plots are shown for VIN voltage of 12 V and load current of 2.5 A.

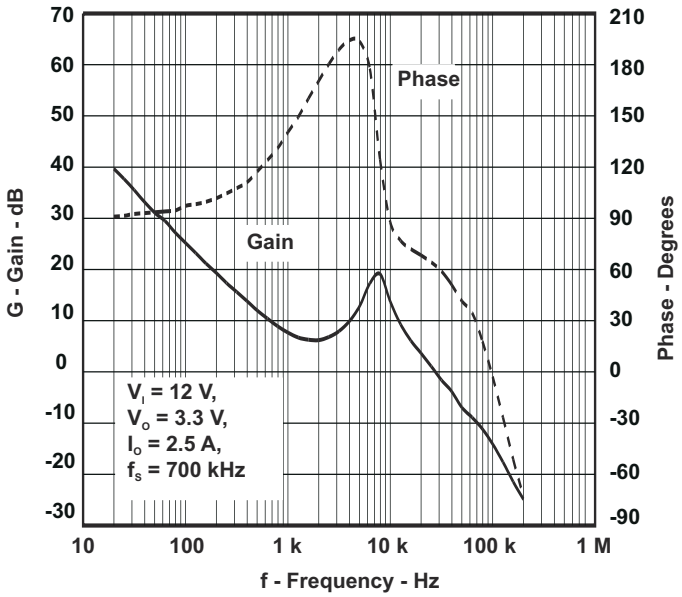

Figure 4-5. Measured Loop Response, TPS54550, V_{IN} = 12 V

4.6 Output Voltage Ripple

The TPS54550EVM-158 output voltage ripple is shown in Figure 4-6. The input voltage is V_{IN} = 12 V for the TPS54550. Output current is the rated full load of 5 A. Voltage is measured directly across output capacitors.

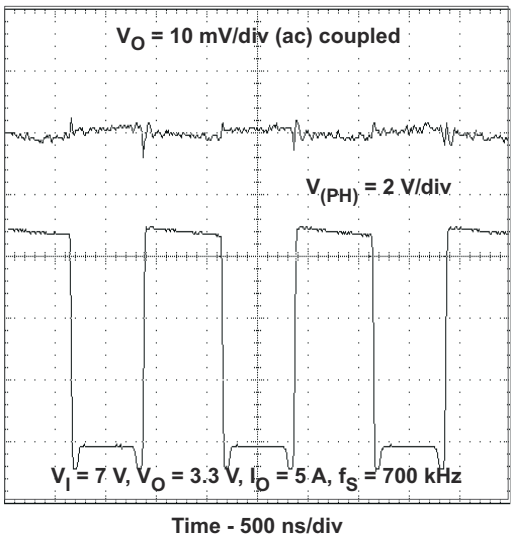

Figure 4-6. Measured Output Voltage Ripple, TPS54550

4.7 Input Voltage Ripple

The input voltage ripple is shown in Figure 4-7. The input voltage is V_{IN} = 12 V for the TPS54550. Output current for each device is at full rate TPS54550EVM-158 load of 5 A.

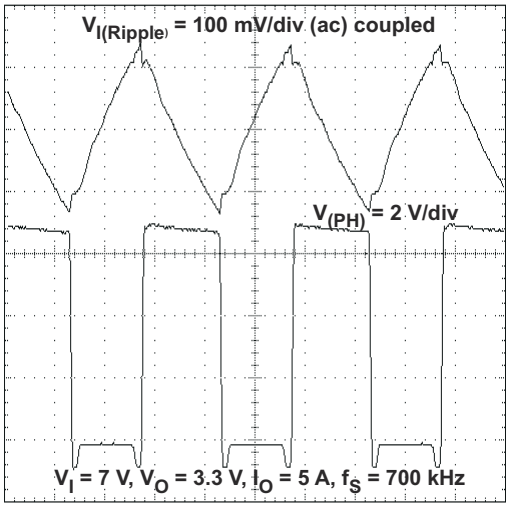

Figure 4-7. Input Voltage Ripple, TPS54550

4.8 Powering Up

The TPS54550EVM-158 start-up waveforms are shown in Figure 4-8. The top trace shows V_{IN} whereas the bottom trace shows OUT. Vin charges up from 0 V toward 12 V. When the input voltage reaches the internally set UVLO threshold voltage, the slow-start sequence begins. After a delay, the internal reference begins to ramp up linearly at the internally set slow-start rate towards 0.891 V, and the output ramps up toward the set voltage of 5 V. The output may be inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released and the slow-start voltage begins to ramp up at the internally set rate. When the EN voltage reaches the enable-threshold voltage of 1.06 V, the start-up sequence begins as described previously.

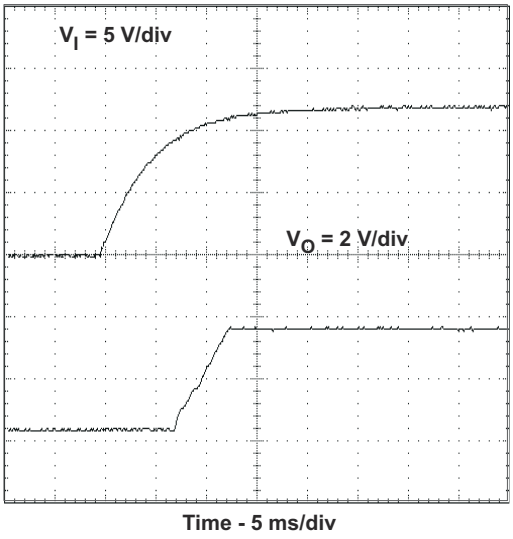

Figure 4-8. Power Up, OUT Relative to V_{IN}

5 Board Layout

This section provides a description of the TPS54550EVM-158 board layout and layer illustrations.

5.1 Layout

The board layout for the TPS54550EVM-158 is shown in Figure 5-1 through Figure 5-3. The topside layer of the TPS54550EVM-158 is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for VIN, OUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54550 and a large area filled with ground. The bottom layer contains ground and some signal routing. The top and bottom and internal ground traces are connected with multiple vias placed around the board including four vias directly under the TPS54550 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitor (C1) and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the voltage setpoint resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, adjacent to the output capacitor C3.

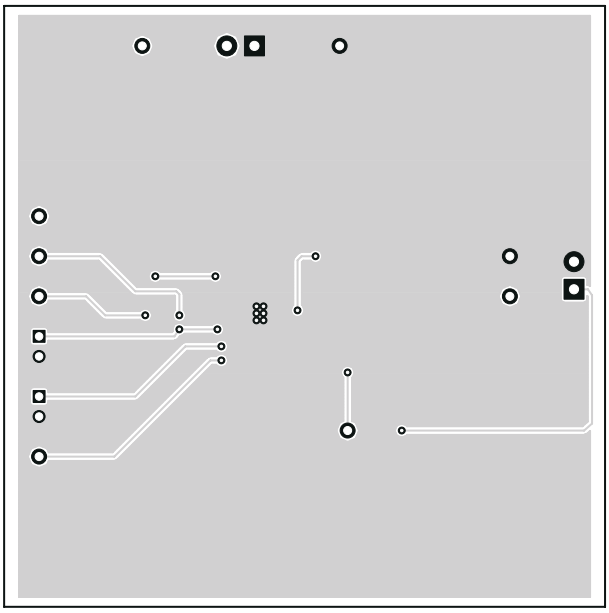

Figure 5-1. Top-Side Layout

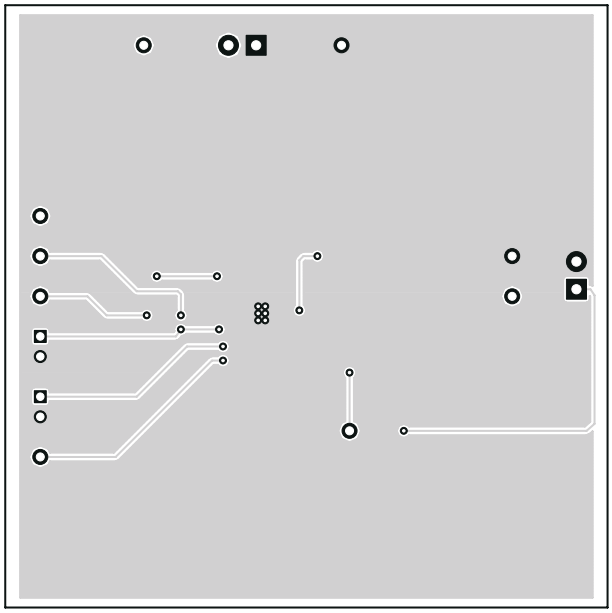

Figure 5-2. Bottom-Side Layout (Looking From Top Side)

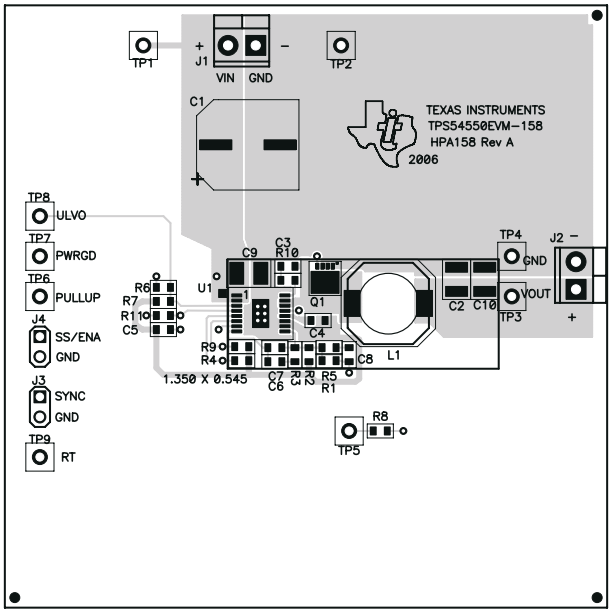

Figure 5-3. Top-Side Assembly

6 Schematic and Bill of Materials

The TPS54550EVM-158 schematic and bill of materials are presented in this section.

6.1 Schematic

The schematic for the TPS54550EVM-158 is shown in Figure 6-1.

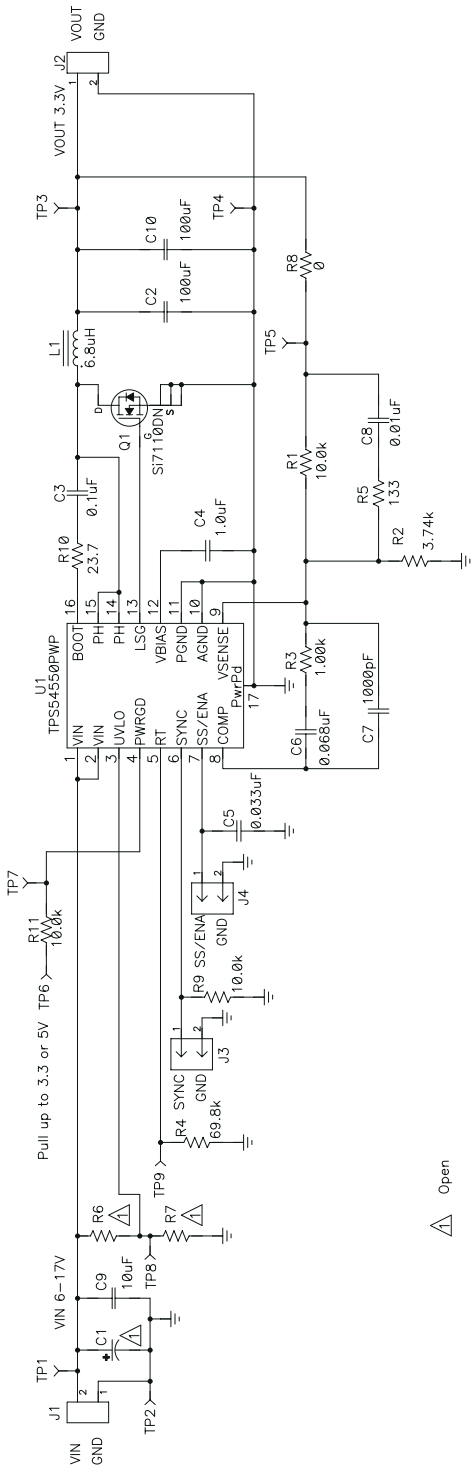

Figure 6-1. TPS54550EVM-158 Schematic

6.2 Bill of Materials

The bill of materials for the TPS54550EVM-158 is given by Table 6-1.

Table 6-1. TPS54550EVM-158 Bill of Materials

Count	REF DES	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, Aluminum, SM	10 × 12mm		
2	C2, C10	100 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	C3225X5R0J107M	TDK
1	C3	0.1 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E104KB	TDK
1	C4	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105KB	TDK
1	C5	0.033 µF	Capacitor, Ceramic, 50V, X5R, 10%	0603	C1608X5R1H333KB	TDK
1	C6	0.068 µF	Capacitor, Ceramic, 50V, X5R, 10%	0603	C1608X5R1H683KT	TDK
1	C7	1000pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H102JB	TDK
1	C8	0.01 µF	Capacitor, Ceramic, 50V, X5R, 10%	0603	C1608X5R1H103KB	TDK
1	C9	10 µF	Capacitor, Ceramic, 16V, X5R, 20%	1210	C3225X5R1C106M	TDK
2	J1, J2		Terminal Block, 2 pin, 6A, 3,5 mm	0.27 × 0.25	ED1514	OST
2	J3, J4		Header, 2 pin, 100 mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
1	L1	6.8 µH	Inductor, SMT, 5.4A, 14 mΩ	0.405 sq inch	CDRH105R-6R8	Sumida
1	Q1		MOSFET, Fast Switching, NChan, 20V, 21.1A, 5.3 mΩ	PWRPAK 1212	Si7110DN	Vishay
3	R1, R9, R11	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	23.7	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	3.74k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	1.00k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	69.8k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	133	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R6, R7		Open Resistor, Chip, 1/16W, 1%	0603		
1	R8	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
7	TP1, TP3, TP5, TP6–TP9		Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keystone
2	TP2, TP4		Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100	5001	Keystone
1	U1		IC, 4.5 to 20V Input, 6A Step down converter with adjustable output voltage	PWP16	TPS54550PWP	TI
1	–		PCB, 3 In × 3 In × 0.062 In		HPA158	Any

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2006) to Revision A (August 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 3
- Updated the user's guide title..... 3

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