User's Guide

TPSM63606(S) 36-V, 6-A Buck Regulator Evaluation Module User's Guide

ABSTRACT

With an input operating voltage range from 3 V to 36 V and rated output current from 2 A to 6 A, the TPSM63602, TPSM63603, TPSM63604, and TPSM63606 family of synchronous buck power modules outlined in Table 1-1 provides flexibility, scalability, and optimized solution size for a wide range of applications. With intergrated power MOSFETs, buck inductor and PWM controller, these modules enable DC/DC solutions with high density, low EMI, and increased flexibility. Available EMI mitigation features include pseudorandom spread spectrum (PRSS), RBOOT-configured switch-node slew rate control, and integrated input bypass capacitors. All modules are rated for ambient and junction temperatures up to 105°C and 125°C, respectively.

Table 1-1. TPSM63602, TPSM63603, TPSM63604, and TPSM63606 Synchronous Buck DC/DC Power Module Family

DC/DC MODULE	RATED I_{OUT}	PACKAGE	DIMENSIONS	FEATURES	EMI MITIGATION
TPSM63602	2 A	B0-QFN (30)	6.0 × 4.0 × 1.8 mm	RT adjustable F_{SW}, external synchronization	PRSS, slew-rate control, integrated input, VCC and BOOT capacitors
TPSM63603	3 A				
TPSM63604	4 A	B3-QFN (20)	5.5 × 5.0 × 4.0 mm		
TPSM63606	6 A				

The TPSM63606EVM and TPSM63606SEVM use the TPSM63606(S) – a compact, easy-to-use synchronous buck module IC with a wide output voltage range of 1 V to 16 V and an output current up to 6 A. The default output voltage of the EVM is 5 V and is adjustable using jumper settings to the following voltages as needed:

- 1.8 V
- 2.5 V
- 3.3 V
- 12 V

The solution supports adjustable input voltage UVLO for application-specific power-up and power-down requirements, external clock synchronization to mitigate beat frequencies in noise-sensitive applications, and a PGOOD indicator for sequencing and output voltage monitoring.

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1 High-Density EVM Description

The TPSM63606EVM features the TPSM63606 synchronous buck power module configured for operation with typical 3-V to 36-V input bus applications (the TPSM63606SEVM features the TPSM63606S, where S denotes pseudo-random spread spectrum frequency modulation). This wide-V_{IN} range DC/DC solution offers outsized voltage rating and operating margin to withstand supply-rail voltage transients.

The output voltage and switching frequency can each be set to one of five popular values by using configuration jumpers. The EVM provides the full 6-A output current rating of the device. The selected input and output capacitors accommodate the entire range of input voltage and the selectable output voltages on the EVM and are available from multiple component vendors. Input and output voltage sense terminals and a test point header facilitate measurement of the following:

- Efficiency and power dissipation
- Line and load regulation
- Load transient response
- Enable ON/OFF
- Bode plot (crossover frequency and phase margin)

The header also provides connections for enable (EN), external clock synchronization (SYNC), and power-good (PGOOD) features of the device. The recommended PCB layout maximizes thermal performance and minimizes output ripple and noise. The schematic and layout are the same for the TPSM63606EVM and TPSM63606SEVM. The only difference is the module IC.

1.1 Typical Applications

- Test and measurement, aerospace and defense
- Factory automation and control, general-purpose power supplies
- Inverting buck-boost (IBB) circuits requiring negative output voltage

1.2 Features and Electrical Performance

- Complete 6-A buck power stage with integrated power MOSFETs, buck inductor, and PWM controller
- Wide input voltage operating range of 3 V to 36 V (absolute maximum rating of 42 V)
- Default output voltage and switching frequency of 5 V and 1 MHz, respectively. Use jumper options for alternative configurations:
  - 1.8 V, 500 kHz
  - 2.5 V, 500 kHz
  - 3.3 V, 750 kHz
  - 12 V, 2 MHz
- High efficiency across a wide load-current range
  - Full-load efficiency of 92% and 91.4% at V_{IN} = 12 V and 24 V, respectively
  - 95% and 93.5% efficiencies at half-rated load, V_{IN} = 12 V and 24 V, respectively
  - External bias option reduces no-load supply current and enhances thermal performance
- Improved EMI performance for noise-sensitive applications
  - Meets CISPR 11 and CISPR 32 Class B EMI standards for both conducted and radiated emissions
  - Input π-stage EMI filter with electrolytic capacitor for parallel damping
  - Parallel input and output paths with symmetrical capacitor layouts minimize radiated field coupling
  - Clock synchronization and FPWM mode provide constant switching frequency across the full load range
  - Integrated input, VCC, and bootstrap capacitors enable low-noise switching performance
  - The TPSM63606SEVM includes pseudo-random spread spectrum (PRSS) for lower peak emissions
- Peak current-mode control architecture enables fast line and load transient response
  - Integrated loop compensation and frequency-proportional slope compensation
- Inherent protection features for robust and reliable design
  - Overcurrent protection (OCP) with peak and valley current limits
  - Thermal shurdown protection with hysteresis
  - PGOOD indicator with 49.9-kΩ pullup resistor to VOUT
  - Resistor-programmable input voltage UVLO set to turn on and off at V_{IN} of 5.1 V and 3.65 V, respectively
- Fully assembled, tested and proven 4-layer PCB design with 76-mm × 63-mm total footprint

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2 EVM Performance Specifications

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 6 A and F_{SW} = 1 MHz

Table 2-1. Electrical Performance Specifications

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Operating		4		36	V
Input voltage turn-on, $V_{IN(on)}$	Adjusted using EN divider resistors			5.1		
Input voltage turn-off, $V_{IN(off)}$				3.65		
Input voltage hysteresis, $V_{IN(hys)}$				1.45		
Input current, disabled, $I_{IN(off)}$	V_{EN} = 0 V (with 402-kΩ and 133-kΩ UVLO divider)			45		µA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT} (1)	Adjustable from 1 V to 16 V		4.9	5.0	5.1	V
Output current, I_{OUT}	V_{IN} = 4 V to 36 V (2)		0		6	A
Output voltage regulation, ΔV_{OUT}	Load regulation	I_{OUT} = 0 A to 6 A		0.1%		
	Line regulation	V_{IN} = 6 V to 36 V		0.1%		
Output voltage ripple, $V_{OUT(AC)}$				25		mVrms
Output overcurrent protection, I_{OCP}				8		A
SYSTEM CHARACTERISTICS						
Default switching frequency, $F_{SW(nom)}$	Adjustable from 200 kHz to 2.2 MHz (based on V_{OUT})			1		MHz
Half-load efficiency, η_{HALF} (1)	V_{IN} = 24 V, I_{OUT} = 3 A	V_{OUT} = 2.5 V, F_{SW} = 500 kHz		89.4%		
		V_{OUT} = 3.3 V, F_{SW} = 750 kHz		92.7%		
		V_{OUT} = 5 V, F_{SW} = 1 MHz		93.5%		
		V_{OUT} = 12 V, F_{SW} = 2 MHz		95.7%		
	V_{IN} = 24 V, I_{OUT} = –1.5 A (3)	V_{OUT} = –12 V, F_{SW} = 2 MHz		90.3%		
Full-load efficiency, η_{FULL} (1)	V_{IN} = 24 V, I_{OUT} = 6 A	V_{OUT} = 2.5 V, F_{SW} = 500 kHz		85.7%		
		V_{OUT} = 3.3 V, F_{SW} = 750 kHz		88.5%		
		V_{OUT} = 5 V, F_{SW} = 1 MHz		91.4%		
		V_{OUT} = 12 V, F_{SW} = 2 MHz		94.8%		
	V_{IN} = 24 V, I_{OUT} = –3 A (3)	V_{OUT} = –12 V, F_{SW} = 2 MHz		91.5%		
Ambient temperature, T_A			–40		105	°C
Junction temperature, T_J			–40		125	

(1) The default output voltage and switching frequency of this EVM are 5 V and 1 MHz, respectively. The VLDOIN pin conencts to the output for output voltages of 3.3 V and above. Efficiency and other performance metrics can change based on operating input voltage, load current, switching frequency, external bias voltage, ambient temerature, externally connected output capacitance, and other parameters.

(2) The recommended airflow is 200 LFM when operating at output currents greater than 4 A and switching freqeuncies above 1 MHz.

(3) Configure the EVM as an *IBB topology* with negative output voltage by connecting the input source between the VIN+ and VOUT+ power terminals. The achievable output current is $I_{OUT} = I_{Lmax(DC)} \times (1 - D)$, where $I_{Lmax(DC)}$ = 6 A is the rated DC current of the module's integrated inductor and $D = |V_{OUT}| / (V_{IN} + |V_{OUT}|)$ is the duty cycle.

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3 EVM Photo

Figure 3-1 highlights the buck module power stage and the various connection interfaces associated with the EVM. Use terminal blocks J1 and J2 to connect the input supply and load, respectively. These terminal blocks accept up to 16-AWG wire thickness.

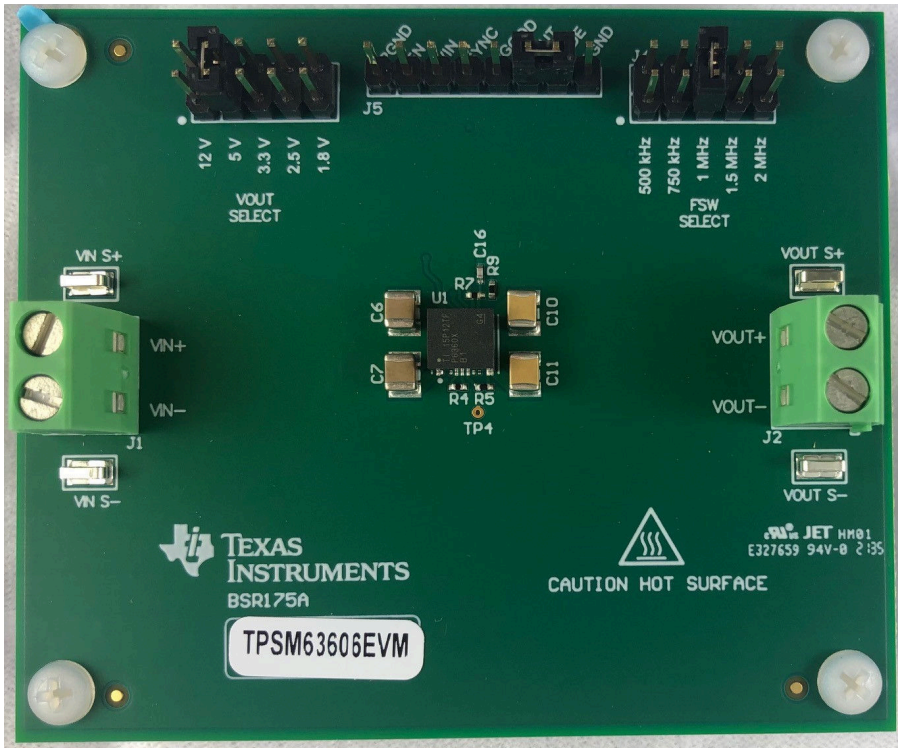

Figure 3-1. TPSM63606(S) EVM Photo

CAUTION

Caution Hot surface.
Contact may cause burns.
Do not touch.

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4 Test Setup and Procedure

4.1 EVM Connections

Referencing the EVM connections described in Table 4-1, use the recommended test setup in Figure 4-1 to evaluate the TPSM63606(S). Working at an ESD-protected workstation, make sure that any wrist straps, bootstraps, or mats are connected and referencing the user to earth ground before power is applied to the EVM.

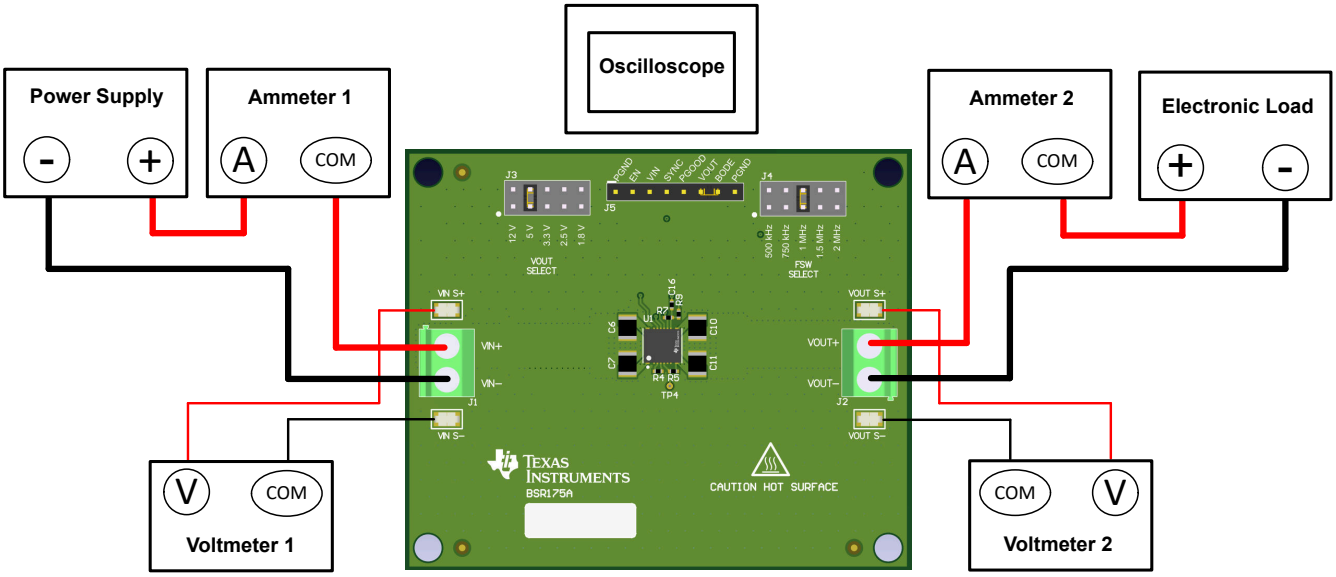

Figure 4-1. EVM Test Setup

Table 4-1. EVM Power Connections

LABEL	DESCRIPTION
VIN+	Positive input power connection
VIN–	Negative input power connection
VOUT+	Positive output power connection
VOUT–	Negative output power connection

Table 4-2. EVM Signal Connections

LABEL(1)	DESCRIPTION
VIN S+	Positive input sense terminal. Connect the multimeter positive lead for measuring efficiency.
VIN S–	Negative input sense terminal. Connect a multimeter negative lead for measuring efficiency.
VOUT S+	Positive output sense terminal. Connect a multimeter positive lead for measuring efficiency and line and load regulation.
VOUT S–	Negative output sense terminal. Connect the multimeter negative lead for measuring efficiency and line and load regulation.
PGND	Ground reference point
EN	Precision enable input and input voltage UVLO protection. Tie EN to GND to disable the regulator. Use a logic signal to control EN for remote ON/OFF functionality. Leave EN open for UVLO turn-on thresholds set at 5.1 V.
SYNC	Synchronization input. Connect a valid clock signal to synchronize the switching frequency from 200 kHz to 2.2 MHz.
PGOOD	Power-good monitor output. This is an open-drain flag with a 49.9-kΩ pullup resistor to VOUT.
BODE, VOUT	Bode plot measurement and signal injection. A 10-Ω resistor from BODE to VOUT facilitates oscillator signal injection for bode plot measurement. Remove the jumper and apply a swept-frequency signal bettwen BODE and VOUT while measuring the respective response at each terminal for loop gain measurement.

(1) Refer to the TPSM63606 data sheet for absolute maximum ratings associated with the features in this table.

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4.2 EVM Setup

- Use the VIN S+ and VIN S– test points along with the VOUT S+ and VOUT S– test points located near the power terminal blocks as voltage monitoring points where voltmeters are connected to measure the input and output voltages, respectively. **Do not use these sense terminals as the input supply or output load connection points.** The PCB traces connected to these sense terminals are not designed to support high currents.
- Header J5 provides access to the following test points:
  - VIN
  - EN
  - SYNC
  - PGOOD
  - VOUT
  - BODE

  The SYNC test point provides a convenient location to connect an external clock signal. The power-good (PGOOD) test point is available to monitor when a valid output voltage is present on the EVM. Refer to Section 4.1 for specific information related to the various test points.
- The **VOUT SELECT** header (J3) allows selection of the required output voltage:
  - 1.8 V
  - 2.5 V
  - 3.3 V
  - 5 V
  - 12 V

  Before applying power to the EVM, make sure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.
- The **FSW SELECT** header (J4) allows selection of a suitable switching frequency:
  - 500 kHz
  - 750 kHz
  - 1 MHz
  - 1.5 MHz
  - 2 MHz

  This establishes an acceptable ripple current for the integrated buck inductor based on the circuit requirements, specifically the input voltage range and output voltage. Before applying power to the EVM, make sure that the jumper is present and properly positioned for the intended switching frequency. Always remove input power before changing the jumper settings.

Note

Choose a switching freqeuency that aligns with the output voltage setting. For example, the following list contains typical settings that yield 30% to 40% inductor peak-to-peak ripple current and optimal slope compensation contribution:

- 2.5 V at 500 kHz
- 3.3 V at 750 kHz
- 5 V at 1 MHz
- 8 V at 1.5 MHz
- 12 V at 2 MHz

Refer to the TPSM63606 data sheet, TPSM63606 Quickstart Calculator and WEBENCH® Power Designer for additional guidance pertaining to module setup and component selection.

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4.3 Test Equipment

Voltage Source: The input voltage source V_{IN} should be a 36-V variable DC source capable of supplying 6 A.

Multimeters:

- **Voltmeter 1:** Measure the input voltage at VIN S+ to VIN S–.
- **Voltmeter 2:** Measure the output voltage at VOUT S+ to VOUT S–.
- **Ammeter 1:** Measure the input current. Set the ammeter to 1-second aperture time.
- **Ammeter 2:** Measure the output current. Set the ammeter to 1-second aperture time.

Electronic Load: Use an electronic load set to constant-resistance (CR) or constant-current (CC) mode and capable of 0 ADC to 6 ADC. For a no-load input current measurement, disconnect the electronic load as it can draw a small residual current.

Oscilloscope: With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this may induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Safety: Always use caution when touching any circuits that can be live or energized.

4.4 Recommended Test Setup

4.4.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 0.1-A maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 4-1.
- Connect voltmeter 1 at VIN S+ and VIN S– connection points to measure the input voltage.
- Connect ammeter 1 to measure the input current and set it to at least a 0.1-second aperture time.

4.4.2 Output Connections

- Connect an electronic load to the VOUT+ and VOUT– connections as shown in Figure 4-1. Set the load to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
- Connect voltmeter 2 at VOUT S+ and VOUT S– sense points to measure the output voltage.
- Connect ammeter 2 to measure the output current.

4.5 Test Procedure

4.5.1 Line/Load Regulation and Efficiency

- Set up the EVM as described in Section 4.
- Set load to constant resistance or constant current mode to sink 0 A.
- Increase the input source voltage from 0 V to 24 V; use voltmeter 1 to measure the input voltage.
- Increase the current limit of the input supply to 6 A.
- Use voltmeter 2 to measure the output voltage, V_{OUT}, and vary the load current from 0 A to 6 A DC; V_{OUT} should remain within the load regulation specification.
- Set the load current to 3 A (50% rated load) and vary the input source voltage from 6 V to 36 V; V_{OUT} should remain within the line regulation specification.
- Set the load current to 6 A (100% rated load) and measure the efficiency at typical input voltages (12 V, 24 V, and 28 V).
- Decrease the load to 0 A. Decrease the input source voltage to 0 V.

CAUTION

Extended operation at high output current can raise component temperatures above 55°C. To avoid risk of a burn injury, do not touch the components until they have cooled sufficiently after disconnecting power. Review the thermal performance plots for more detail.

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5 Test Data and Performance Curves

Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements. Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 6 A, and F_{SW} = 1 MHz.

5.1 Efficiency and Load Regulation Performance

This section provides efficiency and load regulation plots for the EVM.

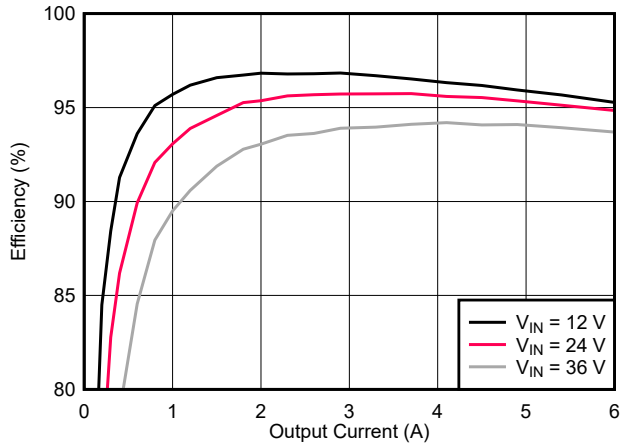

Figure 5-1. Efficiency, V_{OUT} = 12 V, F_{SW} = 2 MHz

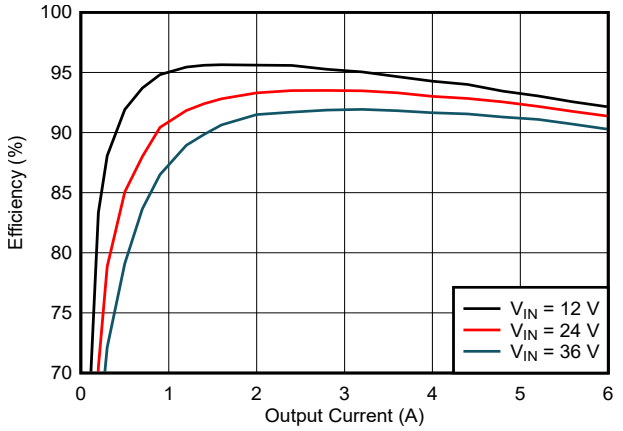

Figure 5-2. Efficiency, V_{OUT} = 5 V, F_{SW} = 1 MHz

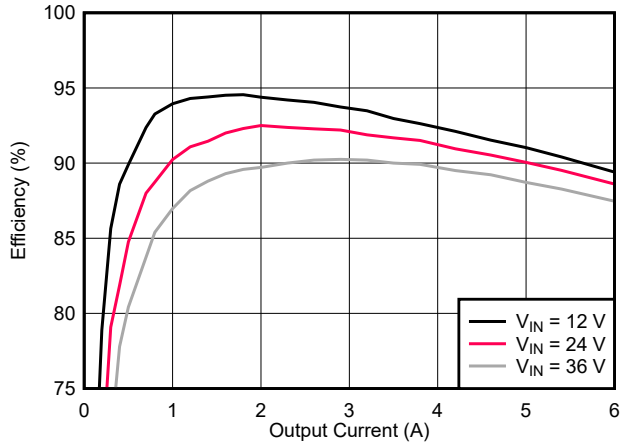

Figure 5-3. Efficiency, V_{OUT} = 3.3 V, F_{SW} = 750 kHz

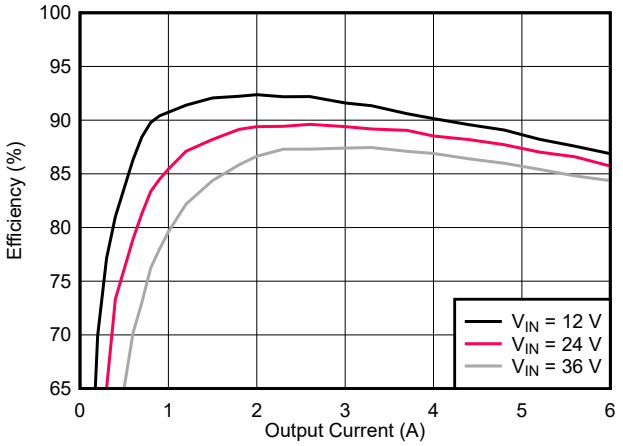

Figure 5-4. Efficiency, V_{OUT} = 2.5 V, F_{SW} = 500 kHz

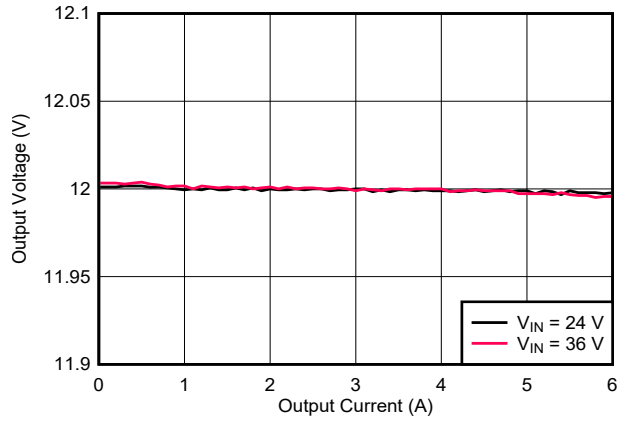

Figure 5-5. Load Regulation, V_{OUT} = 12 V, F_{SW} = 2 MHz

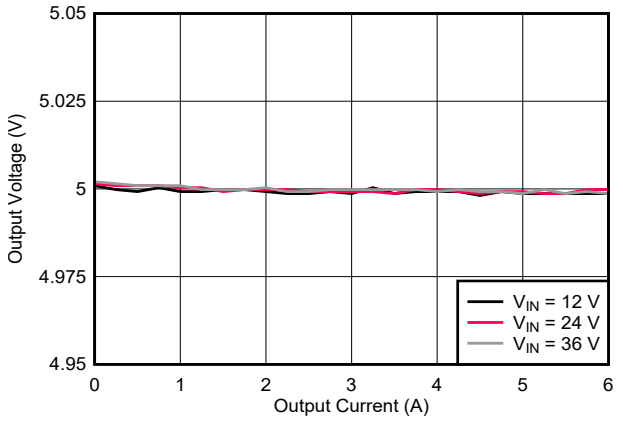

Figure 5-6. Load Regulation, V_{OUT} = 5 V, F_{SW} = 1 MHz

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5.2 Waveforms

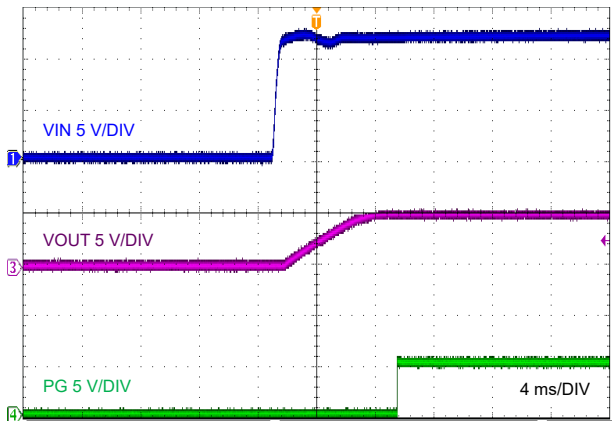

Figure 5-7. Start-Up, V_{IN} Stepped to 12 V

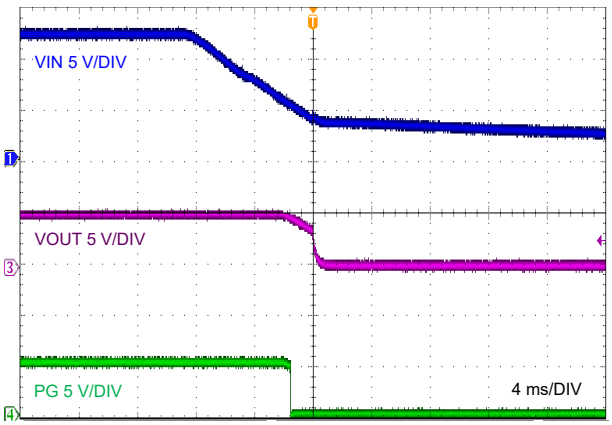

Figure 5-8. Shutdown

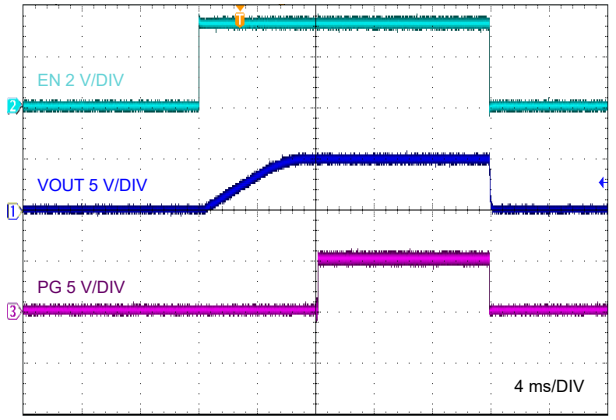

Figure 5-9. Enable ON and OFF

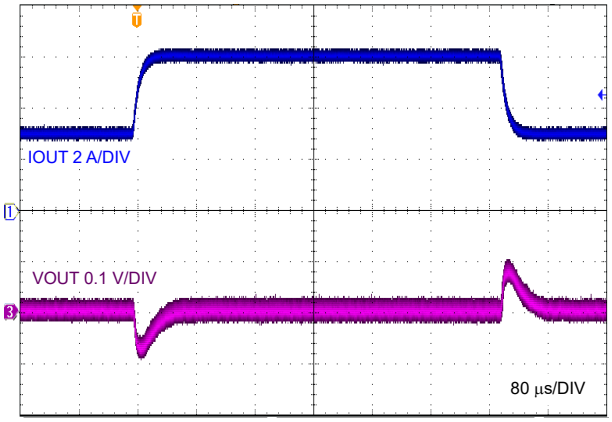

Figure 5-10. Load Transient, 3 A to 6 A at 1 A/µs

5.3 Bode Plot

Figure 5-11 provides the bode plot at V_{IN} = 12 V, V_{OUT} = 5 V and I_{OUT} = 6 A. Figure 5-12 shows a typical capacitance versus voltage curve for a 47-µF, 16-V, X6S output capacitor to highlight the *effective* capacitance value of a ceramic. See component details in Section 6.2.

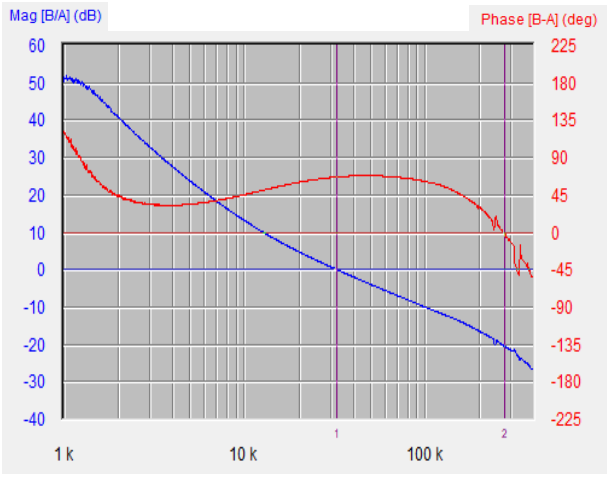

Figure 5-11. Bode Plot with Four 47-µF, 16-V Output Capacitors (110 µF Effective at 5 VDC, 25°C)

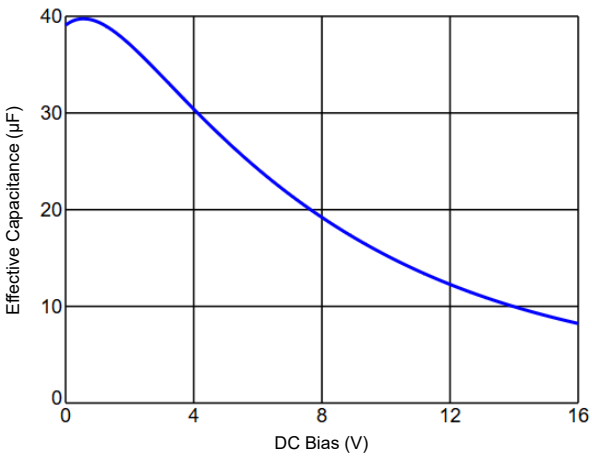

Figure 5-12. Output Capacitor Voltage Derating Curve

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5.4 Thermal Performance

This secton presents (a) thermal images, and (b) derated curves as a function of load current and temperature.

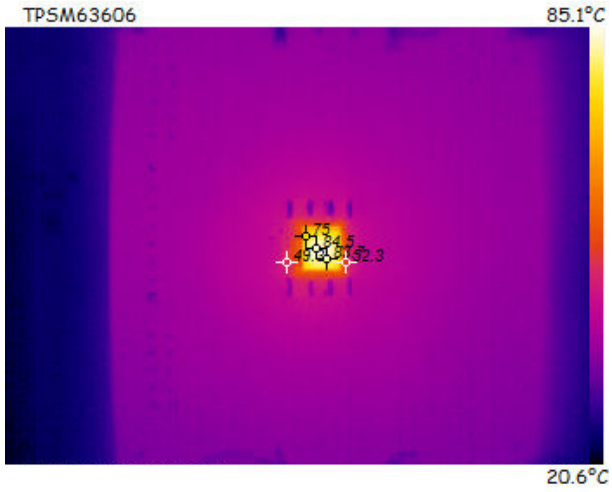

Figure 5-13. Infrared Thermal Image: V_{IN} = 12 V, V_{OUT} = 5.0 V,I_{OUT} = 6 A, F_{SW} = 1 MHz

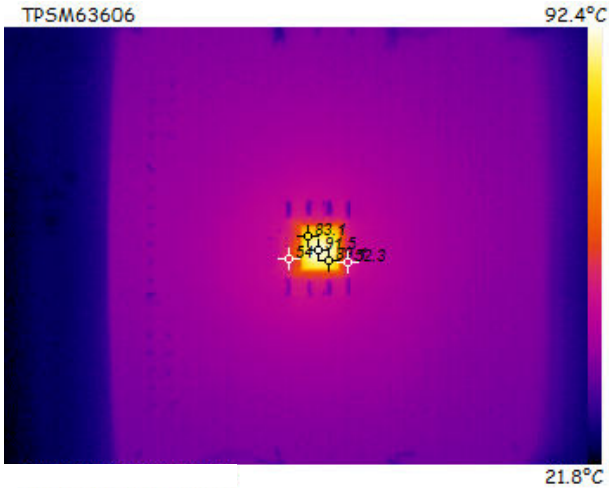

Figure 5-14. Infrared Thermal Image: V_{IN} = 24 V, V_{OUT} = 5.0 V, I_{OUT} = 6 A, F_{SW} = 1 MHz

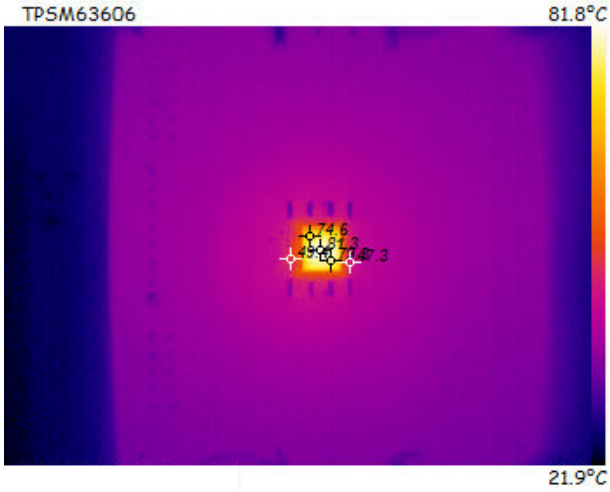

Figure 5-15. Infrared Thermal Image: V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 6 A, F_{SW} = 750 kHz

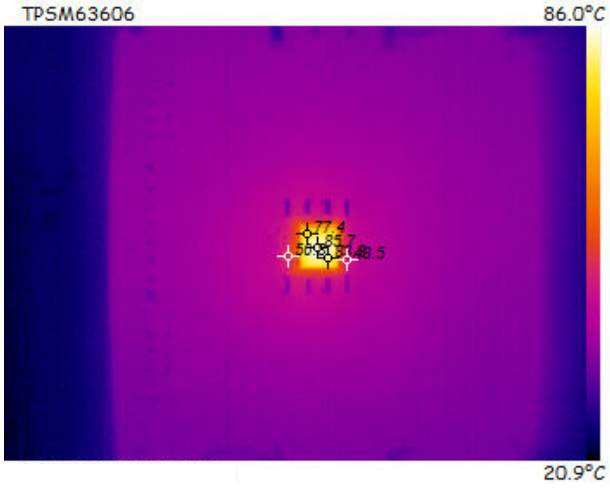

Figure 5-16. Infrared Thermal Image: V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 6 A, F_{SW} = 750 kHz

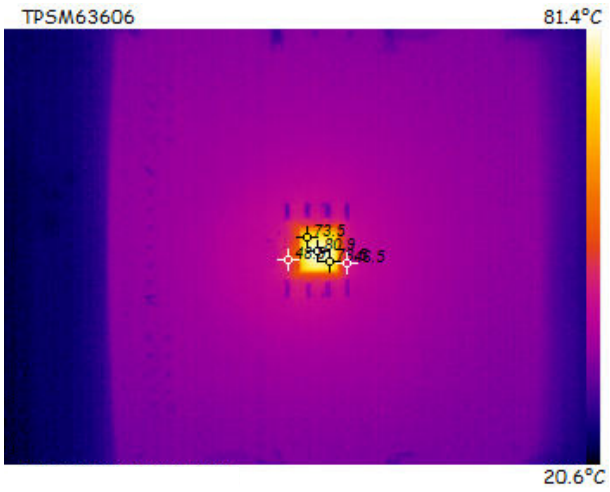

Figure 5-17. Infrared Thermal Image: V_{IN} = 12 V, V_{OUT} = 2.5 V, I_{OUT} = 6 A, F_{SW} = 500 kHz

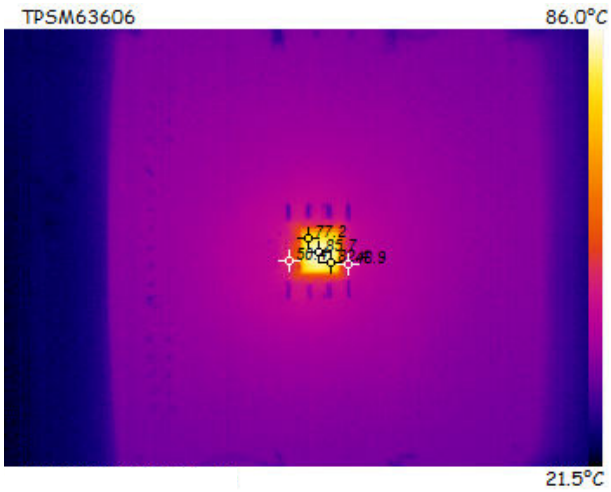

Figure 5-18. Infrared Thermal Image: V_{IN} = 24 V, V_{OUT} = 2.5 V, I_{OUT} = 6 A, F_{SW} = 500 kHz

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5.4 Thermal Performance (continued)

This secton presents (a) thermal images, and (b) derated curves as a function of load current and temperature.

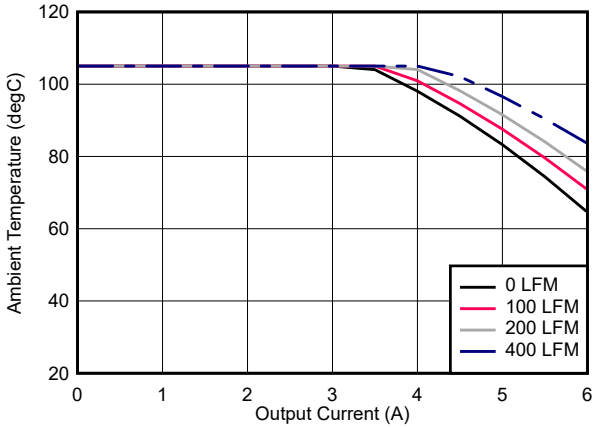

Figure 5-19. Thermal Derating Curve: V_{IN} = 12 V, V_{OUT} = 5.0 V, F_{SW} = 1 MHz

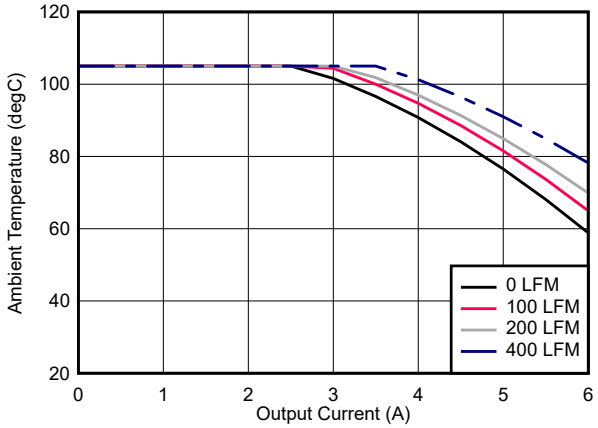

Figure 5-20. Thermal Derating Curve: V_{IN} = 24 V, V_{OUT} = 5.0 V, F_{SW} = 1 MHz

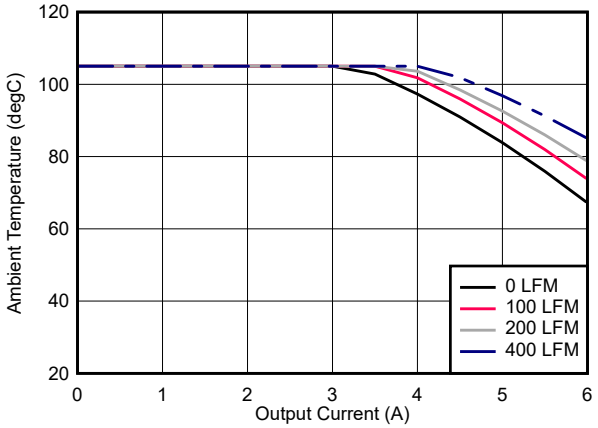

Figure 5-21. Thermal Derating Curve: V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 750 kHz

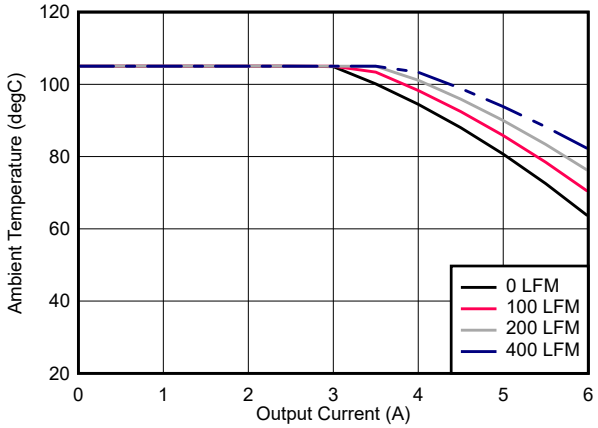

Figure 5-22. Thermal Derating Curve: V_{IN} = 24 V, V_{OUT} = 3.3 V, F_{SW} = 750 kHz

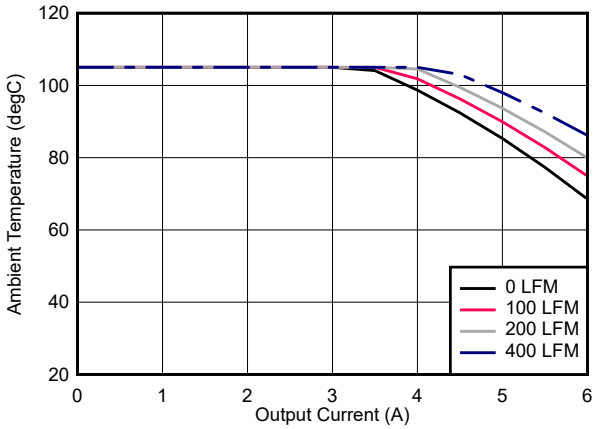

Figure 5-23. Thermal Derating Curve: V_{IN} = 12 V, V_{OUT} = 2.5 V, F_{SW} = 500 kHz

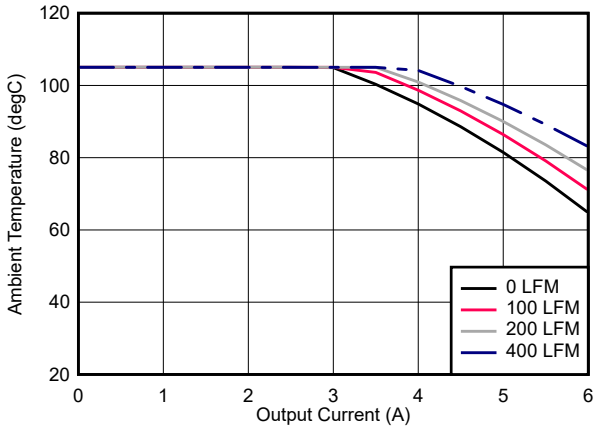

Figure 5-24. Thermal Derating Curve: V_{IN} = 24 V, V_{OUT} = 2.5 V, F_{SW} = 500 kHz

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5.5 EMI Performance

See the Schematic and Bill of Materials for details of the input EMI filter to pass CISPR 32 Class B.

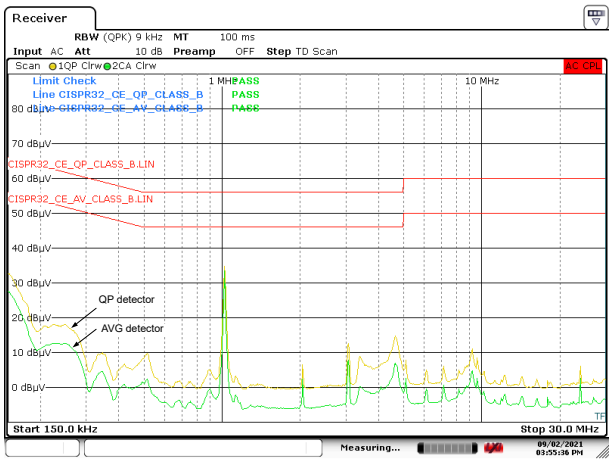

Figure 5-25. CISPR 32 Class B Conducted Emissions: V_{IN} = 12 V, V_{OUT} = 5 V, F_{SW} = 1 MHz

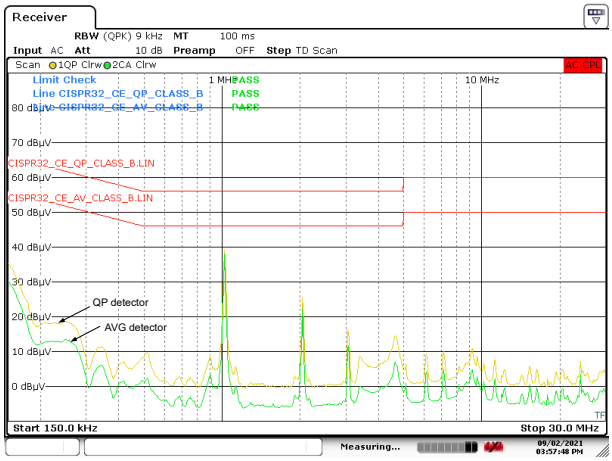

Figure 5-26. CISPR 32 Class B Conducted Emissions: V_{IN} = 24 V, V_{OUT} = 5 V, F_{SW} = 1 MHz

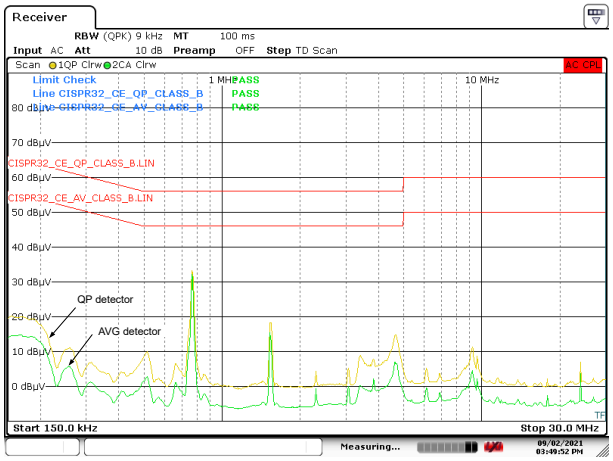

Figure 5-27. CISPR 32 Class B Conducted Emissions: V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 750 kHz

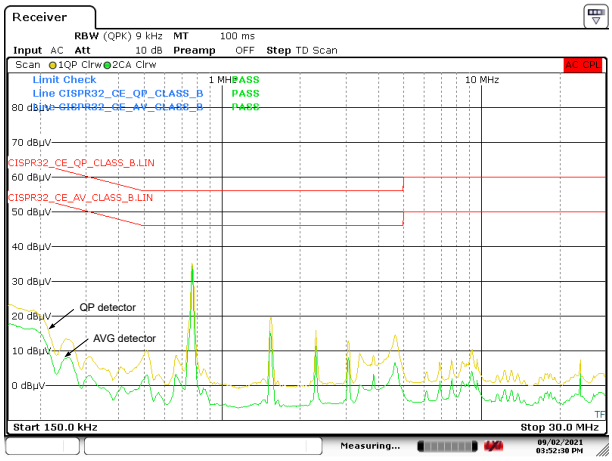

Figure 5-28. CISPR 32 Class B Conducted Emissions: V_{IN} = 24 V, V_{OUT} = 3.3 V, F_{SW} = 750 kHz

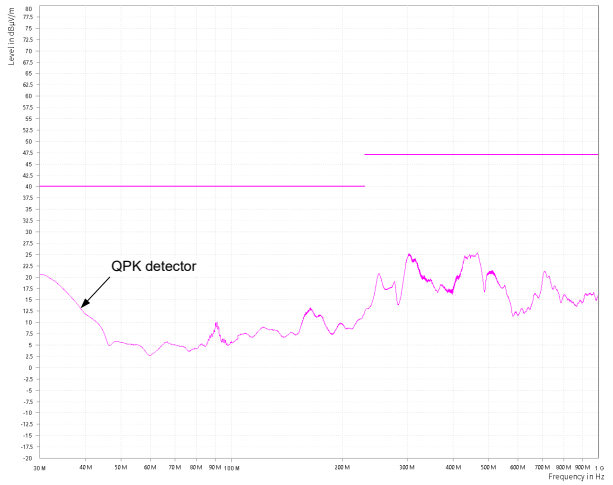

Figure 5-29. CISPR 32 Class B Radiated Emissions: Horizontal Polarization

Figure 5-30. CISPR 32 Class B Radiated Emissions: Vertical Polarization

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6 EVM Documentation

6.1 Schematic

Figure 6-1 illustrates the EVM schematic.

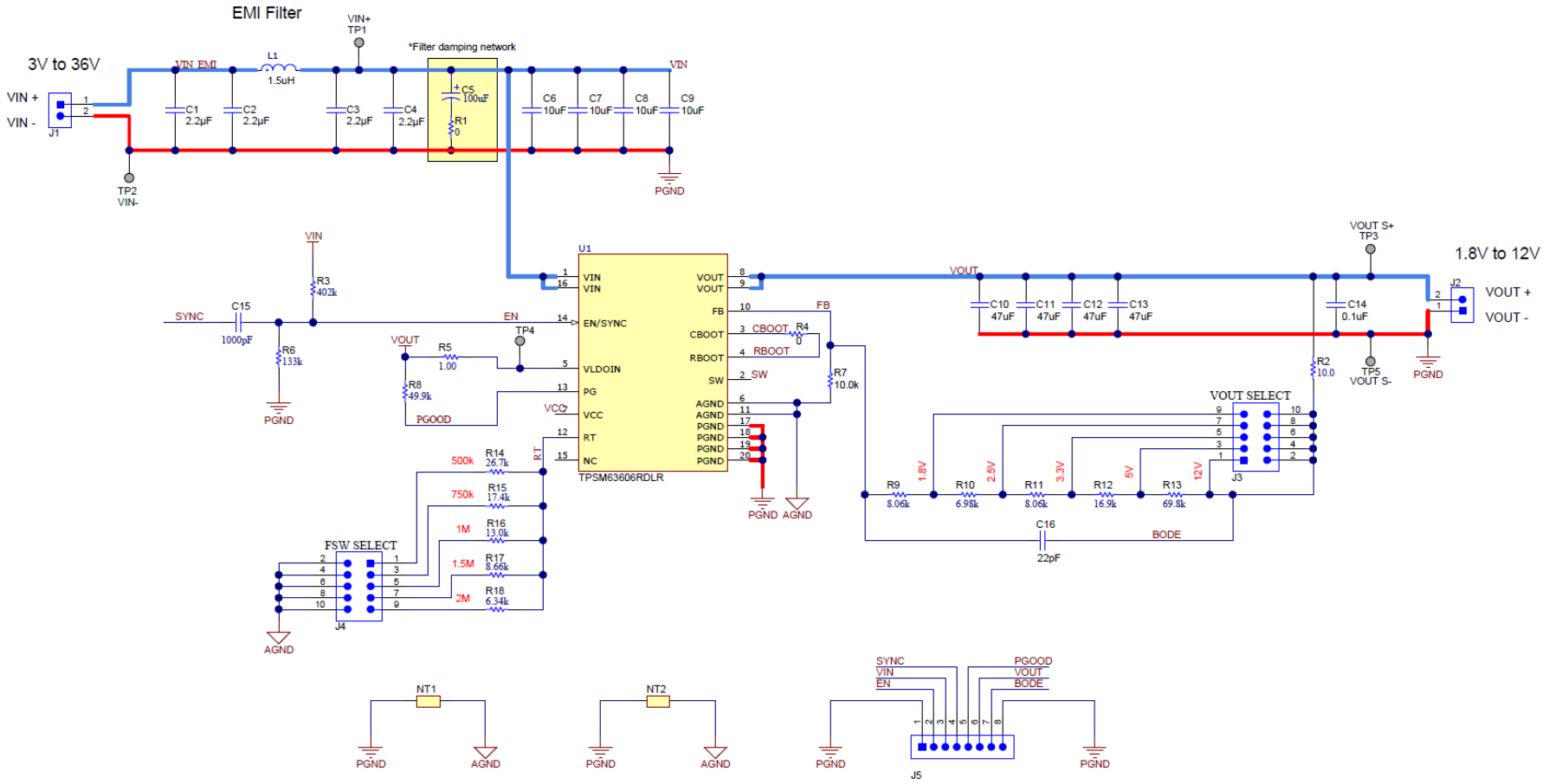

Figure 6-1. EVM Schematic

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6.2 Bill of Materials

Table 6-1. Component BOM

REF DES	QTY	VALUE	DESCRIPTION	PACKAGE	PART NUMBER	MANUFACTURER
C1, C2, C3, C4	4	2.2 µF	CAP, CERM, 2.2 µF, 50 V, X7R	0805	C2012X7R1H225K125AC	TDK
C5	1	100 µF	CAP, AL, 100 µF, 50 V, 0.34 Ω	8 × 10 mm	UUD1H101MNL1GS	Nichicon
C6, C7, C8, C9	4	10 µF	CAP, CERM, 10 µF, 50 V, X7R	1210	GRM32ER71H106KA12L	Murata
C10, C11, C12, C13	4	47 µF	CAP, CERM, 47 µF, 16 V, X6S	1210	GRM32EC81C476ME15L	Murata
C14	1	0.1 µF	CAP, CERM, 0.1 µF, 25 V, X7R	0603	Std	Std
C15	1	1 nF	CAP, CERM, 1 nF, 50 V, X7R	0402	Std	Std
C16	1	22 pF	CAP, CERM, 22 pF, 50 V, 5%, C0G/NP0	0402	Std	Std
H1, H2, H3, H4	4	–	Standoff, Hex, 0.5"L, #4-40, Nylon	–	1902C	Keystone
H5, H6, H7, H8	4	–	Screw, Pan Head, 4-40, 3/8", Nylon	–	NY PMS 440 0038 PH	B&F Fastener Supply
J1, J2	2	–	Terminal block 2 POS 5 mm, TH	–	TSW-110-07-G-S	Phoenix Contact
J3, J4	2	–	Header, 100 mil, 5 × 2, Tin, TH	–	PEC05DAAN	Sullins Connector Solutions
J5	1	–	Header, 100 mil, 8 × 1, Gold, TH	–	TSW-108-07-G-S	Samtec
L1	1	1.5 µH	Shielded power inductor, 1.5 µH, 9.5 mΩ	–	XGL4030-152MEC	Coilcraft
R1	1	0 Ω	RES, 0 Ω, 5%, 0.1 W	0603	Std	Std
R2		10 Ω	RES, 10 Ω, 1%, 0.1 W	0402	Std	Std
R3	1	402 kΩ	RES, 402 kΩ, 1%, 0.063 W	0402	Std	Std
R4	1	0 Ω	RES, 0 Ω, 5%, 0.1 W	0402	Std	Std
R5	1	1 Ω	RES, 1 Ω, 1%, 0.063 W	0402	Std	Std
R6	1	133 kΩ	RES, 133 kΩ, 1%, 0.063 W	0402	Std	Std
R7	1	10 kΩ	RES, 10 kΩ, 1%, 0.063 W	0402	Std	Std
R8	1	49.9 kΩ	RES, 49.9 kΩ, 1%, 0.063 W	0402	Std	Std
R9, R11	2	8.06 kΩ	RES, 8.06 kΩ, 1%, 0.063 W	0402	Std	Std
R10	1	6.98 kΩ	RES, 6.98 kΩ, 1%, 0.063 W	0402	Std	Std
R12	1	16.9 kΩ	RES, 16.9 kΩ, 1%, 0.063 W	0402	Std	Std
R13	1	69.8 kΩ	RES, 69.8 kΩ, 1%, 0.063 W	0402	Std	Std
R14	1	26.7 kΩ	RES, 26.7 kΩ, 1%, 0.063 W	0402	Std	Std
R15	1	17.4 kΩ	RES, 17.4 kΩ, 1%, 0.063 W	0402	Std	Std
R16	1	13 kΩ	RES, 13 kΩ, 1%, 0.063 W	0402	Std	Std
R17	1	8.66 kΩ	RES, 8.66 kΩ, 1%, 0.063 W	0402	Std	Std
R18	1	6.34 kΩ	RES, 6.34 kΩ, 1%, 0.063 W	0402	Std	Std
SH-J1, SH-J2, SH-J3	3	–	Shunt, 100 mil, gold plated, black	Shunt 2 pos. 0.1"	881545-2	TE Connectivity
TP1, TP2, TP3, TP5	4	–	Test point, miniature, SMT	–	5019	Keystone

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Table 6-1. Component BOM (continued)

REF DES	QTY	VALUE	DESCRIPTION	PACKAGE	PART NUMBER	MANUFACTURER
U1	1	–	TPSM63606 36-V, 6-A buck power module	B3QFN-20	TPSM63606RDLR	Texas Instruments
			TPSM63606**S** 36-V, 6-A buck power module **with spread spectrum**		TPSM63606**S**RDLR	

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6.3 PCB Layout

Figure 6-2 through Figure 6-7 show the PCB layout images, including 3D views, copper layers, assembly drawings, and layer stackup diagram. The PCB is 62-mils standard thickness with 2-oz copper on all layers.

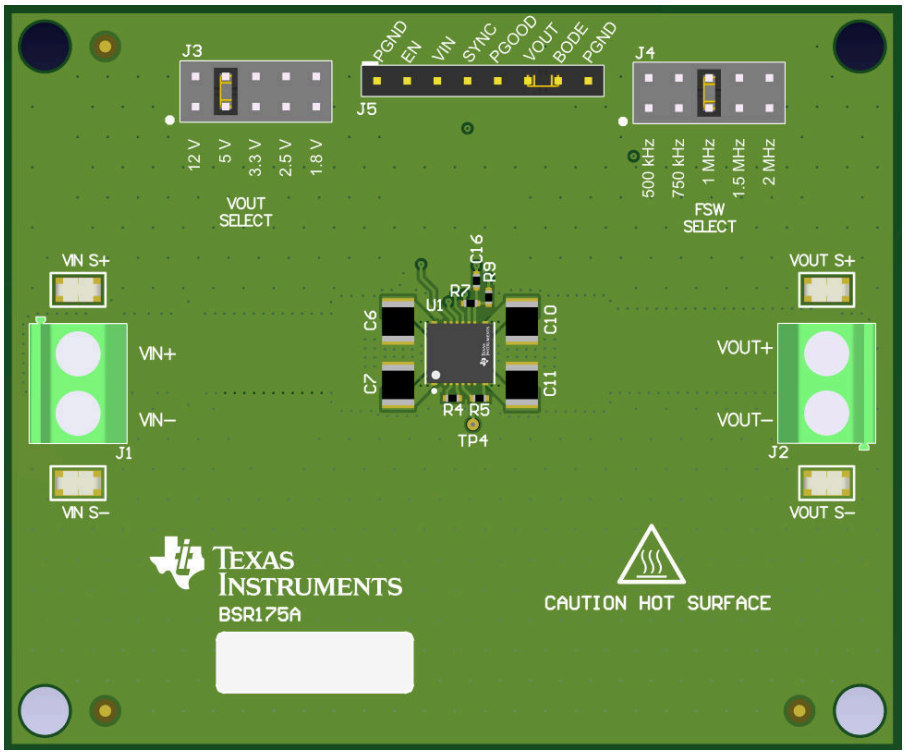

Figure 6-2. 3D Top View

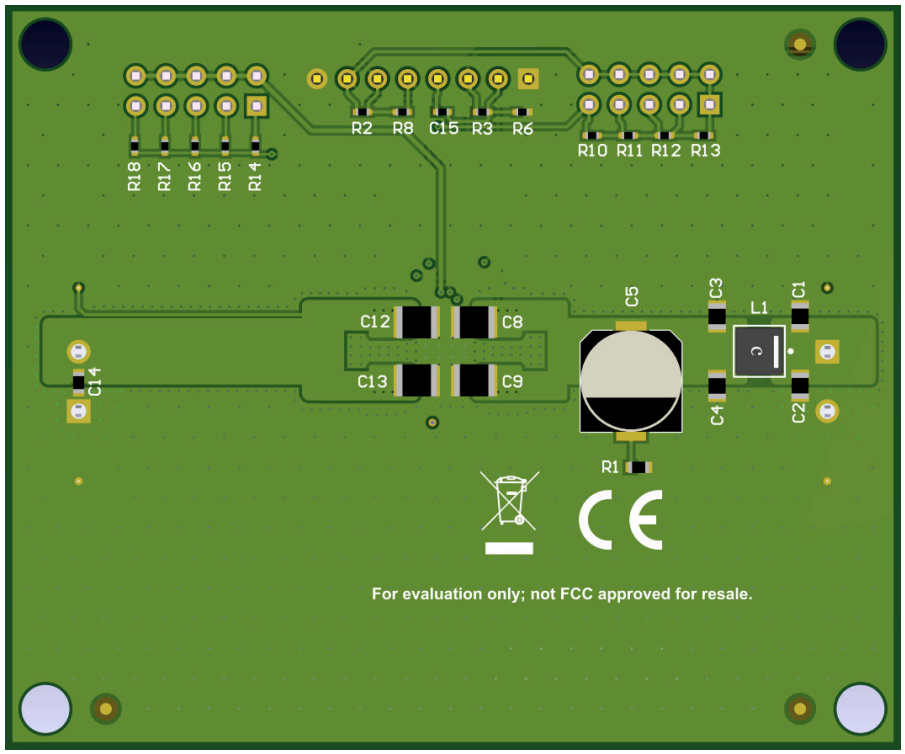

Figure 6-3. 3D Bottom View

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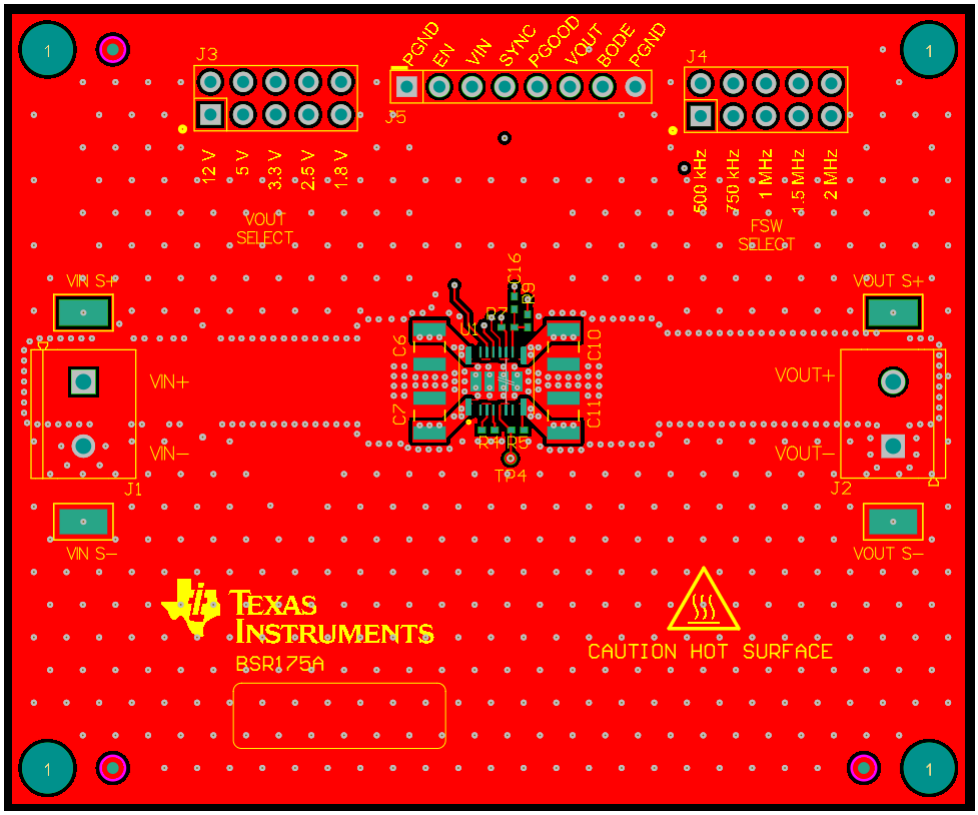

Figure 6-4. Top Layer Copper

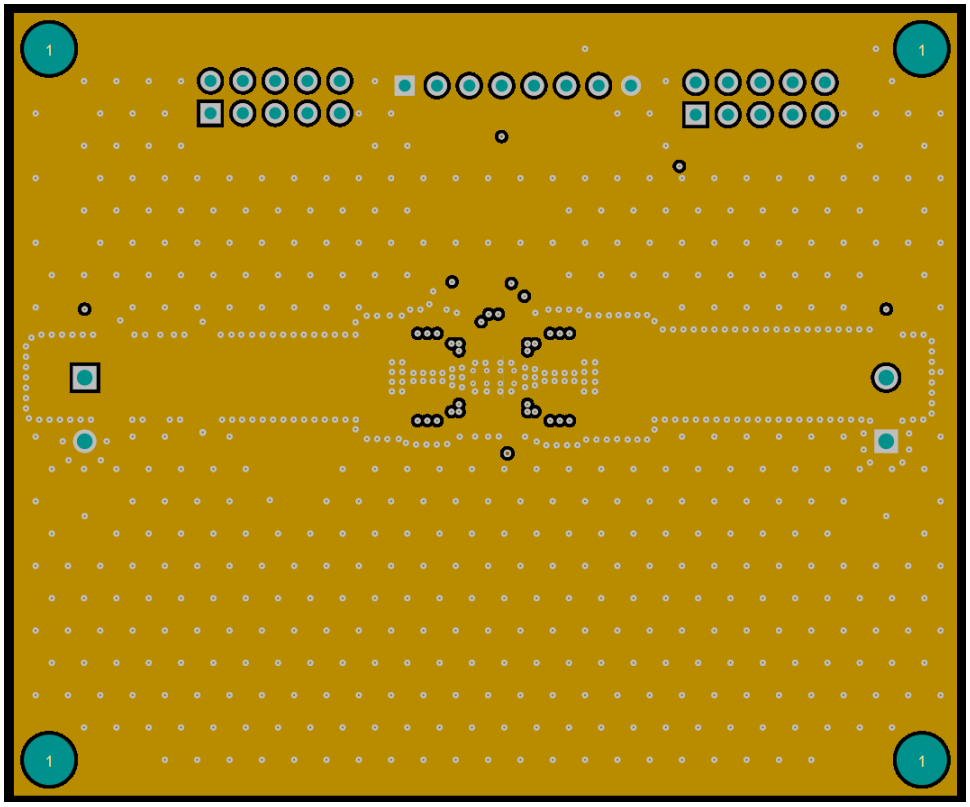

Figure 6-5. Layer 2 Copper

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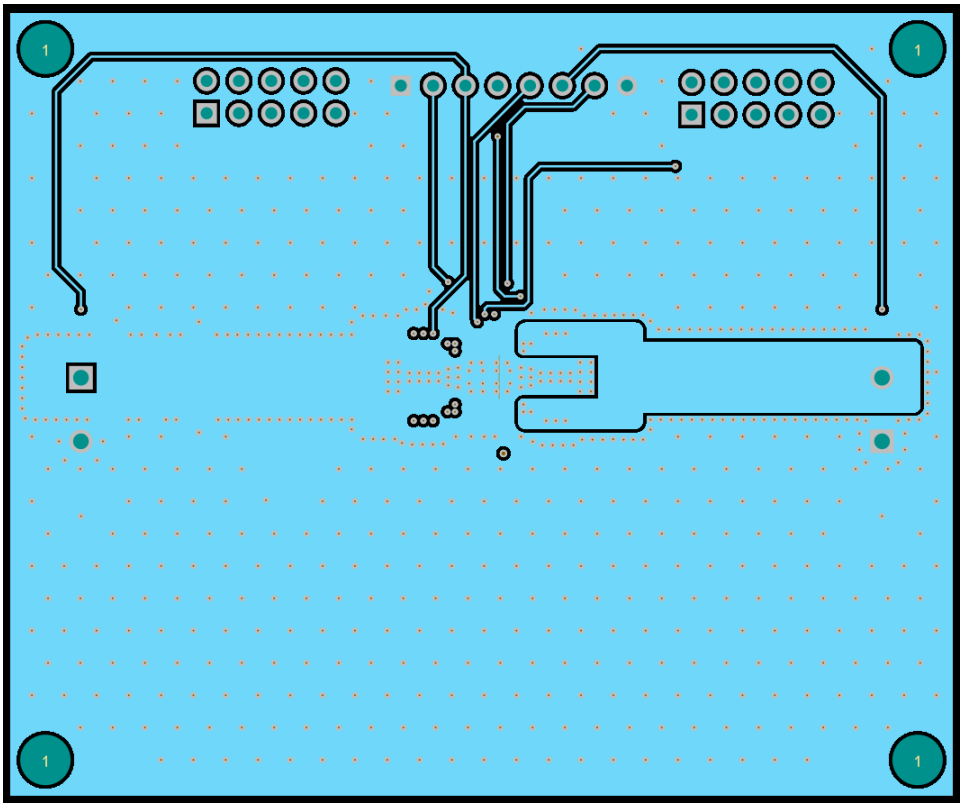

Figure 6-6. Layer 3 Copper

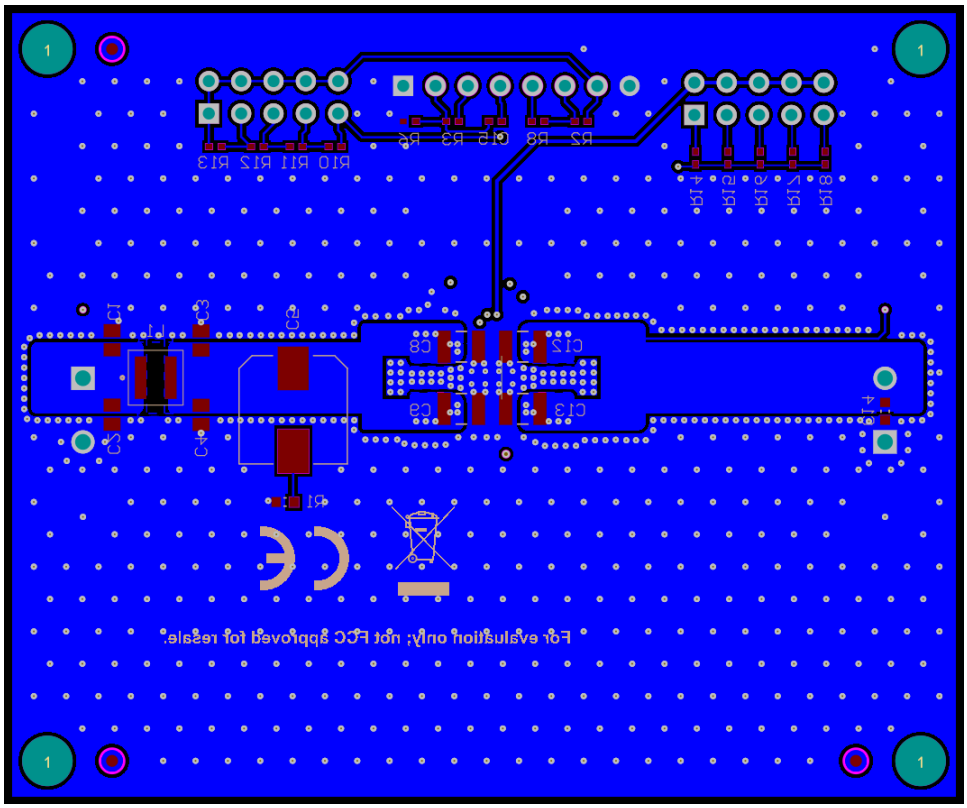

Figure 6-7. Bottom Layer Copper (Viewed From Top)

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6.4 Assembly Drawings

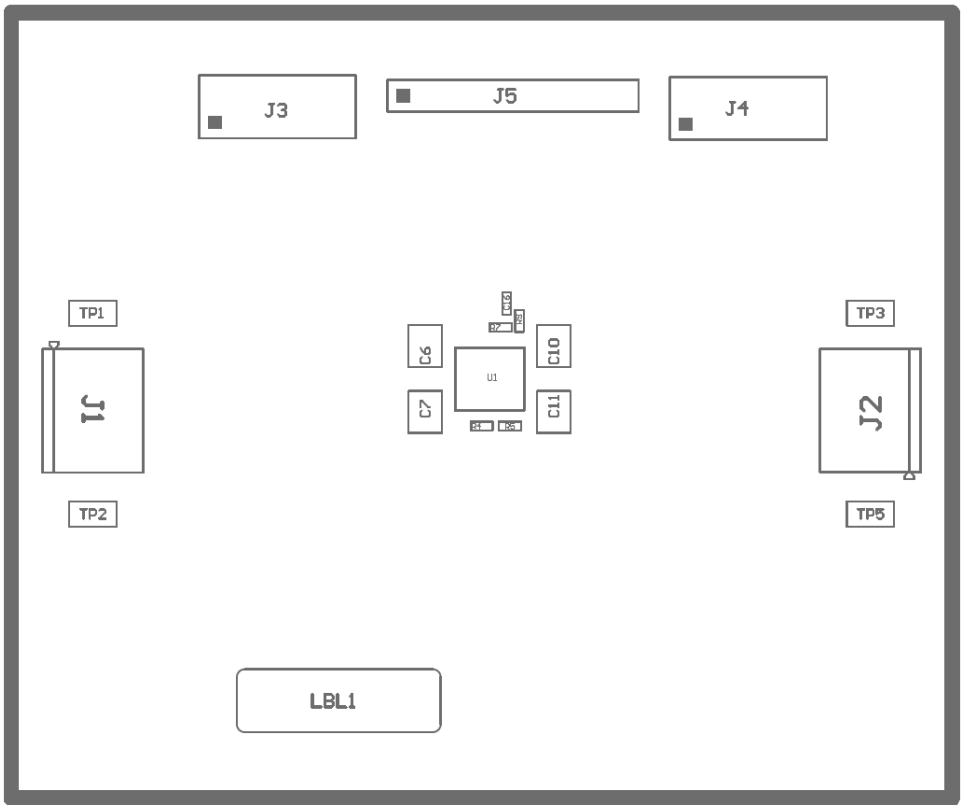

Figure 6-8. Top Assembly (Top View)

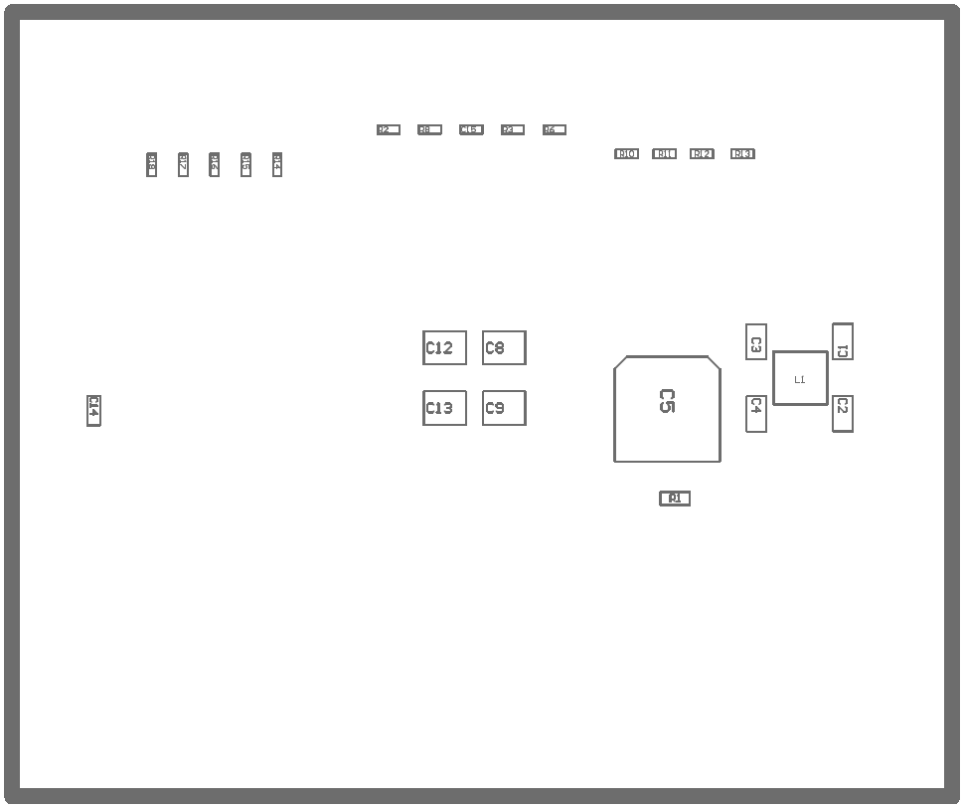

Figure 6-9. Bottom Assembly (Bottom View)

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6.5 Multi-Layer Stackup

	Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
	Top Overlay	Overlay				
	Top Solder	Solder Mask/Coverlay	Surface Material	0.4	Solder Resist	3.5
1	Top Layer	Signal	Copper	2.8		
	Dielectric1	Dielectric	Core	5	FR-4 High Tg	4.8
2	Signal Layer 1	Signal	Copper	2.8		
	Dielectric3	Dielectric	None	40	FR-4 High Tg	4.8
3	Signal Layer 2	Signal	Copper	2.8		
	Dielectric2	Dielectric	None	5	FR-4 High Tg	4.8
4	Bottom Layer	Signal	Copper	2.8		
	Bottom Solder	Solder Mask/Coverlay	Surface Material	0.4	Solder Resist	3.5
	Bottom Overlay	Overlay				

Figure 6-10. Layer Stackup

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7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

For development support see the following:

- TPSM63606 *Altium layout design files*
- TPSM63606 *simulation models*
- TPSM63603 and TPSM63603S *EVM user's guide*
- For TI's reference design library, visit *TI Reference Design library*
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*
- TI Reference Designs:
  - *Multiple output power solution for Kintex 7 application*
  - *Arria V power reference design*
  - *Altera Cyclone V SoC power supply reference design*
  - *Space-optimized DC/DC inverting power module reference design with minimal BOM count*
  - *3- to 11.5-V_{IN}, –5-V_{OUT}, 1.5-A inverting power module reference design for small, low-noise systems*
- Technical Articles:
  - *Powering medical imaging applications with DC/DC buck converters*
  - *How to create a programmable output inverting buck-boost regulator*
- To view a related device of this product, see the LM61460 36-V, 6-A synchronous buck converter

7.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63606 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2 Documentation Support

7.2.1 Related Documentation

For related documentation, see the following:

- *Innovative DC/DC Power Modules* selection guide
- *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- *Simplify Low EMI Design with Power Modules* white paper
- *Power Modules for Lab Instrumentation* white paper
- *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- *Soldering Considerations for Power Modules* application report
- *Practical Thermal Design With DC/DC Power Modules* application report
- *Using New Thermal Metrics* application report
- *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- *Using the TPSM53602/3/4 for Negative Output Inverting Buck-Boost Applications* application report

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