EVM User's Guide: TPSF12C1QEVM

Active EMI Filter Evaluation Module for Single-Phase AC Power Systems

Description

The TPSF12C1QEVM evaluation module (EVM) is specifically designed to validate the performance of the TPSF12C1 power-supply filter IC. The active EMI filter (AEF) helps to improve the common-mode (CM) electromagnetic interference (EMI) signature in single-phase AC power systems by amplification of the effective Y-capacitance value.

Get Started

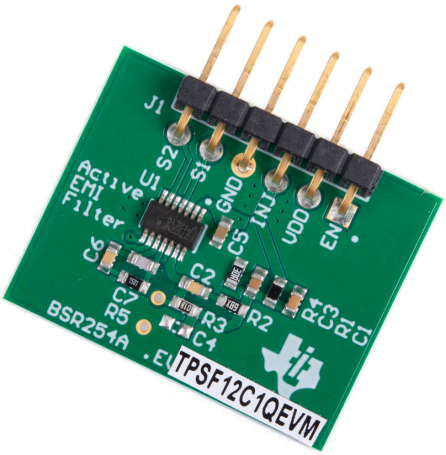
1. Order the TPSF12C1QEVM EVM
2. Study this EVM user's guide and PCB layout files
3. Use the TPSF12C1 quickstart calculator to assist with EMI filter design and component selection
4. Prior to connecting the power stage, test the active filter circuit with a low-voltage signal source
5. Connect the filter to an AC-input power stage and verify the INJ (pin 13) voltage swing is within limits
6. Measure the total (DM and CM) EMI signature and use a splitter to isolate the CM contribution

Features

- Improved CM EMI performance for applications with single-phase AC input
  - Helps to meet EMI standards, such as CISPR 11, 25 or 32
  - Voltage-sense, current-inject AEF topology presents low shunt impedance to ground
    - Up to 30 dB reduction in the CM EMI signature from 100 kHz to 3 MHz
  - A higher effective Y-capacitance enables a reduction in CM choke size, weight and cost
  - No additional magnetic components required
- Simple configuration for single-phase AC systems
  - Integrated sensing filter and summing network
  - Low Y-capacitor line-frequency leakage current to chassis ground maintains safety
  - Simplified compensation and damping network
- Inherent protection features for reliable design
  - Withstands 6-kV+ surge with minimal external component count
    - Helps meet IEC 61000-4-5 surge immunity system-level specification
    - Integrated SENSE input surge protection
  - Wide VDD supply voltage range of 8 V to 16 V
    - Undervoltage lockout (UVLO) set to turn on and off at 7.7 V and 6.7 V, respectively
    - Quiescent supply current of 12.5 mA
  - 175°C thermal shutdown protection
  - Integrated VDD-to-EN pullup allows use of an open-drain/collector device for disable function
- Fully assembled, tested and proven four-layer PCB design with 1" × 0.8" (25 mm × 20 mm) total area

Applications

- On-board charger for BEVs and PHEVs
- Power delivery – high-density server rack PSUs
- Welders and other industrial systems
- Telecom AC/DC rectifiers



1 Evaluation Module Overview

1.1 Introduction

The TPSF12C1QEVM evaluation module (EVM) is designed to conveniently evaluate the performance of the TPSF12C1 active filter IC. The EVM helps to improve the CM EMI signature in single-phase AC power systems.

The TPSF12C1 provides a low shunt impedance path for CM noise in the frequency range of interest for EMI measurement and helps to meet prescribed limits for EMI standards, such as:

- CISPR 11, EN 55011 – Industrial, Scientific and Medical (ISM) applications
- CISPR 25, EN 55025 – Automotive applications
- CISPR 32, EN 55032 – Multimedia applications

Enabling up to 30 dB of CM noise reduction at the lower end of specified frequency ranges (for example, 100 kHz to 3 MHz) significantly reduces the footprint, volume, weight and cost of the overall filter, especially the CM chokes that are designed to attenuate lower-order harmonics – and hence are large size.

While rejecting the line-frequency component at 50 Hz or 60 Hz, the TPSF12C1 senses the high-frequency CM noise-voltage disturbance on each power line using two Y-rated sense capacitors and injects a noise-canceling current back into the power lines using a Y-rated inject capacitor. The GND terminal of the EVM requires a direct, low-inductance connection to the chassis ground or Earth terminal of the filter circuit.

1.2 Kit Contents

- An EVM that includes the TPSF12C1 active EMI filter IC and associated low-voltage components
- EVM Disclaimer Read Me

1.3 Specifications

Table 1-1 lists the EVM specifications. V_{VDD} = 12 V, unless otherwise noted.

Table 1-1. Electrical Performance Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
VDD supply voltage, V_{VDD} (1)		8	12	16	V
VDD UVLO turn-on threshold, $V_{VDD(on)}$	V_{VDD} rising		7.7		
VDD UVLO turn-off threshold, $V_{VDD(off)}$	V_{VDD} falling		6.7		
VDD supply current, enabled, $I_{VDD(on)}$	EN open or tied high		12.5		mA
VDD supply current, disabled, $I_{VDD(off)}$	EN tied to GND		50		µA
OUTPUT CHARACTERISTICS					
Inject voltage, V_{INJ} (2)		2.5		V_{VDD} – 2	V
Inject current, I_{INJ}	V_{VDD} = 8 V to 16 V	–80		80	mA
SYSTEM CHARACTERISTICS					
Common-mode EMI reduction(3)	100 kHz to 1 MHz		25		dB
IC junction temperature, T_J (4)		–40		150	°C

(1) The nominal supply voltage (relative to chassis GND) of the TPSF12C1 is 12 V.
(2) Verify that the INJ pin voltage swing is between the prescribed limits to avoid saturation and clipping.
(3) The expected EMI reduction with this EVM is up to 30 dB (with the device enabled vs. disabled) when swept from 100 kHz to 3 MHz. This performance metric can change based on the VDD supply voltage, passive filter component values, active circuit compensation and damping component values, ambient temperature, and other parameters.
(4) Calculate the TPSF12C1 operating junction temperature based on the VDD supply voltage and current, the local ambient temperature, and the junction-to-ambient thermal resistance: $T_J = T_A + R_{\theta JA} \times P_D$, where the IC power dissipation is $P_D = V_{VDD} \times I_{VDD}$.

1.4 Device Information

CM filters for both commercial (Class A) and residential (Class B) environments typically have limited Y-capacitance due to touch-current safety requirements and thus require large-sized CM chokes to achieve the requisite attenuation. This ultimately results in filter designs with bulky, heavy and expensive passive components. The deployment of active filter circuits enable more compact filters for next-generation power conversion systems.

Figure 1-1 presents typical schematics of equivalent single-phase passive and active filter designs. Terminals designated L, N and PE refer to Live, Neutral and Protective Earth, respectively. Comparing the passive and active circuits in Figure 1-1, the CM inductance of chokes L_{CM1} and L_{CM2} each reduces by a factor of four to six times by virtue of the higher effective Y-capacitance with the TPSF12C1 circuit.

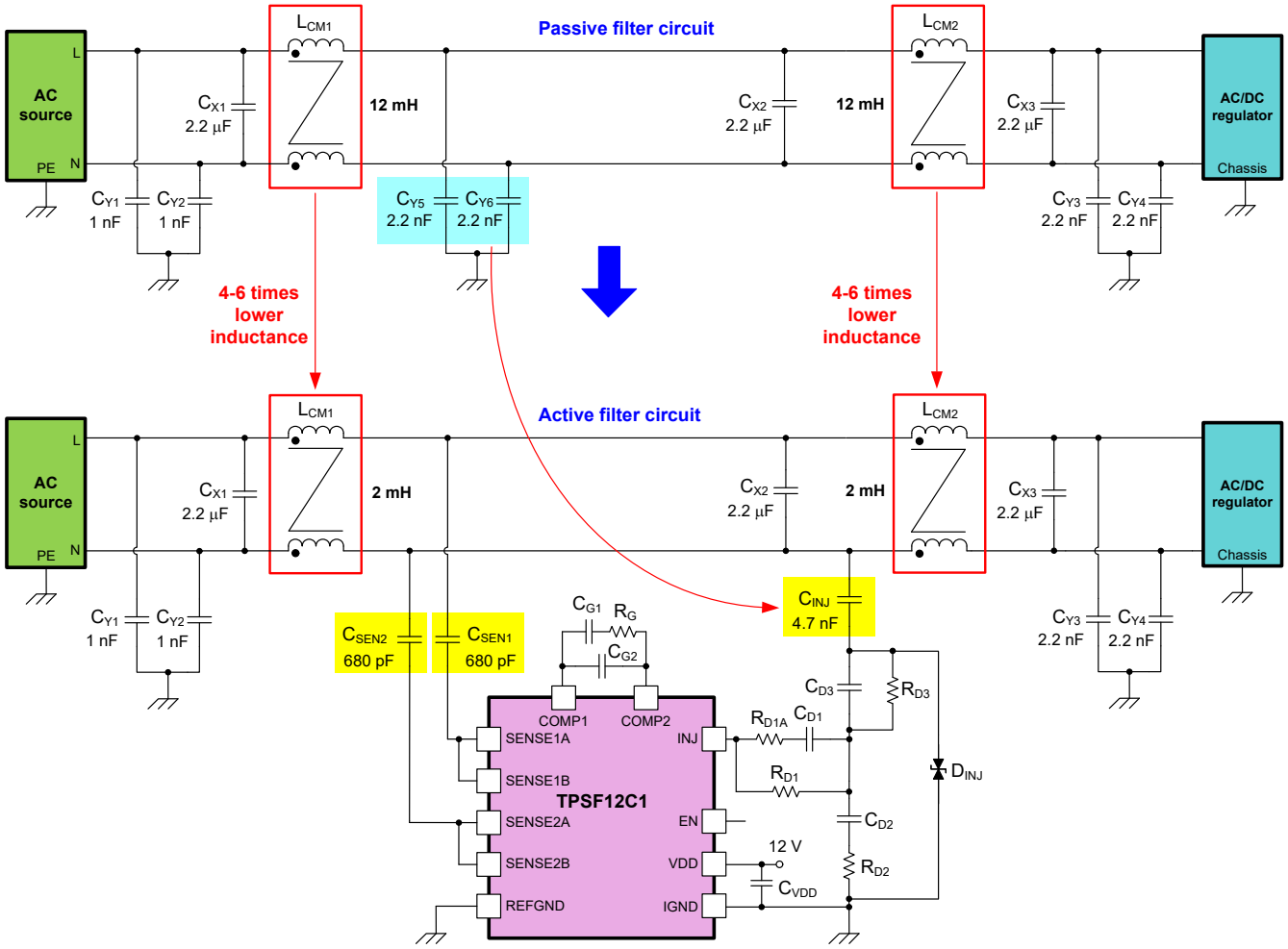


Figure 1-1. Passive and Active Filter Schematics

The AEF circuit uses a capacitive multiplier circuit in place of the two Y-capacitors normally placed between the CM chokes in a conventional two-stage passive filter design – see C_{Y5} and C_{Y6} in Figure 1-1. The TPSF12C1 senses the high-frequency CM disturbance on the two power lines using a set of Y-rated sense capacitors and injects a noise-canceling current back into the power lines using a Y-rated inject capacitor.

The X-capacitors placed between the two CM chokes provides a low-impedance path between the power lines from a CM standpoint, typically up to low-MHz frequencies. This allows current injection onto one power line (neutral in this case) using only one inject capacitor.

The advantages of AEF with the TPSF12C1 summarize as:

1. Simple filter structure – with wide operating frequency range and high stability margins.
2. Reduced CM choke size – for lower volume, weight and cost. This also enables much less copper loss and better high-frequency performance due to lower choke self-parasitics and higher self-resonant frequency.
3. No additional magnetic components for sensing or injection – the TPSF12C1 instead uses Y-rated sense and inject capacitors with minimal impact to peak touch current (measured according to IEC 60990).
4. Enhanced safety – the TPSF12C1 is a low-voltage device referenced to chassis ground.
5. Standalone IC implementation – enables flexible placement of the AEF circuit near the filter components.
6. Surge immunity – the TPSF12C1 is robust to line voltage surges (with an appropriate TVS diode installed at the low-voltage side of the inject capacitor). This helps to meet surge specifications such as IEC 61000-4-5.

2 Hardware

2.1 EVM Description

The TPSF12C1QEVM, a daughter-card design that attaches to an existing passive EMI filter circuit in a single-phase AC power system, showcases the CM EMI performance improvement or size reduction achievable with the TPSF12C1, a single-phase power-supply filter IC.

The EVM can be used for evaluation and for system development of a single-phase EMI filter circuit and application. The AEF circuit effectively replaces the two Y-capacitors normally placed between the CM chokes (and tied to chassis ground) in a conventional two-stage, fourth-order passive CM filter design. The design uses a recommended PCB layout to minimize the overall noise signature and required board area.

Note

The damping and compensation component values included with this EVM can require modification if the passive filter components (the CM chokes in particular) are changed. Refer to the *TPSF12C1 Standalone Active EMI Filter for Common-mode Noise Mitigation in Three-Phase AC Power Systems* data sheet and *TPSF12C1 quickstart calculator* for additional guidance pertaining to AEF circuit operation, loop gain and stability analysis, passive component selection, and expected common-mode EMI performance.

	**CAUTION** Hot surface. Contact can cause burns. Do not touch.
	**CAUTION** High Voltage. Risk of electric shock.

2.2 Setup

Figure 2-1 shows a typical EMI measurement setup. A line impedance stabilization network (LISN) in series with each supply line and a good EMI receiver provide a measurement of the total EMI that includes DM and CM propagation components. Appropriate addition or subtraction of the total noise measurement from each LISN, designated as V_1 and V_2 in Figure 2-1, enables an examination of CM and DM noise signatures, respectively.

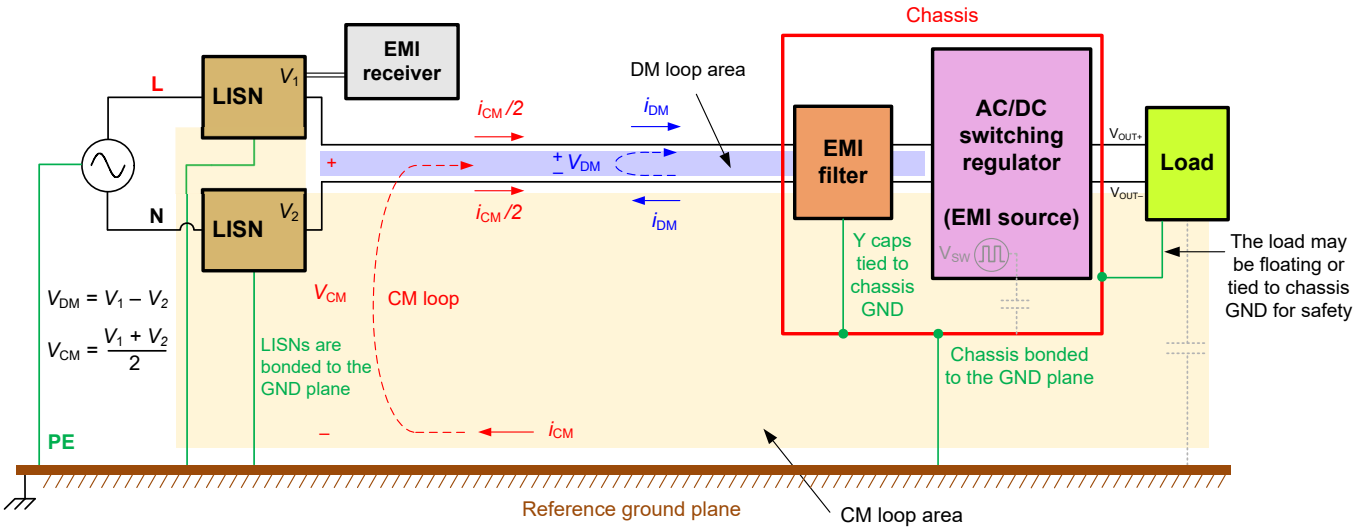


Figure 2-1. EMI Measurement Setup for a Single-Phase System

The AC/DC regulator has internal high-dv/dt switching nodes that can capacitively couple CM noise to the chassis. As such, verifying the Y-capactiors in the EMI filter are closely referenced to the chassis is imperative, as illustrated in Figure 2-1. The Y-capacitors can then return the CM noise current back to the noise source in a tight conduction loop. Otherwise, the noise current can flow in the reference ground plane back to the LISNs, rendering the EMI filter less effective.

2.2.1 High-Voltage Testing

Referencing the header connections described in Table 2-1, use the recommended setup from the schematic of Figure 2-2 to evaluate the performance of the TPSF12C1 with a single-phase AC/DC regulator. A two-phase interleaved boost PFC topology represents a typical power stage and is drawn for illustrative purposes in Figure 2-2 (the setup is essentially agnostic to regulator topology).

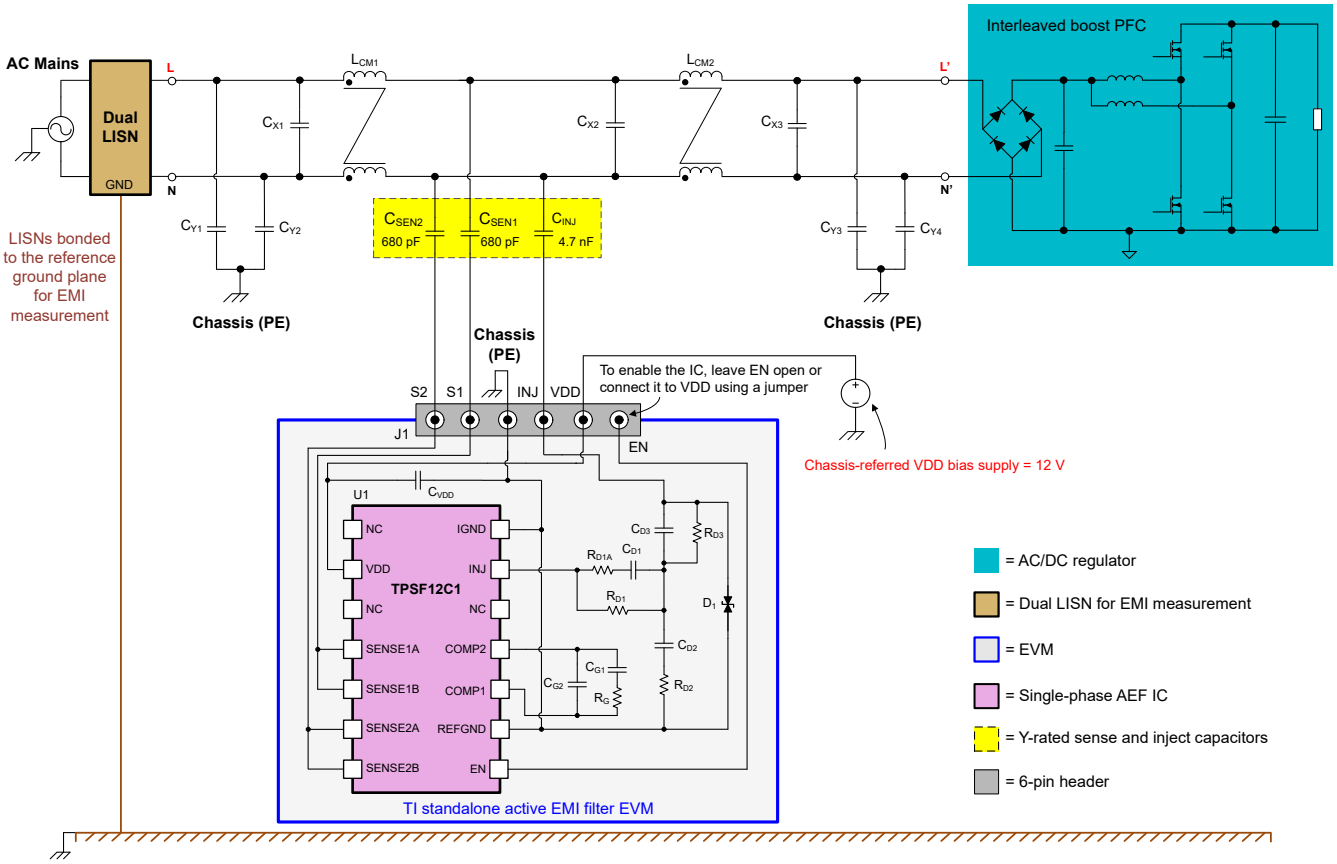


Figure 2-2. EVM Setup Schematic for High-Voltage Testing With an AC/DC Regulator Connected

2.2.2 EVM Connections

The EVM daughter-card connects to the main EMI filter board through header J1. The sense and inject capacitors, along with a robust ground connection, interfaces the low-voltage EVM to the high-voltage power lines.

Header J1 provides an interface through terminals S1, S2, INJ and GND, as described in Table 2-1. Connect S1 and S2 to sense capacitors, designated as C_{SEN1} and C_{SEN2} in Figure 2-2. Connect the opposite terminals of the sense capacitors to the Live and Neutral power lines between the CM chokes, L_{CM1} and L_{CM2}. Connect INJ to the inject capacitor, designated as C_{INJ}, whose opposite terminal then connects to either the Live or Neutral power line as shown. The X-capacitor at this position, designated as C_{X2}, sets a low impedance between the power lines from a CM standpoint – this means that a single inject capacitor is adequate for current injection. Finally, connect a nominal 12-V bias supply from VDD to GND to power the AEF circuit. The GND attachment point on the filter board corresponds to where the Y-capacitors in a passive design normally connect.

Refer to the diagram of Figure 2-3 for an example of component placement on a filter board, where the EVM header J1 can mount directly to receptacle J2.

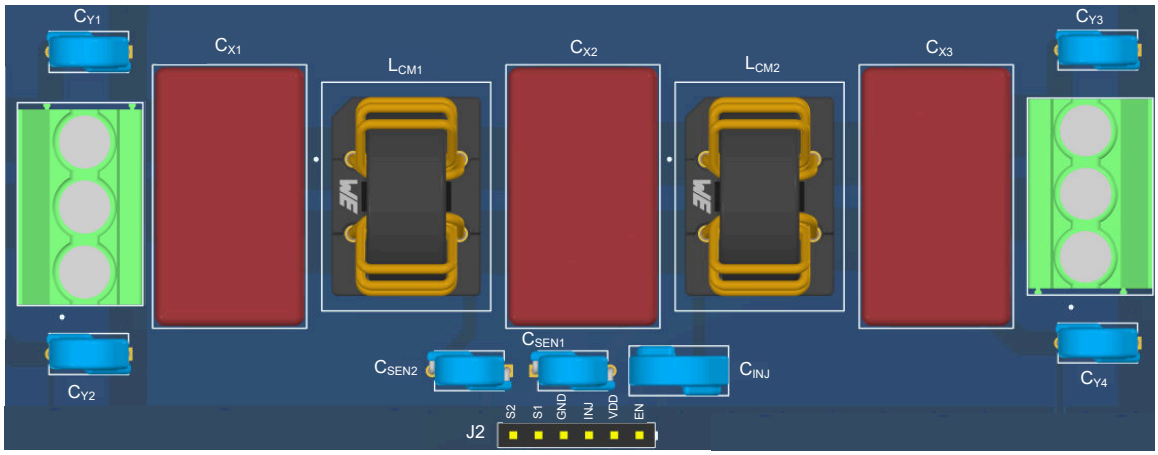


Figure 2-3. Filter Component and EVM Placement Example

2.2.3 Low-Voltage Testing

Figure 2-4 shows a schematic for low-voltage testing of the active filter design, including insertion loss measurement and EMI performance characterization. This facilitates an easy and convenient verification of the active filter circuit prior to connection to a high-voltage switching regulator. A good signal source and coupling capacitor provide CM excitation that mimics the CM noise source voltage and noise source impedance related to the switch-node behavior of an actual power stage.

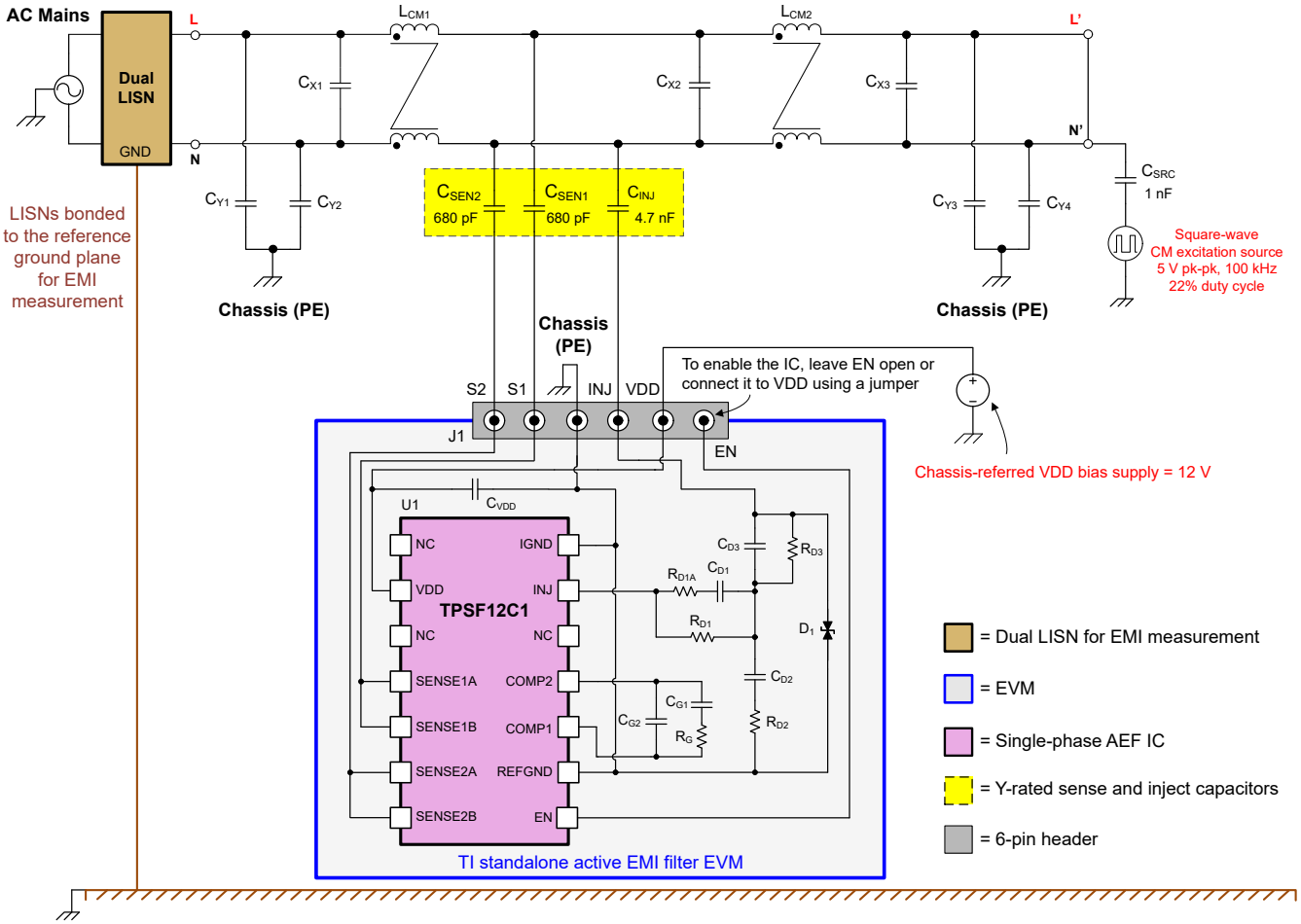


Figure 2-4. EVM Setup Schematic for Low-Voltage Testing

2.3 Header Information

As outlined in Table 2-1, header J1 provides connections to the low-voltage side of the SENSE capacitors (corresponding to the SENSE pins of the IC), the low-voltage side of the inject capacitor, the IC bias power supply (VDD and GND pins), which is set between 8 V and 16 V, and a remote enable (EN) signal.

Table 2-1. J1 Header Connections

POSITION(1)	LABEL	DESCRIPTION
1	EN	Enable input – leave open or tie high to enable the IC; tie to GND to disable
2	VDD	Supply voltage connection – connect to a 12-V bias power supply referenced to GND(2)
3	INJ	Inject output – connect to a Y-rated inject capacitor, C_{INJ}
4	GND	Ground – connect to the chassis ground of the system with a direct, low-inductance connection
5	S1	Sense 1 input – connect to a Y-rated sense capacitor, C_{SEN1}
6	S2	Sense 2 input – connect to a Y-rated sense capacitor, C_{SEN2}

(1) Pin positions of header J1 are designated right to left when viewed from the top side of the EVM.
(2) Working at an ESD-protected workstation, verify that any wrist straps, bootstraps or mats are connected and referencing the user to Earth ground before power is applied to the EVM.

A 6-pin right-angle header, part number TSW-106-08-G-S-RA, connects the EVM to a corresponding female receptacle, part number SSW-106-01-G-S, which mounts on the EMI filter board that carries the passive filter components – the CM chokes, X-capacitors and Y-capacitors – as well as the sense and inject capacitors. The EVM includes both the header and the receptacle, manufactured by Samtec. See Section 4.2.

2.4 EVM Performance Validation

1. Connect the EVM to the filter board (see receptacle J2 in Figure 2-3).
2. Apply a VDD bias supply voltage of 8 V to 16 V (nominal 12 V, with ripple voltage less than 20 mV peak-to-peak) between the VDD and GND terminals of J1.
3. Measure the voltage at the INJ pin of the TPSF12C1 (pin 13) with respect to GND; a DC voltage of $V_{VDD}/2$ and have no AC perturbations that indicate instability. The VDD current consumption must be approximately 12 mA. If the INJ pin voltage is oscillating, modify the damping network components on the EVM to achieve stability.
4. The user must perform *low-voltage testing* prior to connecting the high-voltage power stage. To provide a CM stimulus, connect a 5-V peak-to-peak square-wave source from a function generator as shown in Figure 2-4. Set the signal frequency to the switching freqeuncy of the power stage and choose a duty cycle that creates all the spectral harmonics (aside: 50% duty cycle eliminates the even harmonics, 33.3% removes the triple-n harmonics, and so forth). A 1-nF capacitor in series with the signal source emulates a practical CM noise source impedance.
   - Using this CM excitation source, verify the dynamic voltage range of the TPSF12C1 INJ pin. **Ensure that the INJ pin voltage relative to GND operates in a window between 2.5 V and V_{VDD} – 2 V**.
5. Connect a LISN on each input power line and measure the EMI with AEF disabled (EN tied to GND) to benchmark the existing passive filter. Short the low-voltage (bottom) terminal of the inject capacitor to GND when AEF is disabled by tying the INJ terminal on J1 to GND. This emulates the Y-capacitor connection in an equivalent passive filter design.
6. Remove the pulldown short on the inject capacitor and enable the AEF circuit by allowing EN to float high. Repeat the EMI measurement, thus quantifying the EMI reduction with AEF.
7. In a similar fashion, perform a comparison of filter *insertion loss* or *attenuation* performance using a network analyzer. For a true insertion loss measurement with 50-Ω source and load impedances, replace the LISN by a 50-Ω load tied from L or N to GND.
8. Using high-voltage safety precautions, connect the switching power stage as shown in Figure 2-2. Turn the regulator ON and, similar to step 4, verify that the IC's INJ pin voltage is not getting clipped. To improve the dynamic range of the INJ voltage, increase one or more of the following:
   - Regulator-side Y-capacitance, C_{Y3} and C_{Y4}
   - Inject capacitance, C_{INJ}
   - VDD supply voltage, V_{VDD}
9. Measure the EMI with AEF enabled and disabled, similar to the procedure outlined in steps 5 and 6.
10. Turn the regulator OFF. Wait for all high-voltage capacitors to fully discharge.

2.5 AEF Design Flow

Follow these steps to design an active filter circuit:

1. **Quickstart Calculator** – Use the TPSF12C1 quickstart calculator as a convenient starting point. See Figure 2-5 for illustration.

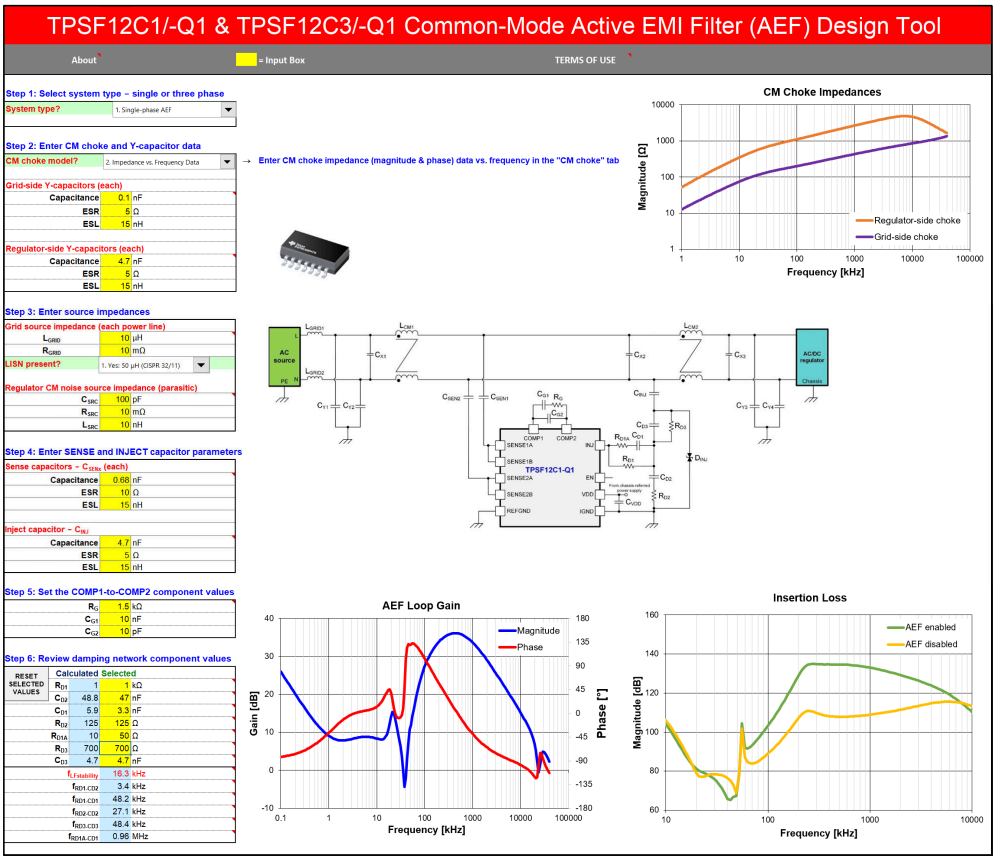


Figure 2-5. Quickstart Calculator With CM Choke Impedance, Loop Gain and Insertion Loss Plots

Typical steps to complete the quickstart calculator are as follows:

- Choose the core material for the CM chokes – the primary choices being nanocrystalline (NC) or ferrite. NC chokes are preferable for active filter designs given their higher permeability (and thus fewer winding turns), broader impedance characteristic over frequency, more damped impedance behavior with softer phase transition, and better stability over temperature.
- Define the CM choke impedances – two options are available:
  - Measure the CM impedance magnitude and phase vs. frequency using a network analyzer. Paste the data directly into the calculator file.
  - Enter the behavioral model parameters for each choke based on (a) a parallel LRC circuit for a ferrite choke (L_{CM} || R_{PAR} || C_{PAR}), or (b) a ladder network for an NC choke consisting of three parallel RL circuits connected in series along with a parasitic capacitance across the total network. An equivalent circuit model is the most convenient option if the choke data sheet includes the CM impedance data.
- Enter values for the grid-side and regulator-side Y-capacitors, sense capacitors and inject capacitor.
- Enter values for source impedance of the grid supply and the noise source. Select from a drop-down menu if a LISN (50 µH or 5 µH) is installed.
- Review the AEF loop gain plot for stability based on the calculated component values for the damping network. Adjust the damping network values to ensure the phase does not reach –180° at the resonant frequencies (when the gain is positive). Refer to the TPSF12C1 data sheet for guidance on component selection. Check the insertion loss plots with AEF enabled and disabled.

2. **Circuit Simulation** – Avail of PSPICE or SIMPLIS simulation models for the TPSF12C1 device. Use such models along with prepared test benches to investigate the operation of the complete active filter circuit. See the SIMPLIS schematic in Figure 2-6 as an example. Perform both time-domain and frequency-domain analyses as required.

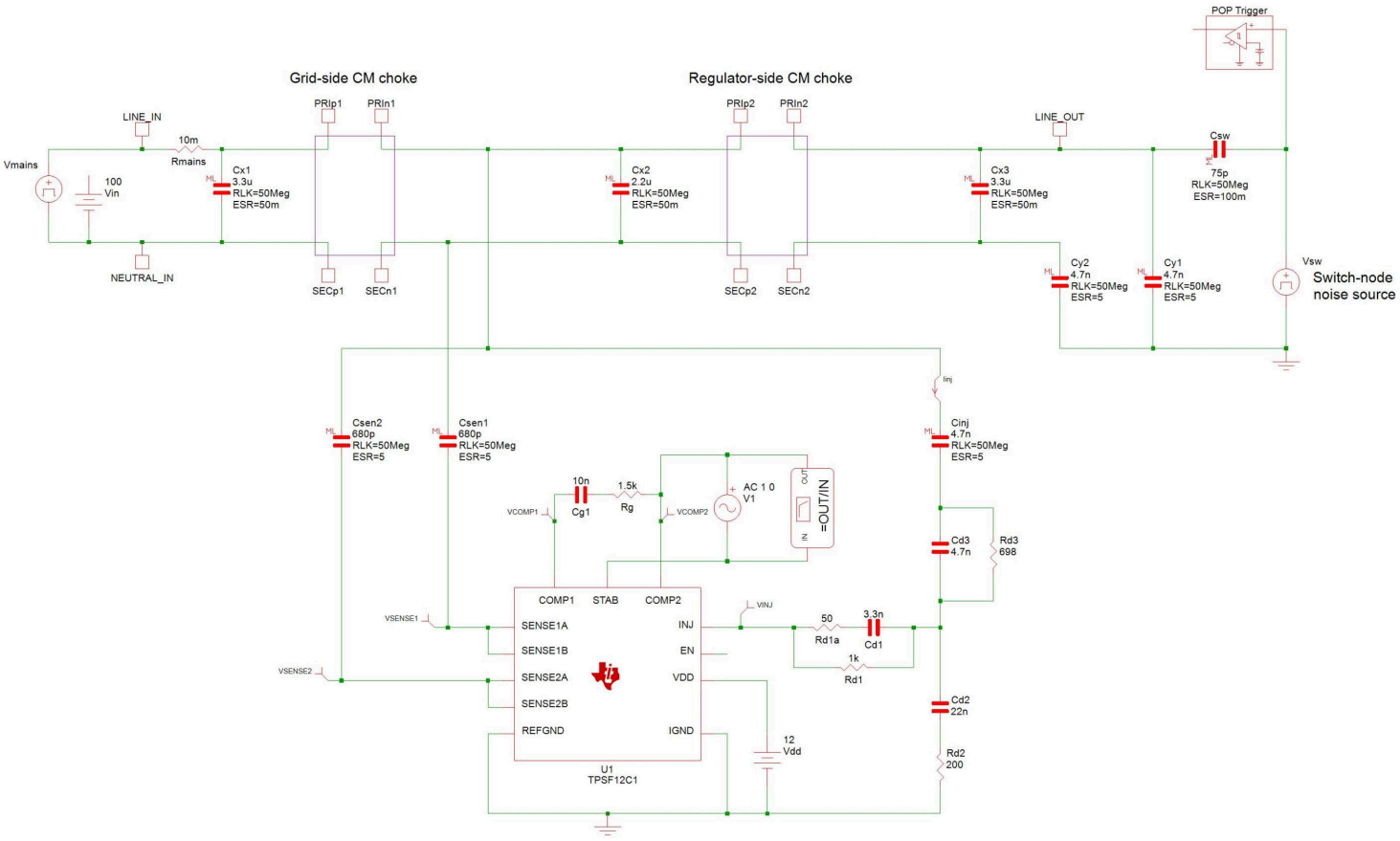


Figure 2-6. SIMPLIS Simulation Schematic of an Active Filter Circuit Using the TPSF12C1

Note that the CM choke model schematics are not shown above. If the choke model equivalent circuit parameters are defined in the quickstart calculator, transfer them directly to the simulation model as needed.

3. **Low-Voltage Tests** – Validate the filter design at low voltage prior to connecting to the switching regulator. This is a relatively easy step to confirm various aspect of the design, including filter stability, insertion loss, voltage swing on the INJ pin, and EMI performance with CM signal excitation. See Figure 2-4 and refer to tests 4 through 7 described in Section 2.4.
   - Insertion loss – measure with 50-Ω source and load impedances.
   - Apply a CM excitation signal with a function generator.
     - Check the dynamic voltage range of the INJ pin (TPSF12C1 pin 13).
     - Measure the EMI (CM only, there is no DM propagation in this test).
4. **High-Voltage Tests** – Validate the filter design while connected to the switching regulator. See Figure 2-2 and refer to tests 8 and 9 described in Section 2.4.
   - Check the dynamic voltage range of the INJ pin.
   - Calculate the device power dissipation(4) based on V_{VDD}, I_{VDD}, T_A and $R_{\theta JA}$. Verify that the maximum junction temperature is less than 150°C under the worst case operating conditions.
   - Check the sense and inject capacitance variation over temperature and ensure the circuit is stable under all operating conditions.
   - Measure the total EMI. Separate the CM (asymmetrical) and DM (symmetrical) propagation components, as the TPSF12C1-based AEF circuit only attenuates the CM noise.

2.5.1 AEF Circuit Optimization and Debug

Here are some considerations and best practices to optimize AEF circuit operation:

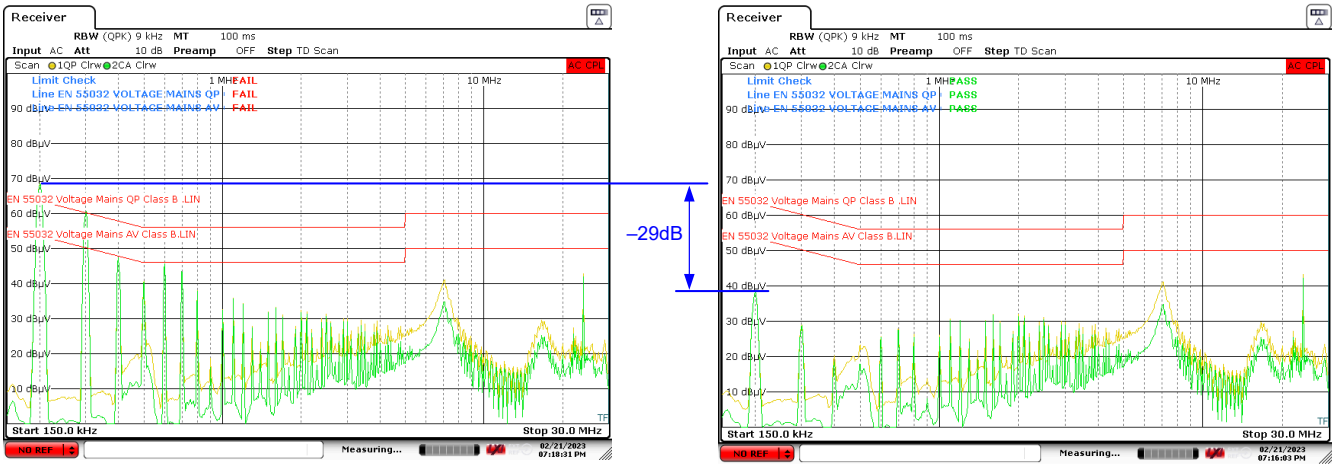
1. If the EMI measurement with AEF enabled is not performing as expected, then probe the TPSF12C1 INJ pin voltage while the regulator is switching. Verify that the INJ voltage is not getting clipped near the positive or negative supply rails, as mentioned in step 4 of Section 2.4.
   - If the INJ voltage is getting clipped, then increase the regulator-side Y-capacitance and/or the inject capacitance. Then recheck loop stability using the TPSF12C1 quickstart calculator or by simulation.
2. The metallic chassis structure is a critical part of the overall filter implementation. The filter PCB typically mounts to the chassis structure using several screw attachments, and the chassis serves to connect the various GND nodes on the filter PCB. These nodes are not explicitly connected with PCB copper and instead rely on the chassis to complete the electrical connection. As such, the chassis becomes the lowest impedance return path for CM noise current.
   - When testing a power system that includes a chassis as illustrated in Figure 2-1, CM noise can capacitively couple to the reference ground plane of the EMI measurement setup and thus bypass a filter circuit that is not closely referenced to the ground plane. In this case, TI recommends bonding the GND plane of the filter EVM directly to the reference ground plane. This also serves to minimize parasitic inductance in the GND connection to the AEF circuit. CM noise current emanating from the power stage then gets recirculated by the low shunt impedance of the Y-capacitors (both active and passive), thereby preventing noise from reaching the LISN.
3. Based on the amplification of the effective Y-capacitance, AEF enables a reduction of the CM choke inductance while maintaining the same LC corner frequency and CM attenuation characteristic. However, a choke with reduced CM inductance and smaller size typically has a lower leakage inductance, which is responsible for DM attenuation along with the X-capacitors.
   - If the DM inductance is significantly reduced when using smaller CM chokes, then increase the X-capacitance or add a small discrete inductor to obtain sufficient DM attenuation. Otherwise, a high DM noise component (relative to the CM component) can dominate the total noise measurement, thereby concealing the impact of AEF on CM noise mitigation.
4. Typical values for the sense and inject capacitances are 680 pF and 4.7 nF, respectively. Depending on the final implementation in the target application, **the default damping and compensation component values installed on the EVM can require modification by the user to achieve acceptable loop stability**. Ferrite chokes are inherently more difficult to stabilize than nanocrystalline.
   - For additional context pertaining to component selection and circuit optimization, refer to the TPSF12C1 product data sheet and the TPSF12C1 quickstart calculator.

3 Implementation Results

Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements. Unless otherwise indicated, V_{VDD} = V_{EN} = 12 V.

3.1 EMI Performance

See the *Schematic* and *Bill of Materials* for details of the EVM components for this measurement. The filter schematic in Figure 1-1 gives the passive circuit component values. As shown, the EMI is reduced by 29 dB at 200 kHz when AEF is enabled.



(a) (b)

Figure 3-1. CISPR 32 Class B Conducted Emissions With AEF Disabled (a) and Enabled (b)

3.2 Thermal Performance

Figure 3-2 shows the typical thermal performance of an active filter design rated at 10 A. The CM choke windings and TPSF12C1 device run at 28°C and 12°C above the local ambient temperature, respectively.

See the TPSF12C1EVM-FILTER *EVM user's guide* for more detail.

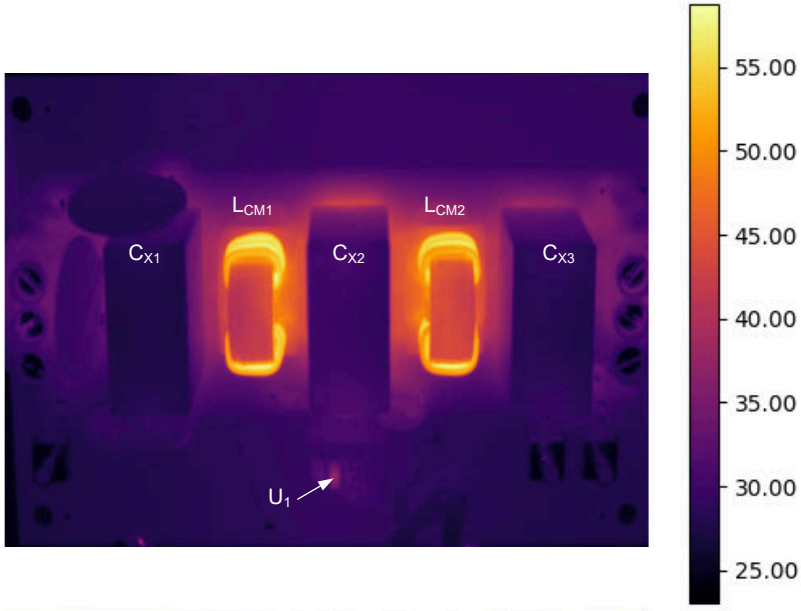


Figure 3-2. Thermal Image of an Active Filter Design at 10-A Load, 27°C Ambient

3.3 Surge Immunity

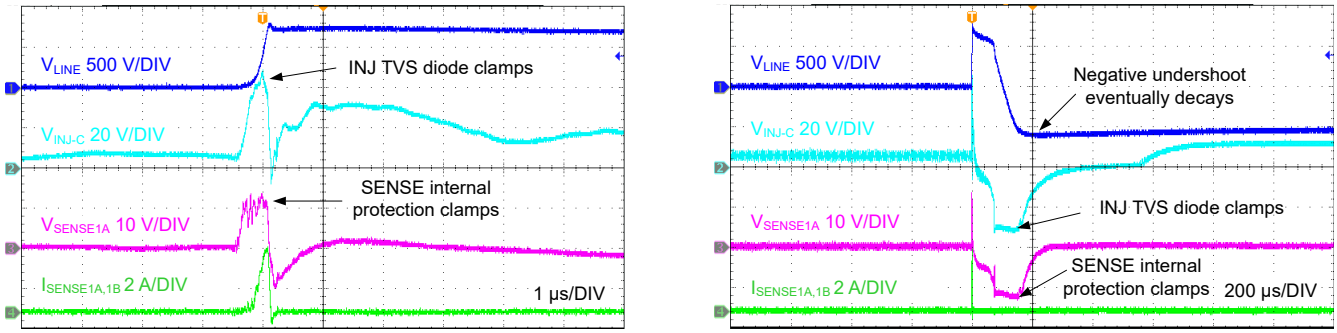


Figure 3-3. IEC 61000-4-5 Positive Surge, 6-kV Single Strike – 1 µs/div (a), 200 µs/div (b)

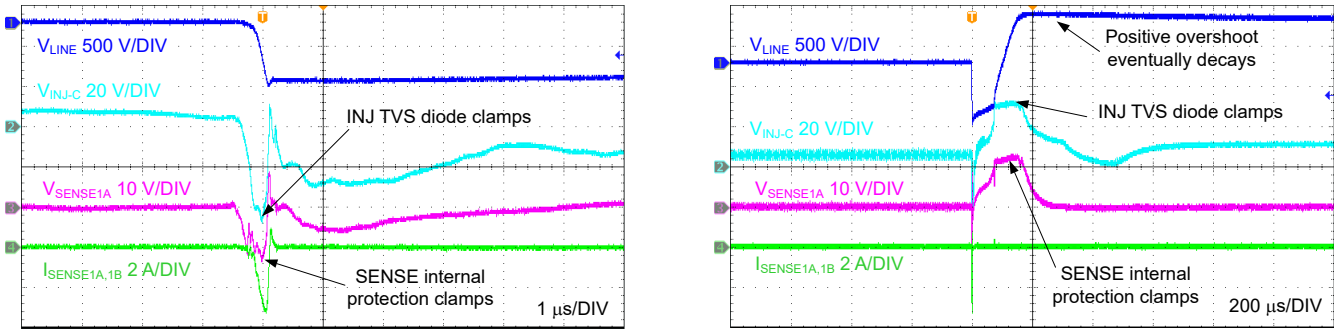


Figure 3-4. IEC 61000-4-5 Negative Surge, 6-kV Single Strike – 1 µs/div (a), 200 µs/div (b)

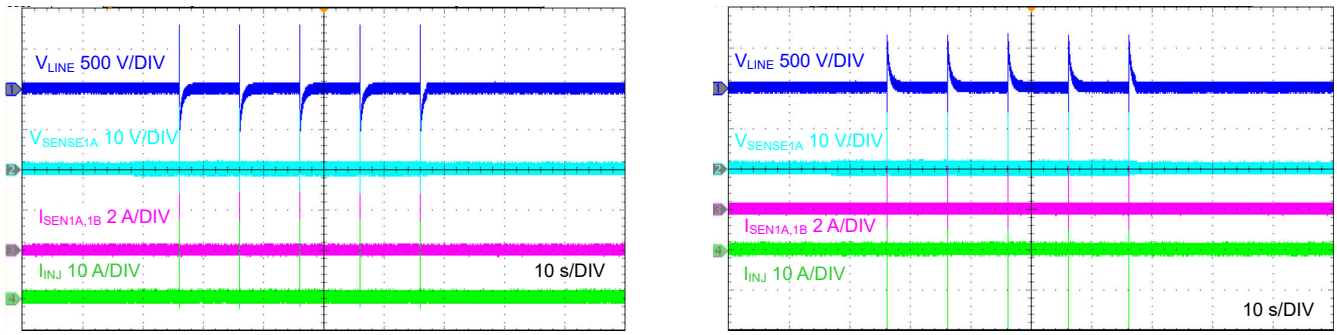


Figure 3-5. IEC 61000-4-5 Surge, 6-kV Repetitive Strike at 10-Second Intervals – Positive (a), Negative (b)

3.4 SENSE and INJ Voltages

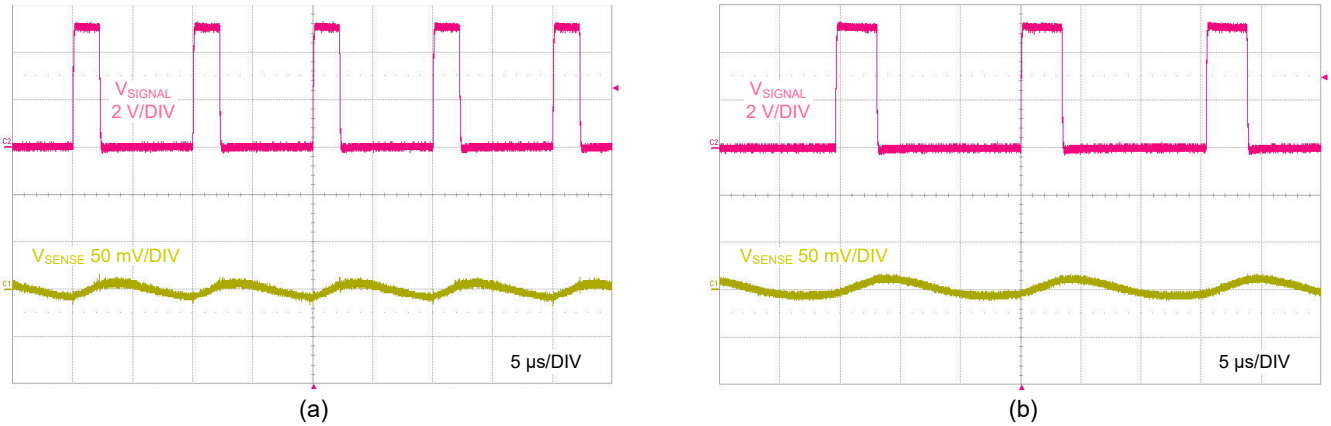


Figure 3-6. TPSF12C1 SENSE (pin 4) Voltage With CM Stimulus Applied – 100 kHz (a), 65 kHz (b)

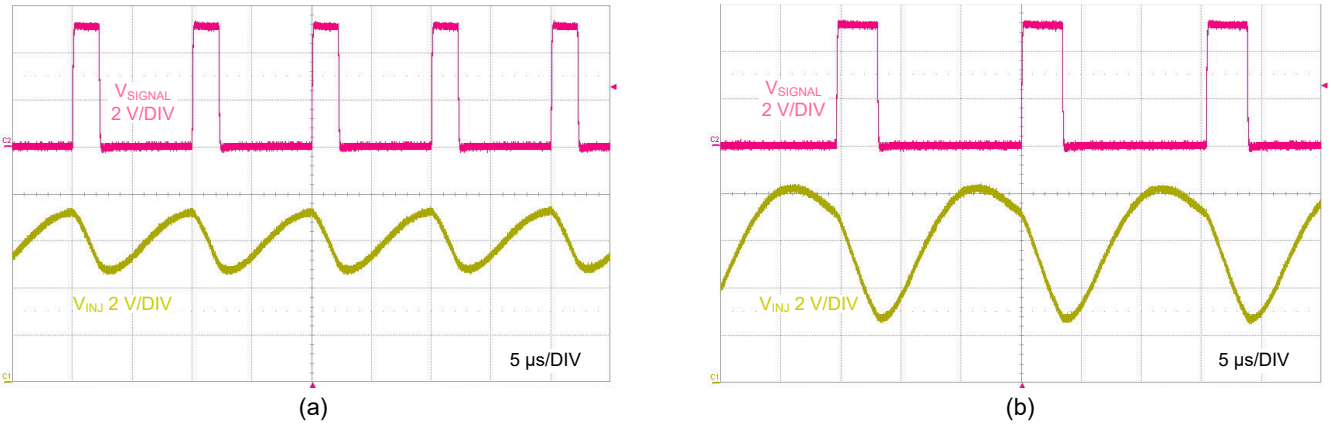


Figure 3-7. TPSF12C1 INJ (pin 13) Voltage With CM Stimulus Applied – 100 kHz (a), 65 kHz (b)

3.5 Insertion Loss

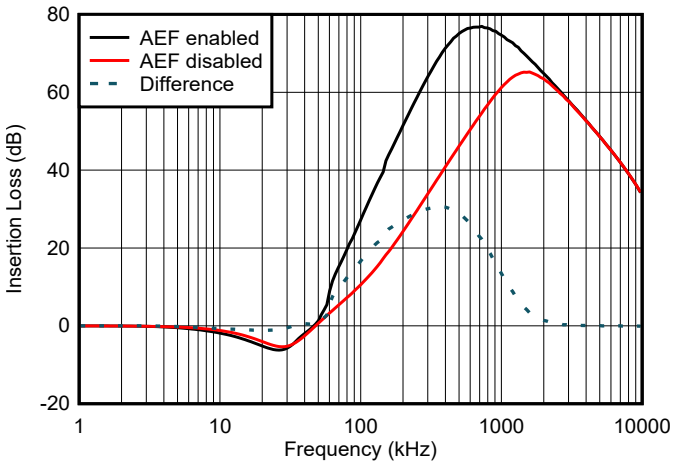


Figure 3-8. Typical Insertion Loss with AEF Enabled and Disabled

4 Hardware Design Files

For development support see the following:

- TPSF12C1 *Quickstart calculator*
- TPSF12C1QEVM *Altium layout source files*
- TPSF12C1 PSPICE for TI and SIMPLIS *simulation models*
- TPSF12C1EVM-FILTER *EVM user's guide*
- TPSF12C1EVM-FILTER *Altium layout source files*
- For TI's reference design library, visit *TI Reference Design library*
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*
- Technical Articles:
  - Texas Instruments, *How a stand-alone active EMI filter IC shrinks common-mode filter size*

4.1 Schematic

Figure 4-1 provides the EVM schematic.

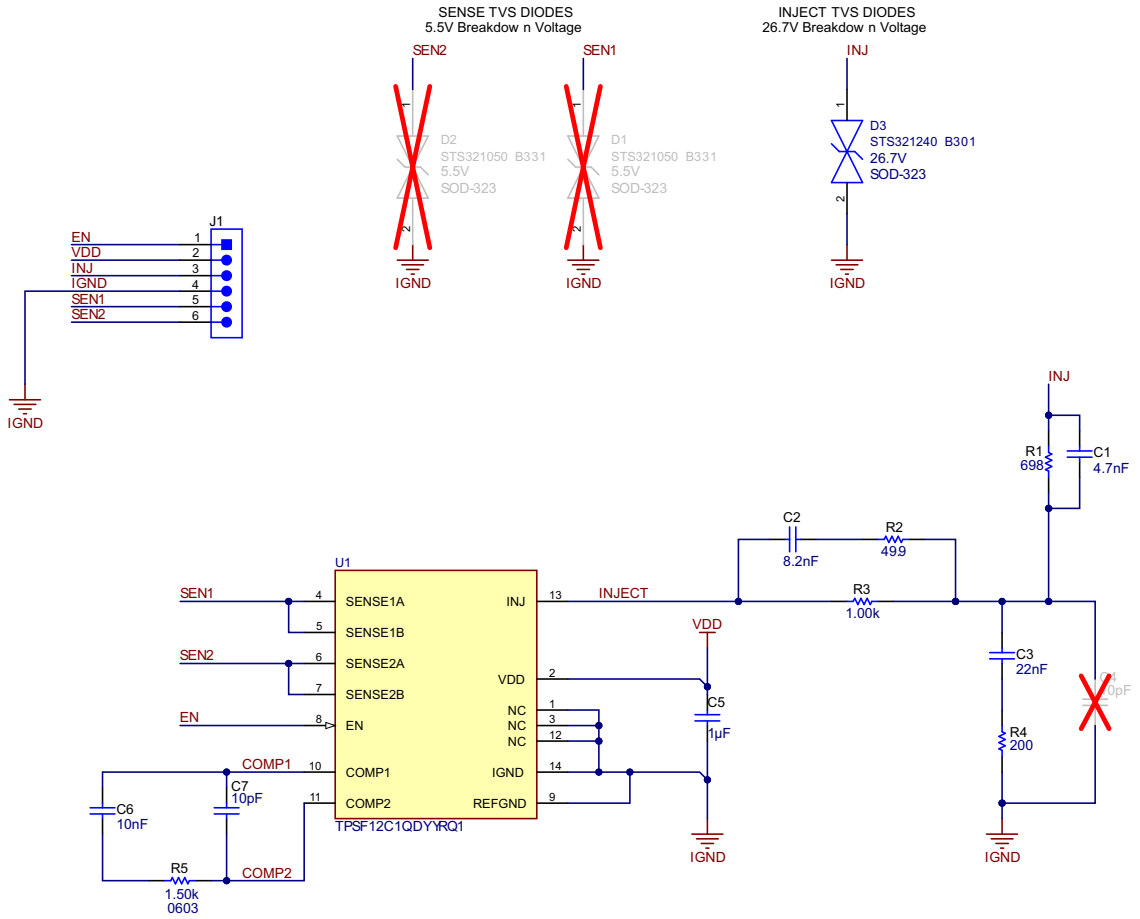


Figure 4-1. EVM Schematic

4.2 Bill of Materials

Table 4-1. EVM Component BOM

REF DES	QTY	VALUE	DESCRIPTION	PACKAGE	PART NUMBER	MANUFACTURER
C1	1	4.7 nF	CAP, CERM, 4.7 nF, 50 V, X7R	0603	C0603C472J5RACTU	Kemet
C2	1	8.2 nF	CAP, CERM, 8.2 nF, 50 V, X7R	0603	GRM188R71H822KA01D	MuRata
C3	1	22 nF	CAP, CERM, 22 nF, 50 V, X7R	0603	C0603C223K5RACTU	Kemet
C5	1	1 µF	CAP, CERM, 1 µF, 25 V, X7R	0603	CGA3E1X7R1E105K080AC	TDK
C6	1	10 nF	CAP, CERM, 10 nF, 50 V, X7R	0603	C0603X103K5RACTU	Kemet
C7	1	10 pF	CAP, CERM, 10 pF, 50 V, C0G/NP0	0603	CGA3E2C0G1H100D080AA	TDK
D3	1	24 V	TVS diode, 24 V standoff, 50 V at 8 A	SOD-323	STS321240B301	Eaton
J1	1	–	Header, 100 mil, 6 × 1, Gold, R/A, TH	–	TSW-106-08-G-S-RA	Samtec
J2	1	–	Receptacle, 6 × 1, 2.54 mm, Gold, TH	–	SSW-106-01-G-S	Samtec
R1	1	698 Ω	RES, 698 Ω, 1%, 0.1 W	0603	CRCW0603698RFKEA	Vishay-Dale
R2	1	49.9 Ω	RES, 49.9 Ω, 1%, 0.1 W	0603	CRCW060349R9FKEA	Vishay-Dale
R3	1	1 kΩ	RES, 1 kΩ, 1%, 0.1 W	0603	CRCW06031K00FKEA	Vishay-Dale
R4	1	200 Ω	RES, 200 Ω, 1%, 0.1 W	0402	CRCW0603200RFKEA	Vishay-Dale
R5	1	1.5 kΩ	RES, 1.5 kΩ, 1%, 0.1 W	0402	CRCW06031K50FKEA	Vishay-Dale
U1	1	–	TPSF12C1-Q1 common-mode AEF IC	TSOT23-14	TPSF12C1QDYYRQ1	Texas Instruments

Table 4-2. Sense and Inject Capacitors (Not Supplied)

REF DES	QTY	VALUE	DESCRIPTION	PACKAGE	PART NUMBER	MANUFACTURER
C_{SEN1}, C_{SEN2}	2	680 pF	CAP, CERM, 680 pF, 300 VAC, Y2	7 mm disc	DE2B3SA681KN3AX02F	MuRata
C_{INJ}	1	4.7 nF	CAP, CERM, 4.7 nF, 300 VAC, Y2	10 mm disc	DE2E3SA472MA3BX02F	MuRata
			CAP, FILM, 4.7 nF, 300 VAC, Y2	13 × 5 mm	R413F147050T1K	Kemet

4.3 PCB Layout

Figure 4-2 through Figure 4-7 show the PCB layout images, including 3D views, copper layers, assembly drawings, and layer stackup diagram. The PCB is 62-mils standard thickness with 1-oz copper on all layers.

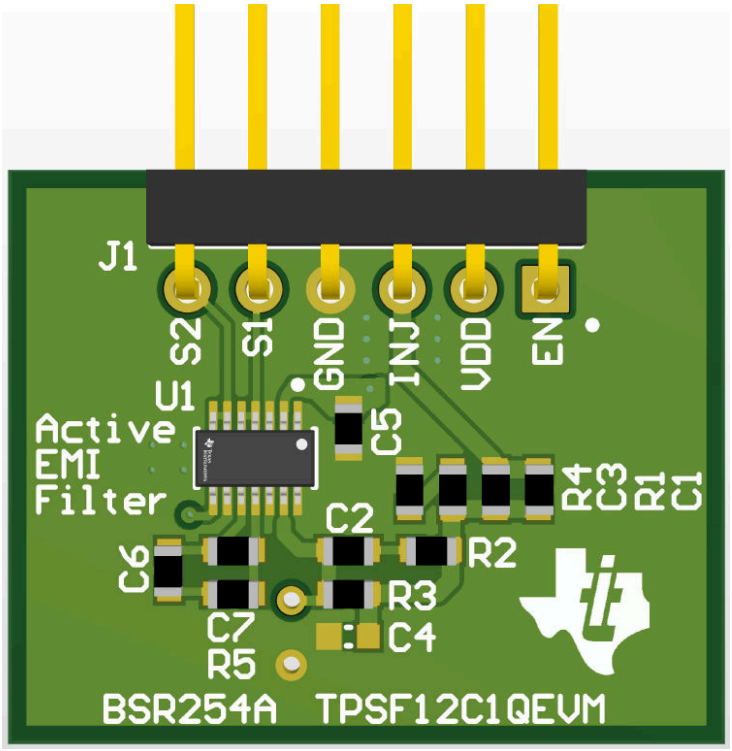


Figure 4-2. 3D Top View

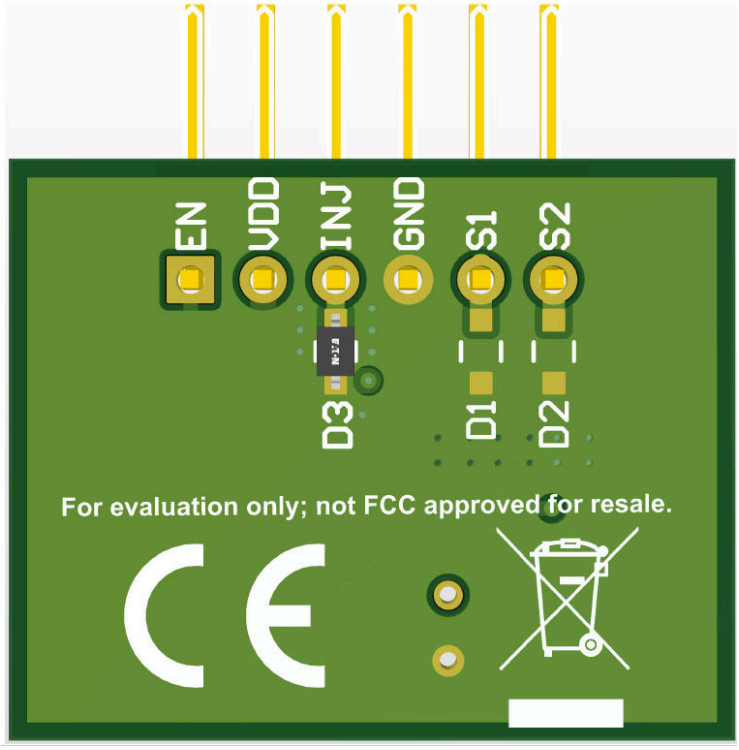


Figure 4-3. 3D Bottom View

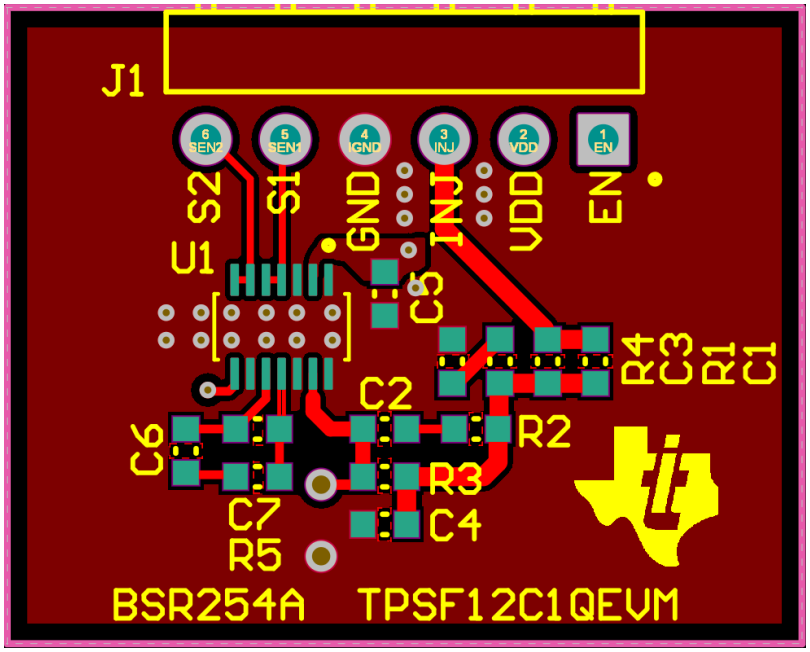


Figure 4-4. Top Layer Copper

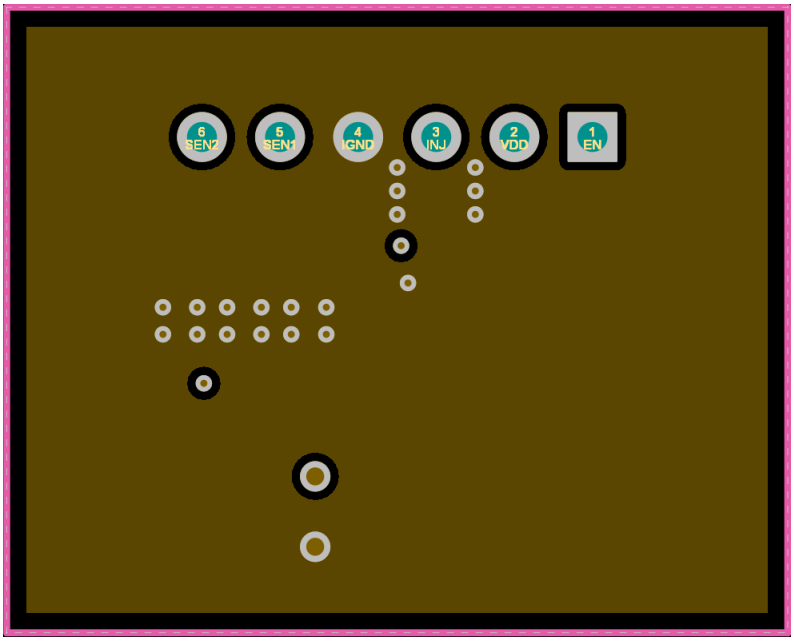


Figure 4-5. Layer 2 Copper

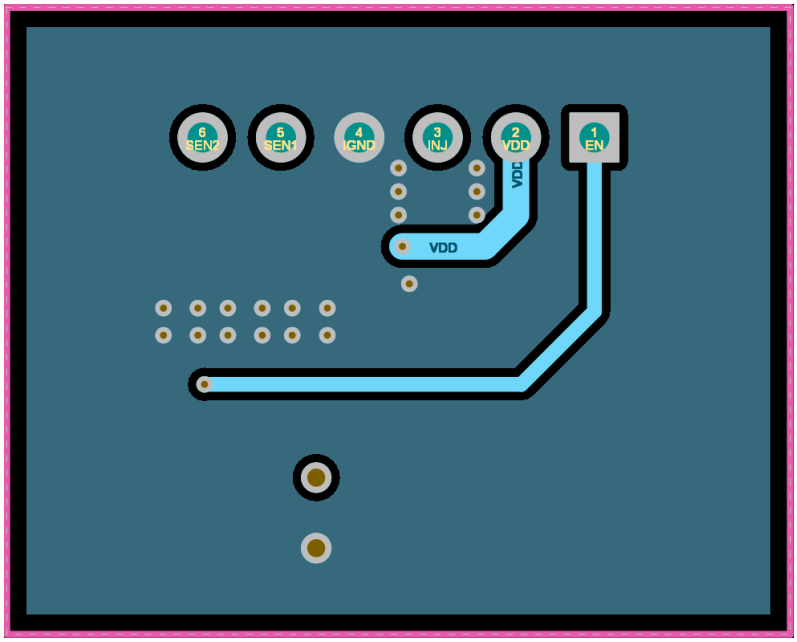


Figure 4-6. Layer 3 Copper

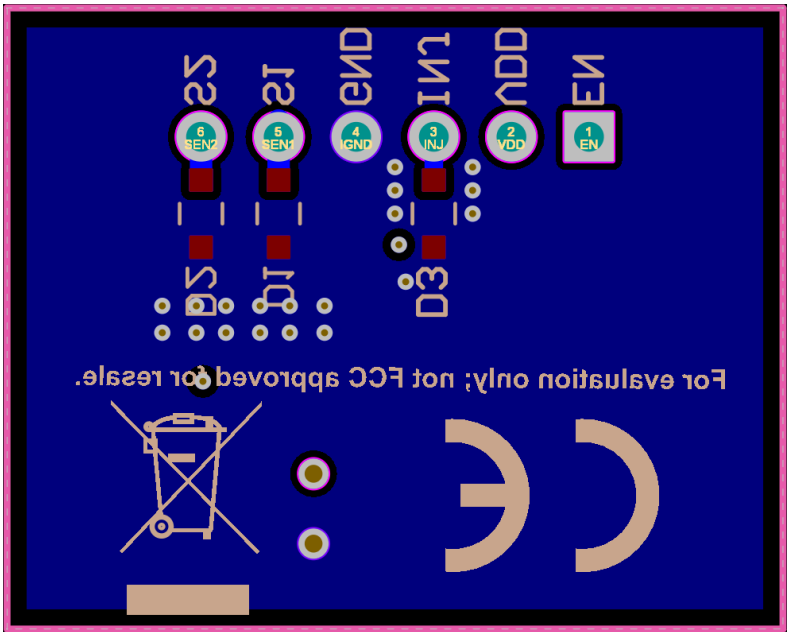


Figure 4-7. Bottom Layer Copper (Viewed From Top)

4.3.1 Assembly Drawings

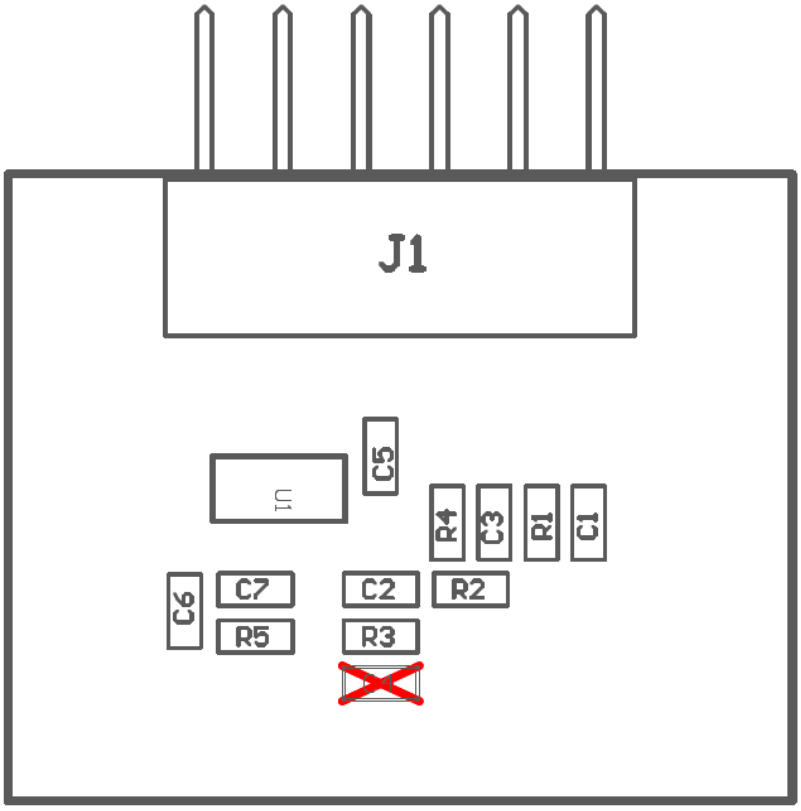


Figure 4-8. Top Assembly (Top View)

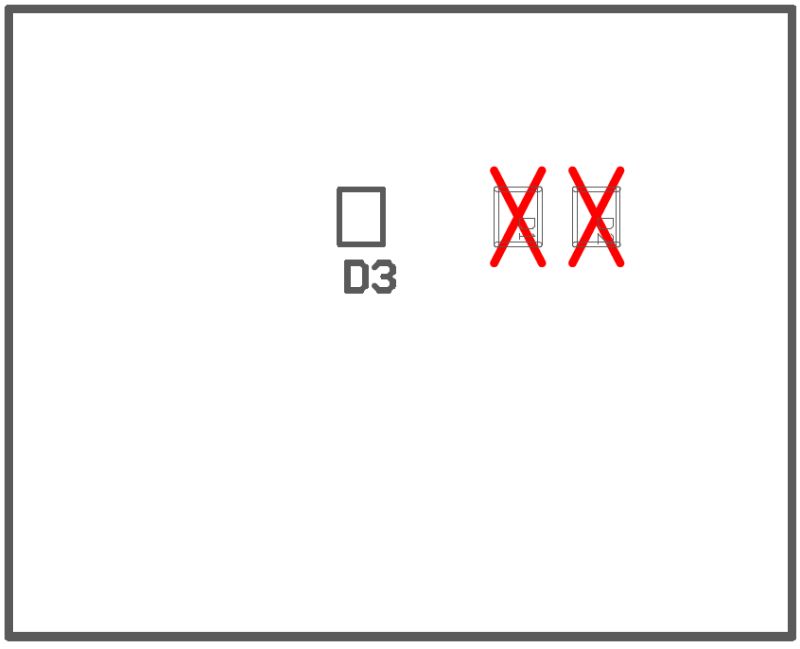


Figure 4-9. Bottom Assembly (Bottom View)

4.3.2 Multi-Layer Stackup

#	Name	Type	Material	Weight	Thickness	Dk
	Top Overlay	Overlay				
	Top Solder	Solder Mask	Solder Resist		0.4mil	3.5
1	Top Layer	Signal		1oz	1.4mil	
	Dielectric 1	Prepreg	FR-4 High Tg		7mil	4.2
2	Signal Layer 1	Signal		1oz	1.4mil	
	Dielectric 2	Core	FR-4 High Tg		41mil	4.2
3	Signal Layer 2	Signal		1oz	1.4mil	
	Dielectric 3	Prepreg	FR-4 High Tg		7mil	4.2
4	Bottom Layer	Signal		1oz	1.4mil	
	Bottom Solder	Solder Mask	Solder Resist		0.4mil	3.5
	Bottom Overlay	Overlay				

Figure 4-10. Layer Stackup

5 Compliance Information

5.1 Compliance and Certifications

- TPSF12C1QEVM EU Declaration of Conformity (DoC) for Restricting the use of Hazardous Substances (RoHS)

6 Additional Information

Trademarks

All trademarks are the property of their respective owners.

7 Related Documentation

7.1 Supplemental Content

For related documentation, see the following:

- Texas Instruments power-supply filter ICs
- Texas Instruments, press release *TI pioneers the industry's first stand-alone active EMI filter ICs, supporting high-density power supply designs*
- White Papers:
  - Texas Instruments, *How Active EMI Filter ICs Mitigate Common-Mode Emissions and Save PCB Space in Single- and Three-Phase Systems*
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *How a stand-alone active EMI filter IC shrinks common-mode filter size* technical article

To view a related EVM for the TPSF12C1 single-phase AEF device, see the TPSF12C1EVM-FILTER single-phase active EMI filter EVM for CM noise mitigation.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2022) to Revision A (July 2023)	Page
• Updated document to new template	1
• Changed the EVM photo	1
• Added *Device Information*	2
• Added *EVM Description*	4
• Changed *Setup* with new information on high-voltage and low-voltage testing	4
• Added information to *EVM Performance Validation* section	7

- Added *AEF Design Flow* section....8
- Added *AEF Circuit Optimization and Debug* section....10
- Changed EMI performance result in Figure 3-1 11
- Added thermal image....11
- Added *SENSE and INJ Voltages* 13
- Added insertion loss plot....13

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

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   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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