# Errata Report for the UCD90120 and UCD90124 Devices

## 1 PWM1 and PWM2 can not get set to 0% duty cycle (UCD90120 and UCD90124)

**Problem Description:** When either PWM1 or PWM2 (pins 31 and 32 respectively) are configured as PWM outputs and are set with duty cycle of 0%, then a small glitch occurs on that signal.

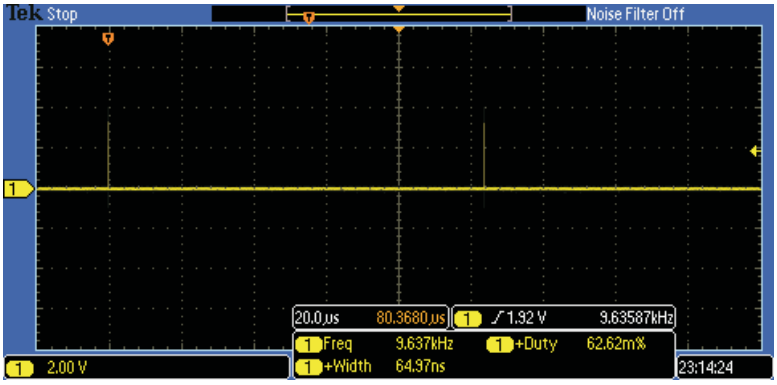


**Figure 1. Capture of glitch at PWM1 set to 0% duty cycle**

**Suggested Workaround:** If a glitch is not acceptable for a 0% setting of the duty cycle, then select from the other PWM pins available (PWM 3-4, FPWM 1-8).

## 2 PWM1 and PWM2 can not get set to 0% duty cycle with immediate speed updates set when controlling fans (UCD90124)

**Problem Description:** When the fan gets a new speed setting (manually or automatically adjusted), the percentage change in speed per second can be set in the FAN_CONFIG parameter "Speed change". For PWM1 or PWM2, if the fan is set for immediate speed updates and the fan is changed from any non-zero duty cycle setting to 0%, then the fan will stay at the non-zero duty cycle. If the fan was not set for immediate speed updates and the fan speed is changed from non-zero duty cycle to 0%, then the fan speed will walk down to 1% and stay there.

**Suggested Workaround:** If immediate speed update is desired then select the maximum speed update setting (8% per second) or select 1% as the desired end target duty cycle. Setting 1% in lieu of 0% for fan control is usually acceptable because most fans require a minimum duty cycle for them to operate.

## 3 Must configure FPWMs after PWMs (UCD90120 and UCD90124)

**Problem Description:** Configuring a PWM (pins 31, 32, 41 and 42) after a FPWM (pins 17-24) will corrupt the frequency setting for the FPWM. This problem is only observed when making direct $I^2C$/PMBus commands to reconfigure the PWM/FPWM pins.

**Suggested Workaround:** When using the PWM_CONFIG command, configure all PWMs before configuring any FPWMs.

## 4 Setting phase of 360° for FPWMs shuts down the FPWM (UCD90120 and UCD90124)

**Problem Description:** Setting the phase of an FPWM (pins 17-24) to 360° turns off the FPWM signal, forcing a 0V output.

**Suggested Workaround:** If setting the phase to 360° is required, then use 0° instead. Technically a phase of 0° is the same as a phase of 360°.

## 5 LOGGED_FAULT_DETAIL_INDEX can become invalid when using FIFO modes (UCD90120 and UCD90124)

**Problem Description:** If the LOGGED_FAULT_DETAIL is configured for one of the two FIFO modes, the LOGGED_FAULT_DETAIL_INDEX will be invalid after rollover and a reset. The “Total Number of LOGGED_FAULT_DETAIL entries” should be equal to the maximum number of LOGGED_FAULT_DETAIL entries. Instead, it is equal to the number of new entries since the rollover.

Example1:

1. The maximum fault detail entries is 10
2. The log is configured as a **full FIFO**
3. 12 faults are logged
4. The device is reset

The device reports that there are 2 log detail entries

Example 2:

1. The maximum fault detail entries is 10
2. The log is configured as a **half FIFO**
3. 12 faults are logged
4. The device is reset

The device reports that there are 7 log detail entries

In both cases, there are actually 10 valid log entries, but the device will not let you read past the number of entries that it reports.

**Suggested Workaround:** The log detail FIFO modes should not be used. Ensure that FIFO mode is disabled in the Miscellaneous Configuration Byte within the MISC_CONFIG command.

## 6 CLEAR_FAULTS command does not clear "Sequencing Timeout" and "Slaved Fault" bits (UCD90120 and UCD90124)

**Problem Description:** The CLEAR_FAULTS command does not clear the "Sequencing Timeout" and "Slaved Fault" status bits that are in the MFR_STATUS command for every rail.

**Suggested Workaround:** These bits get cleared when the associated rail is re-enabled.

## 7 Fan System Shutdown and fan Fault Increase Speed can't be used at the same time (UCD90124)

**Problem Description:** The fan System Shutdown Enable and the fan Fault Increase Speed that are set within the FAN_CONFIG command can not be used at the same time.

**Suggested Workaround:** Do not enable the fan System Shutdown Enable and the Fault Increase Speed at the same time.

## 8 Reading the GPIO_CONFIG for certain pins can change the state of the pin (UCD90120 and UCD90124)

**Problem Description:** Reading the GPIO_CONFIG for certain pins can change the state of the pin.

**Suggested Workaround:** Limit the use of GPIO_CONFIG command to only writes.

## 9 Using the Boolean Logic, GPOs defaulted to true show short glitch on GPO after a reset (UCD90120/UCD90124)

**Problem Description:** Any time that you have a GPO configured to a logic equation in which the default state is true when the device comes out of RESET, you will see a short glitch on the GPO. On a reset, the device initializes the GPOs to “false”, so if the condition is really supposed to be initialized to true, there will be a glitch.

**Suggested Workaround:** If a glitch is not acceptable on the GPO then may be able to add a filter on the GPO that would remove the glitch.

## 10 Command to Turn On rail ignored during a delayed Turn Off (UCD90120 and UCD90124)

**Problem Description:** When a rail is in the process of turning off with delay, it will ignore any command given to turn back on.

**Suggested Workaround:** Must ensure that turn on commands are given after the turn off delay has expired and the rail has actually turned off. If the commands were sent before the delay expires then the command should be resent once the delay expires.

## 11 Cautionary Use of PWM for Power Supply Margining (UCD90120 and UCD90124)

**Problem Description:** The UCD90120 and UCD90124 have two types of PWMs – Fast Pulsed Width Modulators (FPWM1–FPWM8) and generic PWMs (PWM1–PWM4). The product datasheet gives indication that all PWM types can be used for power supply margining.

It should be noted with this errata that caution must be taken when using PWM1–PWM4 for margining. Margining with a PWM seems to be acceptable when the appropriate external components are selected (per the application). While using any of PWM1–PWM4, a glitch may occur when the duty cycle is updated. This causes the rail output voltage to decrease below its permitted low voltage thresholds momentarily, and then go back to the desired margining setpoint. By selecting proper filter capacitor, that voltage dip can be reduced to ~2% below the setpoint.

**Suggested Workaround:** Although this might not be an issue for all applications, it is recommended that PWM1–PWM4 are not used for power supply margining. Using PWM1–PWM4 for margining is under application system designer’s discretion after evaluating actual operation in their system and determining that it is not an issue.

All FPWMs (FPWM1–FPWM8) operate as expected for power supply margining.

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