14-bit, 125-MSPS ADS5500 evaluation

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Introduction

The ADS5500 is a high-speed, pipeline, CMOS ADC with 14-bit resolution and a 125-MSPS sampling rate. In March 2004 Texas Instruments (TI) introduced the device, which is the first ADC in the world market with such high sampling speed and high resolution. The ADS5500 is suitable for applications such as wireless communication, test and measurement instrumentation, control systems, medical imaging, and high-speed digitization.

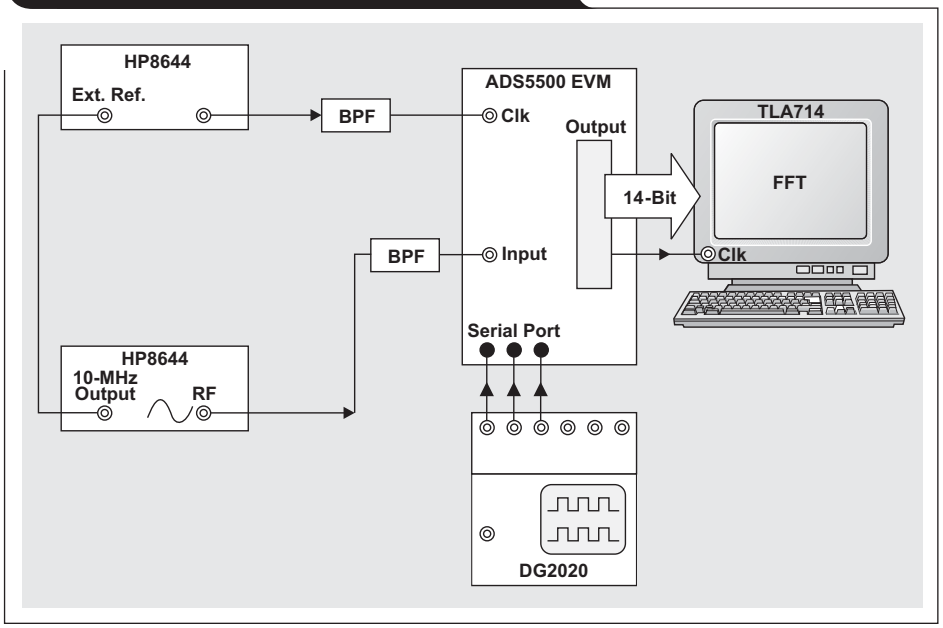
The ADS5500 consists of an input sample-and-hold stage; a 14-bit, pipeline ADC core; an internal voltage reference; a clocking circuit; digital error correction; a digital output driver; and a single 3.3-V voltage supply. The leading features and advantages of the ADS5500 are a wide signal input bandwidth of 750 MHz, a large dynamic differential input-signal range of 2.3 V peak-to-peak, a high signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) at wide frequency range, a good SNR of up to 74 dBFS with low signal amplitude for receiver applications, and very low power dissipation (780 mW) at normal operation with a large load.[1] For example, with a 125-MSPS sampling rate, a –1-dBFS signal amplitude, and an input frequency of 190 MHz with proper input configuration, the ADS5500 has a typical SNR of about 70 dB and an SFDR above 82 dB. With the same sampling frequency, the same input frequency, and a –15-dBFS input signal amplitude, the ADS5500 has an SNR of 74 dBFS and an SFDR of 83 dBFS.

Since the ADS5500 has such high performance, it has a wide application; however, because of its high speed and high resolution, the device is sometimes challenging to evaluate. For this reason, this article introduces an ADS5500 evaluation system that includes the test equipment, system configuration, test circuit, basic high-speed ADC test concept, and test data.

The ADS5500 test system

One of the ADS5500 bench test systems used for dynamic performance evaluation is shown in Figure 1. It basically consists of a signal source (HP8644), a clock source (HP8644), a digital logic analyzer (TLA714), a data generator (DG2020), bandpass filters (BPFs), a test board, and a fast Fourier transform (FFT) program. The signal source generates a pure tone signal with the amplitude and frequency necessary to test the ADS5500. The clock source generates a sine wave to trigger an external clock circuit of the ADS5500, which can be a transformer or PECL driver to produce an ideal sampling clock. The data generator is used to generate serial data for the control register. The Tektronix digital logic analyzer (TLA) is used to capture the data from the ADS5500 and analyze it with the FFT. If

Figure 1. ADS5500 bench evaluation system



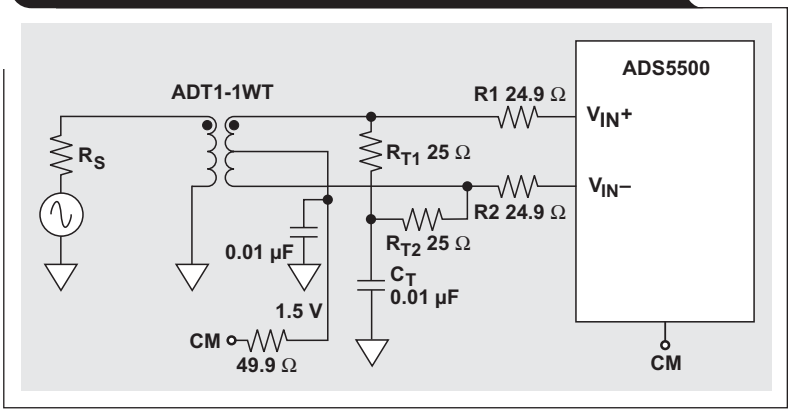
no such instrumentation is available, a FIFO or an FPGA board with a PC can be used as a TLA or data generator.

Some important specifications of the instrumentation in this system are signal frequency bandwidth, signal power, source impedance, noise, harmonics, jitter, phase lock function, and the ADS5500 digital load. The low input capacitance of devices such as the digital buffer, digital data capture board, or logic analyzer is important. The logic analyzer shown in Figure 1 has a 2-pF input capacitance. The maximum digital output load of the ADS5500 is 12 pF; a larger load will affect the ADS5500 evaluation. The timing between the data capture clock and the ADC output data can affect the test result if an external capture clock is used, so the timing must meet the data sheet specification. Data must be captured during the data-valid time. Using the ADS5500 output clock to capture ADS5500 data is strongly recommended, since the output clock is synchronized with the output data. There is a delay variation between the input clock and the output clock across devices and temperature as well as supply voltage; therefore, using the input clock for output data capture is less preferred and is not recommended, particularly at high speeds.

On the analog side of the ADS5500, all the signal and clock generators shown in Figure 1 have phase lock function, low-noise mode (Mode 3), 50-Ω source impedance, and 20-dBm source power. To avoid energy reflection on the signal transmission path, the equivalent input impedance of the ADC, including the external input circuit, should match the source impedance. This is shown in Figure 2, a configuration similar to one shown in Reference 2. At very high input frequency with certain test conditions, the source may not have enough power for the ADC due to the attenuation from the BPF and input circuit. In this case a wideband amplifier (for example, the THS900x or ZHL-6A) with a certain gain and a 50-Ω input/output impedance is needed to provide sufficient power to the ADS5500. Properly reducing R1 and R2 and increasing R_{T1} and R_{T2} will reduce the power requirement from the source at very high input frequency.

In a real test system, a BPF is used in the ADS5500 signal input path to minimize the harmonics and noise from the source. A narrow BPF is also used in the clock input path to minimize jitter from the clock source and to provide a good clock duty cycle when the sampling speed is very high. The bench test shows that with or without a BPF on the input signal path, the FFT result is dramatically different. The bench test also shows that, with the system in Figure 1 and a high input frequency, a narrow (3-MHz-bandwidth) BPF on the signal input path results in an SNR at least 0.3 dB better than a wide (10-MHz-bandwidth) BPF. The BPF on the clock input path can improve SNR more than 0.5 dB and SFDR more than 2 dB on the current EVM board with a 125-MHz clock and a very high input frequency. In any case the BPF itself should be tested to make sure it is functioning well. The input and output impedance of the BPF should be matched with the signal source impedance and the ADC input impedance. A good BPF choice would be the TTE KC series with a stopband attenuation of 50 dBC (minimum) to optimize the evaluation.

Figure 2. Differential transformer input configuration for ADS5500 evaluation

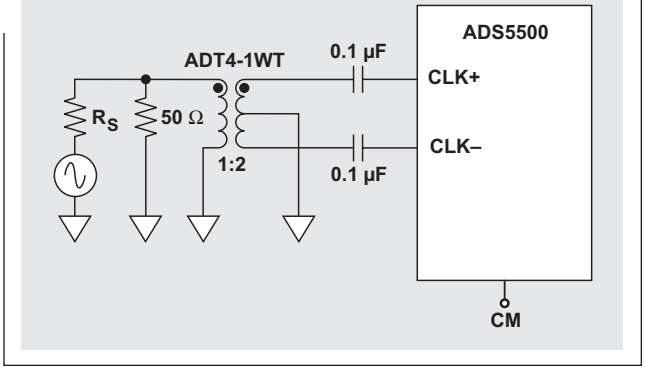


In the ADS5500 test it was observed that the ADS5500 performance is sensitive to the system jitter, analog input configuration, and test-board layout. These are discussed in the following sections.

The clock requirement

For the best evaluation, the ADS5500 requires its input clock to have low jitter; a 50% duty cycle; and a differential amplitude of 3 V_{PP} if the input clock signal is a sine wave, or 1.5 V_{PP} if it is a pulse. A sharper input clock signal edge provides a better SNR. The ADS5500 internally supports a dc offset voltage to the internal input clock circuit; therefore, a clock ac coupling path is recommended. To provide a sharp clock signal edge and the lowest external circuit noise and thus to get the best performance from the ADS5500 EVM, a 1:2 turns ratio transformer is used to couple a sine wave into the ADS5500 clock input as shown in Figure 3.[2] With a high clock frequency, using a BPF such as the TTE KC4T-125M-3M-50-69A BPF on the input

Figure 3. Sine wave clock input circuit for the ADS5500 evaluation



clock path is recommended if necessary to reduce the clock jitter noise from the source. To preserve the excellent ac performance of the ADS5500 and get the best evaluation, a low-jitter clock for this test is critical because the ADS5500 itself has a very low jitter of about 300 fs.[1] Any input clock circuit or driver must not carry extra jitter. Generally, as the input frequency increases, the clock jitter becomes more dominant in the system for maintaining a good SNR. The following equation can be used to calculate the achievable SNR for a given input frequency and system jitter in psrms.

$$\mathrm{SNR} = 20\log\frac{1}{2\pi f_{IN} t_{ja}},$$

where t_{ja} is the rms aperture jitter from all jitter sources such as the clock edge, input signal, test board, and device; and f_{IN} is the input frequency.

In addition, the input clock is treated as an analog signal, and its power supply should be separated from the digital driver power supply to limit the digital noise.

Analog input configuration

The analog input configuration of the ADS5500 is important for the evaluation and typically includes a transformer-coupled differential input (see Figure 2) or an operational amplifier-driven differential input (see Figure 4). This configuration can be found in Reference 2. The transformer configuration provides low noise and harmonics over a wide frequency range. It also provides ac coupling, differential input, and a wide signal bandpass, making it a good way to evaluate the ADS5500 even though the transformer has some insertion loss. The op amp, widely used for signal conditioning and power boosting, is also used for dc coupling.

In the transformer configuration, the input impedance of the ADS5500 is an important consideration. The ADS5500 input impedance is capacitive and is the function of both the sampling clock frequency and the input signal frequency. When the sampling and input frequency speeds are relatively low, the ADS5500 input impedance is relatively high, and matching the source impedance is not difficult. When the sampling speed is very high (at 125 MHz) and the input frequency is very high (above 150 MHz), the input impedance of the ADC is low. In this case the equivalent input impedance could be smaller than 50 Ω, which may cause a mismatch with the source impedance and require more source current. This needs to be accounted for in the evaluation.

Figure 2 shows a transformer-coupled analog input circuit for the evaluation of the ADS5500. R_{T1} and R_{T2} are the termination resistors for the source impedance match; they also form the low-pass filter with C_T. We have seen that at input frequencies below 150 MHz, $R_{T1} + R_{T2} = 50\ \Omega$ provides the best SNR and SFDR; while at input frequencies above 150 MHz, higher values of R_{T1} and R_{T2} can be used in the evaluation due to low ADC input impedance and high transformer roll-off. R1 and R2 are the analog input serial resistors for isolation between the ADC switch capacitor input and the signal source. They also form a low-pass filter with the ADS5500 input capacitance. Proper R1 and R2 values are needed for the best performance. If R1 and R2 are too small, the SFDR could decrease; and if they are too big, the signal source power will increase. We have seen that a value of 25 Ω for R1 and R2 provides the best result when a transformer coupling is used in the input circuit. In Reference 2, two transformers are used in the input circuit to reach the best differential signal balance; but this causes a 9-dB input signal roll-off from 70 MHz to 350 MHz at the front end of the ADC and requires a large signal source. For this reason only one transformer was used in some tests. We have seen that there is no significant difference in the performance whether one or two transformers is used. The transformer is used in our test for signal ac coupling and single-ended to differential signal conversion.

Figure 4. The op amp input configuration for ADS5500 evaluation

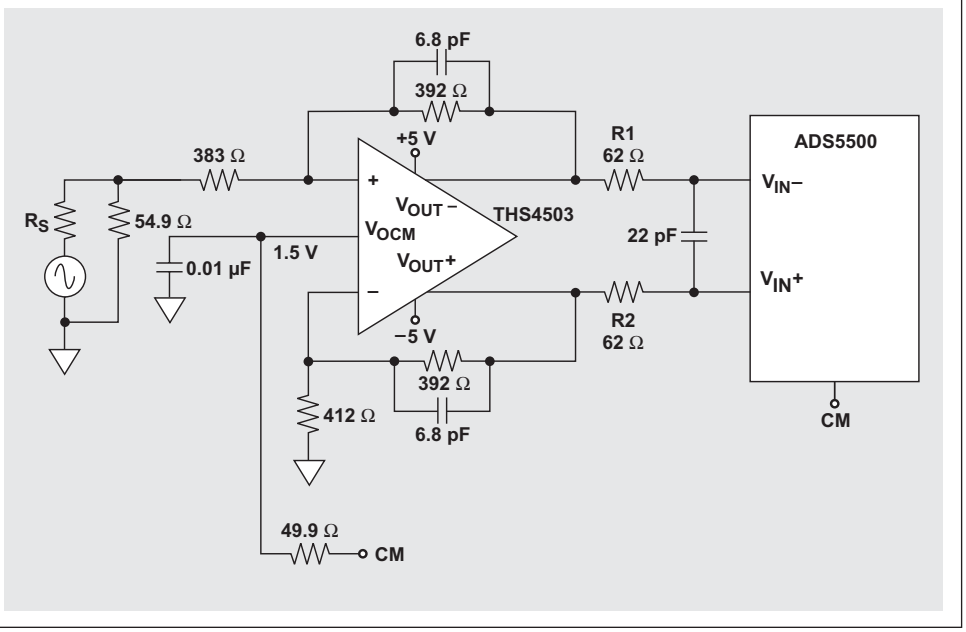


Figure 4 shows the ADS5500 EVM configuration used to evaluate the ADS5500 when the input signal is driven by the THS4503 fully differential op amp. The dc-coupled THS4503 is set for unity gain by the input and feedback resistors. A low-pass filter is set by the feedback resistor and capacitors on the feedback paths to limit signal

bandwidth. The THS4503 receives a single-ended analog signal and dc offset voltage, then outputs a differential signal with the dc offset voltage for the ADS5500. A small (22-pF) input capacitor is needed to form a low-pass filter with serial resistors R1 and R2. The serial resistors are important for isolation between the op amp and the ADC input stage. A value around 60 Ω is chosen for these resistors in the circuit. With this configuration the ADS5500 can provide good performance with input frequencies of up to 20 MHz. This is described later under "ADS5500 test data."

Board layout and decoupling

The evaluation board layout and signal decoupling are equally important factors in the ADS5500's performance. The ADS5500 package is designed with the analog inputs on one side and the digital outputs on the other, providing good physical isolation between them. To achieve optimum ADS5500 performance, it is important to use a short signal trace, separated digital and analog signal locations, and ground planes with a multilayer board. When the analog inputs to the ADS5500 are driven differentially, it is especially important to make the layout highly symmetrical to avoid phase differences between the two signal paths, as an asymmetrical parasitic on the PCB creates input signal distortion. The differential input clock signal traces should be symmetrical and short to avoid mismatches in propagation delays. The clock lines should not cross any other signal traces. Short circuit traces on the digital outputs will minimize capacitive loading.

The ADS5500 must be treated as an analog component, and its power supply pins should be connected to the analog supply. For the best performance, the analog supply (AV_{DD}) and the digital driver supply (VDRV) should be separated to limit substantial current transient noise from the digital driver. The VDRV pins must also be connected to a low-noise supply. The supply voltage must be thoroughly filtered before connecting to the supply of the converter. The recommended supply decoupling scheme for the ADS5500 is shown in Reference 2. All supply pins can be bypassed with a combination of 0.1-µF ceramic capacitors and a 10-µF tantalum tank capacitor or ceramic capacitor. To minimize the lead and trace inductance, the capacitors must be located as close to the supply pins as possible. In addition, larger (10-µF to 47-µF) bipolar decoupling capacitors effective at lower frequencies must be used on the main supply pins.[2] All ground connections on the ADS5500 are internally bonded to the metal flag (bottom of the package) that forms a large ground plane. All ground pins must directly connect to the analog ground plane that is under the converter. All the supply pins and reference pins must be sufficiently bypassed due to the clock feedthrough (switch noise) caused by the high-frequency clock of the ADS5500. Insufficient bypassing will add noise to the conversion process. Besides the factors already discussed, others affecting SNR and SFDR, such as external bias resistance, the serial port, the digital output load, the external buffer, etc., can contribute a small performance variation to the evaluation.

FFT analysis

In the ADS5500 dynamic performance evaluation, the FFT is used to determine the SNR, total harmonic distortion (THD), and SFDR of the device in the test system shown in Figure 1. The FFT signal frequency domain analysis provides a signal spectrum. When a pure tone signal passes through a nonideal or real system, the signal spectrum always changes. The changed signal spectrum presents the system dynamic characteristics.

When a high-performance ADC is tested, a perfectly synchronized system is critical. Therefore the user must make sure that the input signal and sampling clock sources are synchronized and that they meet the following coherent sampling requirement to avoid spectrum leakage on the FFT.

$$f_{IN} = m\frac{f_S}{N},$$

where f_{IN} is the input signal frequency, f_S is the sampling clock frequency, N is the sampling size, and m is an odd number. If coherent sampling can't be ensured, then windowing techniques can be used in the FFT.[3]

ADS5500 test data

As good application examples of this test system, some test data is presented here for users whose designs are not covered by the current ADS5500 data sheet.[2] This data includes an FFT at very high input frequency; two-tone intermodulation distortion (IMD); an FFT of the ADS5500 combined with an op amp; as well as differential nonlinearity (DNL) and integral nonlinearity (INL). The data is measured using an EVM similar to the ADS5500 EVM shown in Reference 2. Some of this data is better than the data sheet specification because the test system used here was optimally set for the frequency conditions.

Figure 5 shows an FFT plot of the ADS5500 with a very high input frequency and a 125-MHz sampling clock through a transformer-coupled differential input configuration. The input frequency is 190 MHz and the amplitude is –1 dBFS. The FFT analysis shows that the SNR is 69.6 dBFS and

Figure 5. FFT plot of ADS5500 with 190-MHz input frequency and 125-MHz sampling clock

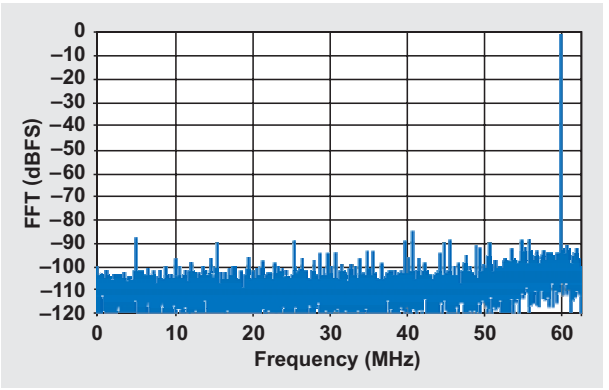
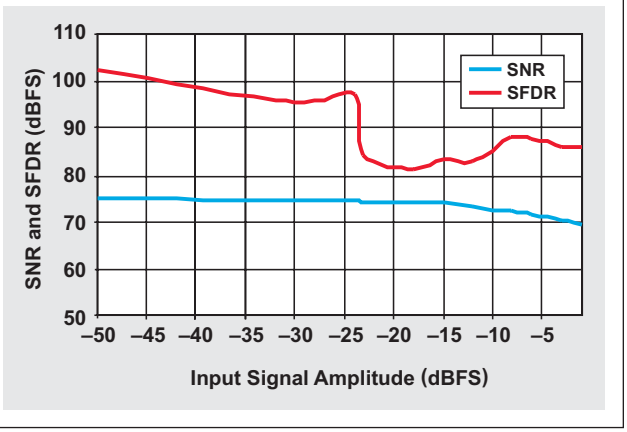


Figure 6. Dynamic performance of ADS5500 with different input amplitudes, 190-MHz input frequency, and 125-MHz sampling clock



the SFDR is 85 dBFS. In this case the input impedance due to R_{T1} and R_{T2} is about 200 Ω, and R1 and R2 are each less than 25 Ω in the input circuit.

Figure 6 shows the dynamic performance of the ADS5500 with different input amplitudes, a 190-MHz input frequency, and a 125-MHz sampling clock. This data shows that at such a high input frequency and with low input amplitudes, the ADS5500 has a 74-dBFS SNR and a high SFDR.

Figure 7, Figure 8, and Table 1 show the two-tone IMD test data of the ADS5500 in an undersampling condition. This test uses the ADS5500 EVM shown in Reference 2. The test signal is a two-tone signal combined from two sine waves with different frequencies, such as any two frequencies above the ADC's Nyquist frequency with a 1-MHz separation. The two-tone signal amplitude should not exceed the ADS5500's full scale. Just as with a single-tone FFT, when the signal amplitude is higher, the spur and IMD from the ADC are higher. In this test the amplitude of –7 dBFS or –10 dBFS for each tone is used, providing the ADS5500 with a combined input signal at full scale or 3 dB below full scale. The input signal frequency ranges from 76 to 125 MHz, and the clock frequency ranges from 96 to 125 MHz. The IMD rejection is the ratio of the rms value of one input tone to the value of the worst third-order intermodulation product.

Figures 7 and 8 show FFT plots for two different sampling speeds at an input amplitude of –10 dBFS for each tone. In Figure 7 the two-tone SFDR is 96 dBFS with about a 100-MHz input frequency, a 1-MHz separation, and a 125-MHz sampling clock. In Figure 8 the two-tone SFDR is 97 dBFS with about a 125-MHz input frequency, a 1-MHz separation, and a 96.5-MHz sampling clock.

Figure 7. Two-tone IMD of ADS5500 with 100-MHz input frequency, 1-MHz separation, and 125-MHz sampling clock

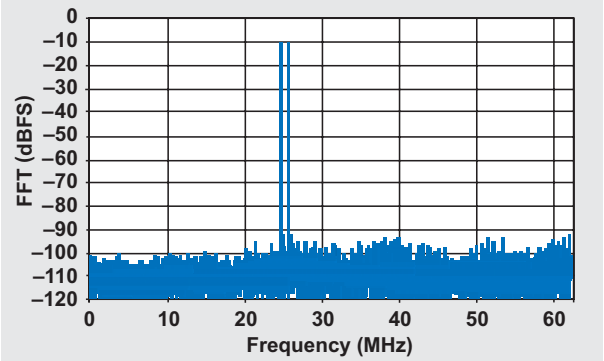


Figure 8. Two-tone IMD of ADS5500 with 125-MHz input frequency, 1-MHz separation, and 96.5-MHz sampling clock

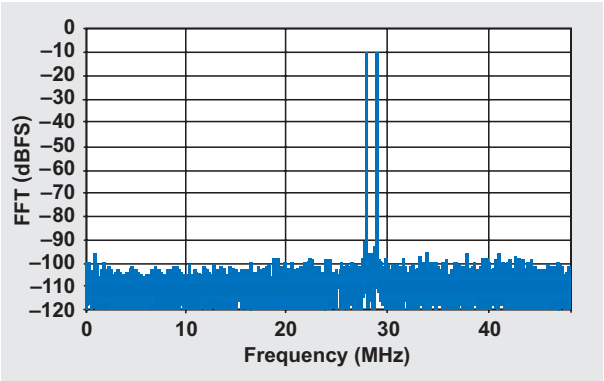


Table 1. Two-tone IMD of ADS5500

CLK (MHz)	INPUT FREQUENCY 1 (MHz)	INPUT FREQUENCY 2 (MHz)	SFDR (dBFS)	IMD REJECTION (dBFS)	IMD2 (dBFS)	IMD3 (dBFS)	AMPLITUDE (dBFS)
125	99.0	100.0	96	—	98	94	–10
125	81.0	82.0	95	—	104	92	–10
125	99.0	100.0	—	87	95	86	–7
125	81.0	82.0	—	88	102	88	–7
102.4	76.1	77.1	91	—	101	93	–10
102.4	76.1	77.1	—	95	101	91	–7
96.5	124.5	125.5	97	—	102	97	–10
96.5	124.5	125.5	—	83	97	81	–7

Table 1 shows that with a 125-MHz sampling clock and an 80- to 100-MHz input frequency, the two-tone IMD rejection is above 87 dBFS at full-scale input (–7-dBFS input amplitude for each tone). Table 1 also shows the ADS5500's good undersampling IMD performance with a 96.5- to 125-MHz sampling clock and a 76- to 125-MHz input frequency. This data shows that the ADS5500 has leading IMD performance at such high input frequencies and sampling speeds.

Figure 9 shows the dynamic performance of the ADS5500 and THS4503 combined. This data is measured on the circuit shown in Figure 4 with a 125-MHz sampling clock and different input frequencies. Note that the serial resistors R1 and R2 in Figure 4 each have a value of 62 Ω instead of 25 Ω as mentioned in Reference 2. The data shows that with the THS4503, at input frequencies of up to 18 MHz, the ADS5500 can provide an SNR of 71 dBFS and an SFDR above 86 dBFS. At input frequencies above 20 MHz, the performance starts degrading due to the bandwidth limitation of the THS4503. The THS4503 is a fully differential op amp; detailed information can be found in Reference 4. For wideband applications with an op amp input configuration, the OPA695 is recommended.[5]

The linearity of the ADS5500 is important in its applications. Two specifications, DNL and INL, are used to describe ADC nonlinearity. DNL is measured from sampling a pure sine wave with a large sample size, then calculating the deviation of the transition from each code. INL is integrated from DNL. Figure 10, Figure 11, and Table 2 show a typical linearity measurement of the ADS5500 from the test system just discussed and a typical EVM board. With a 125-MHz sampling clock, an input frequency of 10 MHz, and at room temperature, the maximum/minimum DNL is ±0.5 LSB, and the maximum/minimum INL is ±2.5 LSB. Table 2 shows that the ADS5500 has good linearity, with similar DNL/INL at input frequencies of 10, 45, and 100 MHz.

Table 2. DNL/INL of ADS5500 vs. input frequency with 125-MHz sampling clock

INPUT FREQUENCY (MHz)	MAX/MIN DNL (LSB)	MAX/MIN INL (LSB)	MISS CODE
10	0.46/–0.52	2.44/–2.40	0
45	0.47/–0.48	2.59/–2.57	0
100	0.43/–0.44	2.05/–3.05	0

Figure 9. Dynamic performance of ADS5500 with THS4503 vs. input frequency with 125-MHz sampling clock

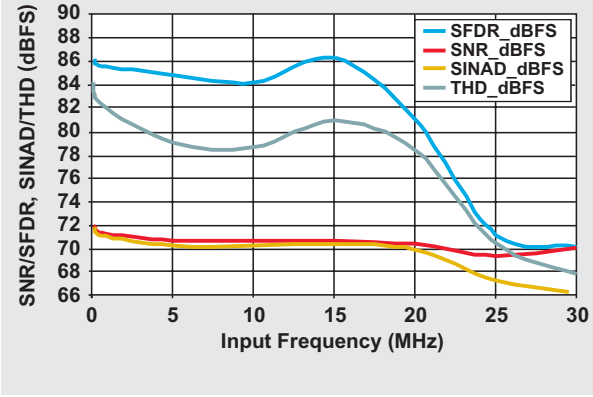


Figure 10. ADS5500 DNL with 10-MHz input frequency and 125-MHz sampling clock

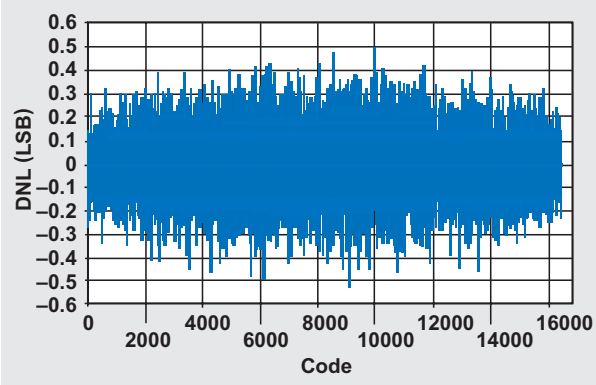
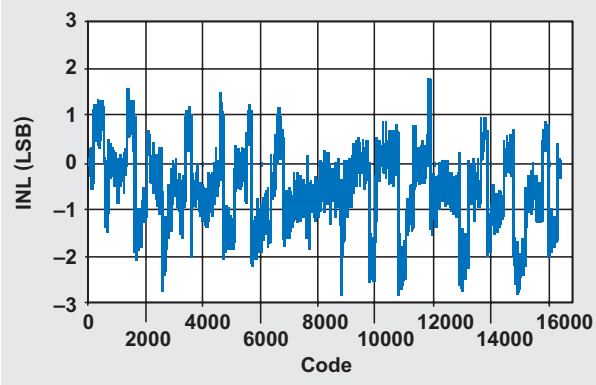


Figure 11. ADS5500 INL with 10-MHz input frequency and 125-MHz sampling clock



Conclusion

The ADS5500 is a very high-performance device with wide application, but evaluating it can present some test setup challenges due to its high frequency and high resolution. This article has introduced an ADS5500 evaluation system including the test equipment, system configuration, test circuit, clock requirements, basic high-speed ADC test concept, and test data. This evaluation has shown the leading performance advantages of the ADS5500: wide signal input bandwidth, large dynamic differential input signal range, high SNR and SFDR over a wide frequency range, good SNR of up to 74 dBFS with a low signal amplitude for receiver applications, and very low power dissipation with a high (125-MSPS) sampling rate.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "14-Bit, 125MSPS Analog-to-Digital Converter," ADS5500 Data Sheet	sbas303
2. "ADS5500/5541/5542/5520/5521/5522 14- and 12-Bit Single Channel ADC EVM," User's Guide	slwu010
3. Alan V. Oppenheim, *Discrete-Time Signal Processing* (Prentice-Hall, Inc., 1989).	—
4. "Wideband, Low-Distortion Fully Differential Amplifiers," THS4502/4503 Data Sheet	slos352
5. "Ultra-Wideband, Current-Feedback Operational Amplifier With Disable," OPA695 Data Sheet	sbos293

Related Web sites

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C011905

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