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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Clock jitter analyzed in the time domain, Part 1

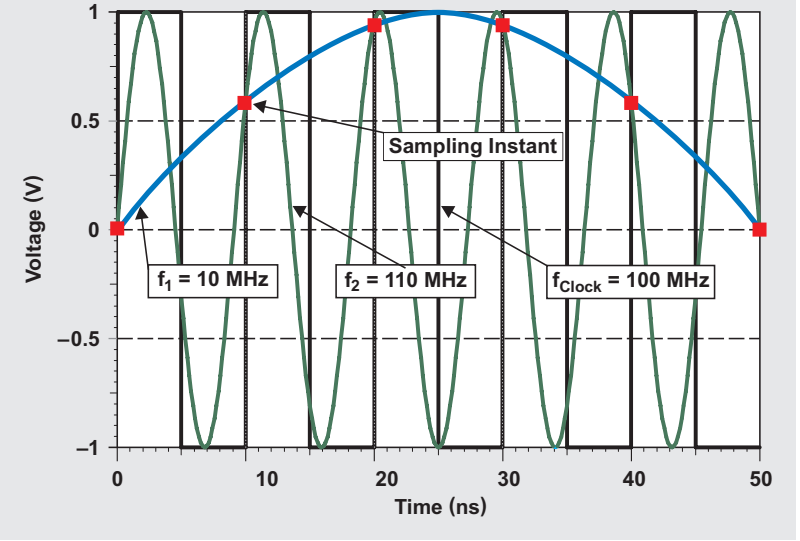
By Thomas Neu
Systems and Applications Engineer

Introduction

Newer high-speed ADCs come outfitted with a large analog-input bandwidth (about three to six times the maximum sampling frequency) so they can be used in undersampling applications. Recent advances in ADC design extend the usable input range significantly so that system designers can eliminate at least one intermediate frequency stage, which reduces cost and power consumption. In the design of an undersampling receiver, special attention has to be given to the sampling clock, because at higher input frequencies the jitter of the clock becomes a dominant factor in limiting the signal-to-noise ratio (SNR).

Part 1 of this three-part article series focuses on how to accurately estimate jitter from a clock source and combine it with the aperture jitter of the ADC. In Part 2, that combined jitter will be used to calculate the ADC's SNR, which will then be compared against actual measurements. Part 3 will show how to further increase the SNR of the ADC by improving the ADC's aperture jitter, with a focus on optimizing the slew rate of the clock signal.

Figure 1. Two input signals sampled at 100 MSPS show the same sample points due to aliasing



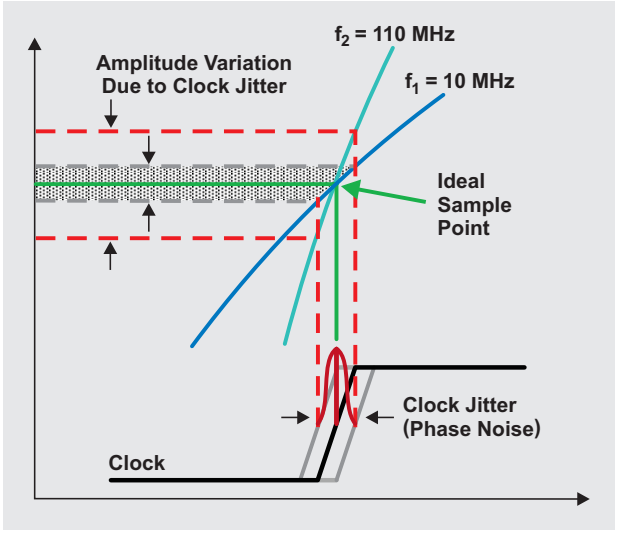
Review of the sampling process

According to the Nyquist-Shannon sampling theorem, the original input signal can be fully reconstructed if it is sampled at a rate that is at least two times its maximum frequency. Assuming that an input signal of up to 10 MHz is sampled at 100 MSPS, it doesn't matter whether the signal is located in the baseband (the first Nyquist zone) at 0 to 10 MHz or undersampled in a higher Nyquist zone at 100 to 110 MHz (see Figure 1). (Sampling in a higher [second, third, etc.] Nyquist zone is commonly referred to as undersampling or subsampling.) However, proper anti-aliasing filtering is required in front of the ADC to sample the desired Nyquist zone and to avoid confusion when the original signal is being reconstructed.

Jitter in the time domain

Looking closely at one sampling point reveals how timing uncertainty (clock jitter or clock phase noise) creates amplitude variation. As the input frequency increases due to undersampling in a higher Nyquist zone (e.g., from f_1 = 10 MHz to f_2 = 110 MHz), a fixed amount of clock jitter generates a larger amount of amplitude deviation (noise)

Figure 2. Clock jitter creates more amplitude error with faster input signals



from the ideal sample point. Furthermore, Figure 2 suggests that the slew rate of the clock signal itself has an impact on variations in the sampling instant. The slew rate

determines how fast the clock signal passes through the zero crossing point. In other words, the slew rate directly impacts the trigger threshold of the clock circuitry inside the ADC.

If there is a fixed amount of thermal noise on the internal clock buffer of the ADC, then the slew rate gets converted into timing uncertainty as well, which degrades the inherent aperture jitter of the ADC. As can be seen in Figure 3, the aperture jitter is completely independent of the clock jitter (phase noise), but those two jitter components combine at the sampling instant. Figure 3 also shows that the aperture jitter increases as the slew rate decreases. The slew rate is usually directly dependent on the clock amplitude.

SNR degradation caused by clock jitter

There are several factors that limit the SNR of the ADC, such as quantization noise (typically not noticeable in pipeline converters), thermal noise (which limits the SNR at low input frequencies), and clock jitter (SNR_{Jitter}) (see Equation 1 below). The SNR_{Jitter} component, which is limited by the input frequency, f_{IN} (depending on the Nyquist zone), and by the total amount of clock jitter, t_{Jitter}, can be calculated as

$$SNR_{Jitter}\left[dBc\right] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}). \quad (2)$$

As expected, with a fixed amount of clock jitter, the SNR degrades as the input frequency increases. This is illustrated in Figure 4, which shows the SNR of a 14-bit pipeline converter with a fixed clock jitter of 400 fs. If the input frequency increases by one decade, such as from 10 MHz to 100 MHz, the maximum achievable SNR due to clock jitter is reduced by 20 dB.

As already mentioned, another major factor that limits the ADC's SNR is the ADC's thermal noise, which doesn't change with input frequency. A 14-bit pipeline converter typically has a thermal noise of ~70 to 74 dB, also shown in Figure 4. The ADC's thermal noise, which can be found in the data sheet, is equivalent to the SNR at the lowest specified input frequency (10 MHz in this example), where clock jitter is not yet a factor.

Let's analyze the 14-bit ADC with a thermal noise of ~73 dB and a clock circuitry with 400 fs of jitter. At low input frequencies such as 10 MHz, the SNR of this ADC is pretty much defined by its thermal noise. As the input frequency increases, the 400-fs clock jitter gets more and more dominant until it completely takes over at ~300 MHz. Even though the SNR due to clock jitter at an input frequency of 100 MHz is reduced by 20 dB per decade compared to the SNR at 10 MHz, the total SNR is degraded by only

Figure 3. Clock jitter and ADC aperture jitter combine at sampling instant

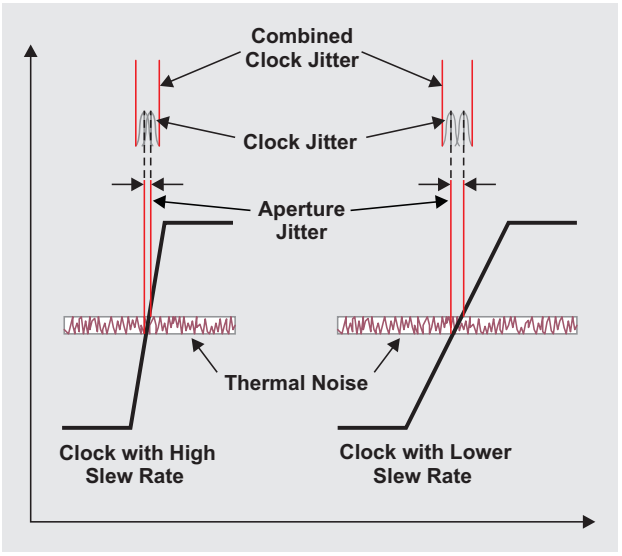
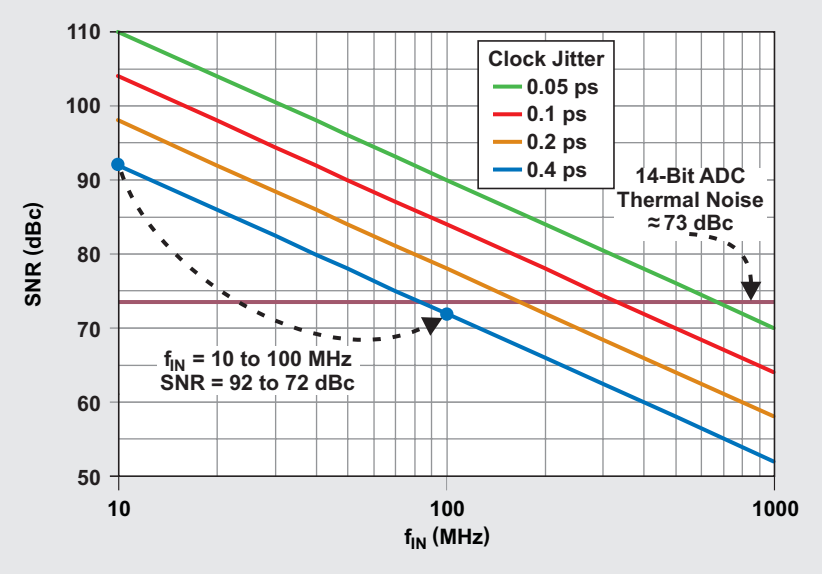
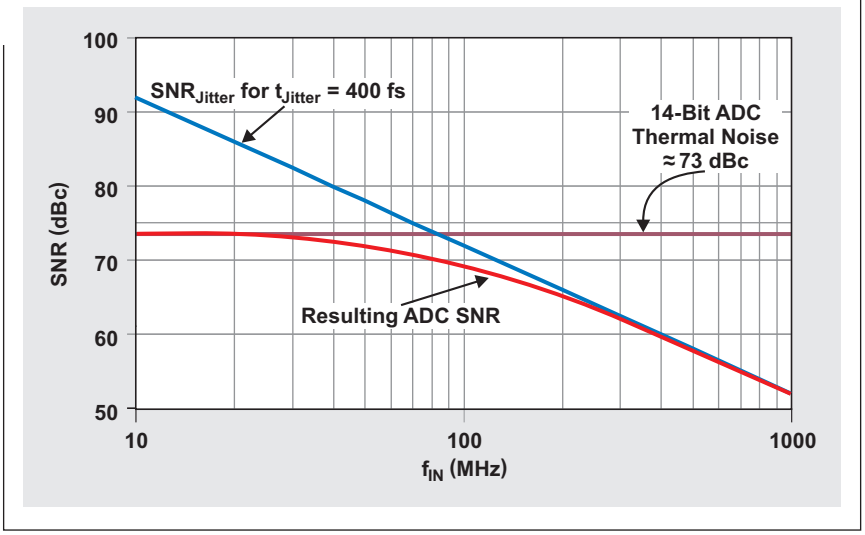


Figure 4. Fixed 400-fs clock jitter reduces SNR by 20 dB per decade



$$SNR_{ADC}\left[dBc\right] = -20 \times \log \sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

Figure 5. Resulting ADC SNR is limited by thermal noise and clock jitter



~3.5 dB (down to 69.5 dB) because of the 73-dB thermal noise (see Figure 5):

$$SNR_{Jitter} = -20 \times \log(2\pi \times 100\ MHz \times 400\ fs) = 72\ dBc$$

$$SNR_{ADC} = -20 \times \log\sqrt{\left(10^{-\frac{73\ dBc}{20}}\right)^2 + \left(10^{-\frac{72\ dBc}{20}}\right)^2} = 69.5\ dBc$$

Now it becomes obvious that if the ADC's thermal noise increases, the clock jitter will become very important when higher input frequencies are sampled. A 16-bit ADC, for example, has a thermal noise floor of ~77 to 80 dB. According to the curves in Figure 4, in order to minimize the effect of clock jitter on SNR at an input frequency of 100 MHz, the clock jitter needs to be on the order of 150 fs or better.

Determining the sample clock jitter

As demonstrated earlier, the sample clock jitter consists of the timing uncertainty (phase noise) of the clock as well as the aperture jitter of the ADC. Those two components combine as follows:

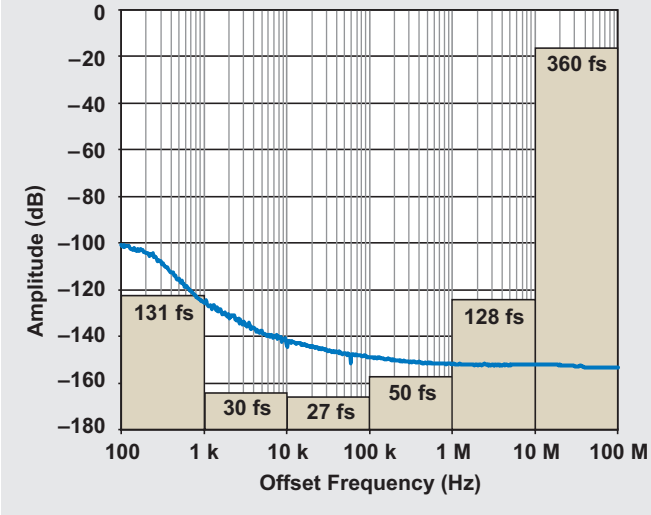
$$t_{Jitter} = \sqrt{(t_{Jitter,Clock\_Input})^2 + (t_{Aperture\_ADC})^2} \quad (3)$$

The aperture jitter of the ADC can be found in the data sheet. It is important to remember that this value is typically specified in combination with either clock amplitude or slew rate. Lower clock amplitudes result in slower slew rates and increase the aperture jitter accordingly.

Jitter from the clock input

The output jitter of devices in the clocking chain (oscillator, clock buffer, or PLL) is typically specified over a frequency range that is offset from the fundamental clock frequency by 10 kHz to 20 MHz—either in picoseconds or as a phase-noise plot, which can be integrated to obtain the jitter information. However, 10 kHz on the low end and 20 MHz on the high end are sometimes not the right boundaries to use, as they are highly dependent upon other system parameters, as will be explained later. The importance of setting the right integration limits is illustrated in Figure 6, where a phase-noise plot is overlaid with its jitter content per decade. It can be seen that the resulting jitter can be quite different if the lower limit is set to a 100-Hz or 10-kHz offset. Likewise, setting the upper integration limit to 10 or 20 MHz yields a drastically different result than setting it to 100 MHz, for example.

Figure 6. Jitter contribution from clock phase noise calculated per decade



Determining the proper lower integration limit

In the sampling process, the input signal gets mixed with the sampling clock's signal, including its phase noise. When an FFT analysis of the input signal is performed, the primary FFT bin is centered over the input signal. The phase noise around the sampled signal (either from the clock or the input signal) determines the amplitude of the bins adjacent to the primary bin, as illustrated in Figure 7. Therefore, all the phase noise with an offset frequency of less than half the bin size gets lumped into the bin of the input signal and doesn't add to the noise. Hence, the lower limit of the phase-noise integration bandwidth should be set to half the FFT bin size. The FFT bin size is calculated as follows:

$$\text{Bin Size} = \frac{\text{Sampling Rate}}{\text{FFT Size}}$$

To further illustrate this point, an experiment using the ADS54RF63 was set up with two different FFT sizes—131,072 and 1,048,576 points. The sampling rate was set to 122.88 MSPS, and the clock phase noise is shown in Figure 8. A 6-MHz, wide-bandpass filter was added to the clock input to limit the amount of wideband noise contributed to the jitter. A 1-GHz input signal was chosen to ensure that the SNR degradation was due solely to clock jitter. Figure 8 shows that the jitter results of the phase-noise integration from half a bin size to 40 MHz are drastically different for the two FFT sizes, and the SNR measurements in Table 1 reflect that as well.

Setting the proper upper integration limit

The phase-noise plot in Figure 6 had a jitter contribution of ~360 fs with the frequency offset between 10 and 100 MHz. This is far more than the entire jitter contribution of ~194 fs with the offset between 100 Hz and 10 MHz. Therefore, the chosen upper integration limit can drastically affect the calculated clock jitter and how well the predicted SNR will match the actual measurement.

To determine the right limit, one has to remember something very important from the sampling process: Noise and spurs on the clock signal alias in-band from other Nyquist zones just like they would if they were present on the input signal (see Reference 1). Hence, if the phase noise of the clock input is not band-limited and doesn't have a rolloff at a higher frequency, then the upper integration limit is set by the bandwidth of the transformer (if used) and the clock input of the ADC itself. In some cases the clock input bandwidth can be very large; for example, the ADS54RF63 has a clock input bandwidth of ~2 GHz to allow higher-order harmonics for very fast clock slew rates.

To verify that the clock phase noise needs to be integrated all the way up to the clock input bandwidth, another experiment was set up. The ADS54RF63 was again operated at 122.88 MSPS with an input signal of 1 GHz to ensure that the SNR jitter was limited. Broadband white noise of 50 MHz to 1 GHz was generated with

Figure 7. Close-in phase noise determines amplitude of FFT bins around primary bin

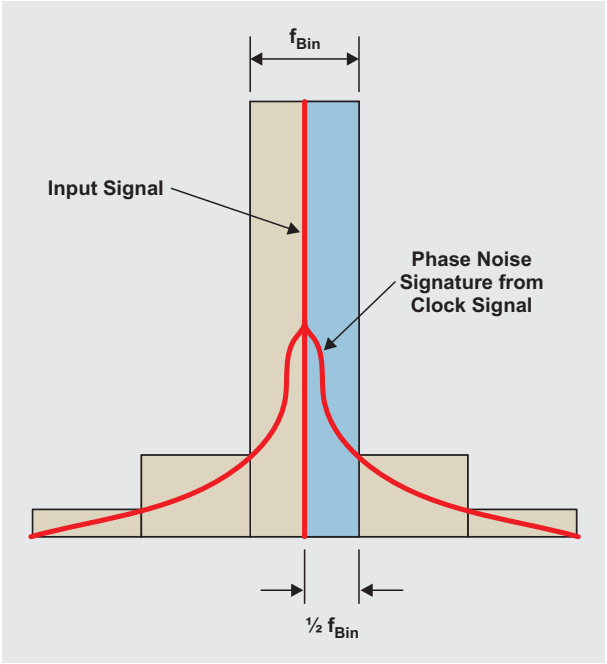


Table 1. SNR measurements for two FFT sizes

FFT SIZE (POINTS)	½ BIN SIZE (Hz)	SNR AT 1 GHz (dBFS)
131,072	469	60.4
1,048,576	59	51.9

Figure 8. Integrated jitter for two FFT sizes with different lower integration limits

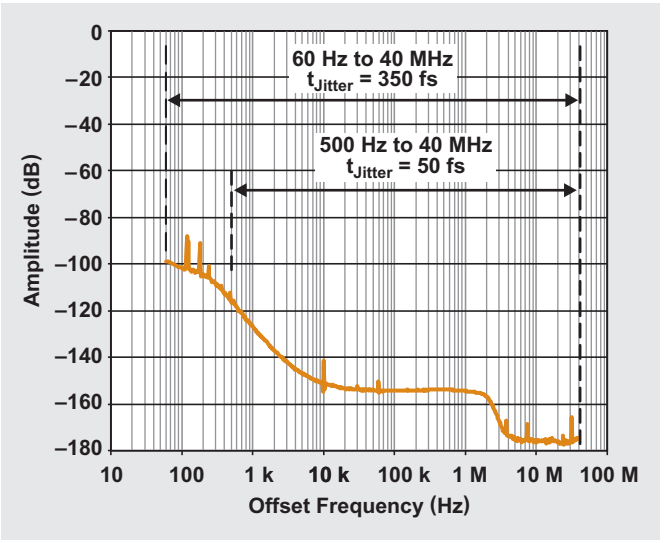
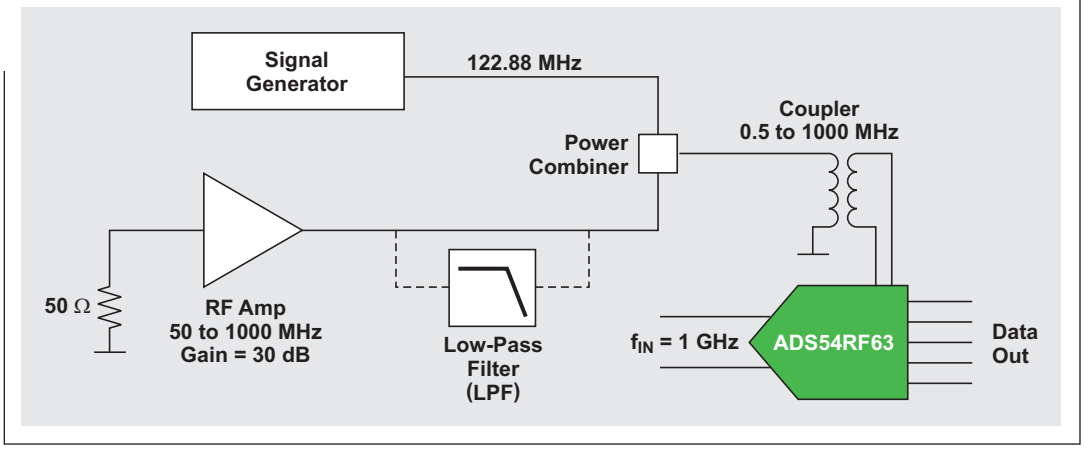


Figure 9. Test setup to verify clock input noise

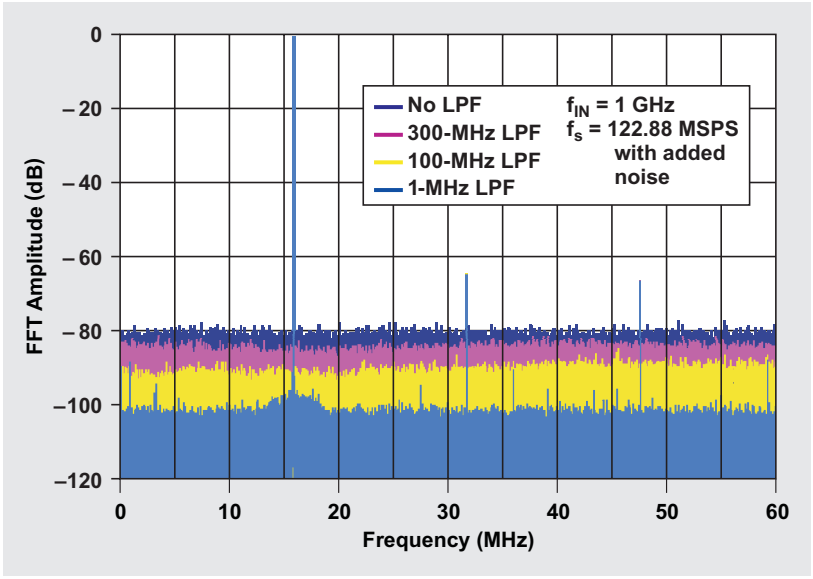


an RF amplifier and added to the sampling clock as shown in Figure 9. Then different low-pass filters (LPFs) were used to limit the amount of noise being added to the clock signal.

The clock input bandwidth of the ADS54RF63 is ~2 GHz, but since the RF amplifier and the transformer both have a 3-dB bandwidth of ~1 GHz, the effective 3-dB clock input bandwidth is reduced to ~500 MHz. The measured SNR results in Table 2 confirm that for this setup the clock input bandwidth indeed is around 500 MHz. A comparison of the FFT plots in Figure 10 further confirms how the wide-band noise from the RF amplifier limits the noise floor and degrades the SNR.

This experiment showed that the phase noise of the clock needs to be either very low or band-limited, ideally through a tight bandpass filter. Otherwise the upper integration limit, set by the clock bandwidth of the system, can degrade the ADC's SNR substantially.

Figure 10. Overlaid measured FFT plots with different noise contributions



Conclusion

This article has shown how to accurately estimate the sampling-clock jitter and determine the proper upper and lower integration boundaries. Part 2 will show how to use this estimation to derive the ADC's SNR and how this result compares against actual measurements.

Table 2. SNR measurements for setup in Figure 9

SETUP	SNR (dBFS)
No filter	39.9
300-MHz LPF	43.6
100-MHz LPF	49.4
1-MHz LPF	57.7

Reference

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1. Thomas Neu, "Impact of sampling-clock spurs on ADC performance," *Analog Applications Journal* (3Q 2009) slyt338

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Coupled inductors broaden DC/DC converter usage

By Jeff Falin
Senior Applications Engineer

Introduction

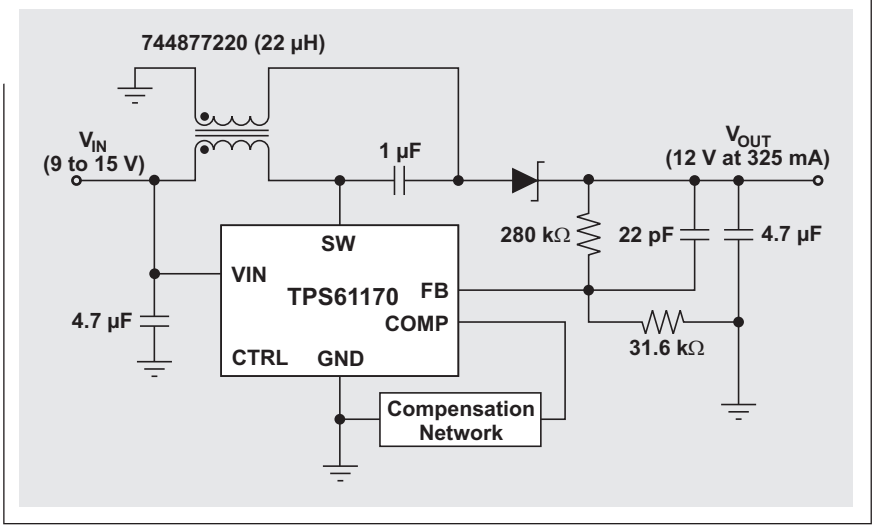
Recently, inductor manufacturers have begun to release off-the-shelf coupled inductors. Consisting of two separate inductors wound on the same core, coupled inductors typically come in a package with the same length and width as that of a single inductor of the same inductance value, only slightly taller. The price of a coupled inductor is also typically much less than the price of two single inductors. The windings of the coupled inductor can be connected in series, in parallel, or as a transformer. This article highlights four DC/DC converter topologies that meet common application needs with coupled inductors.

Clearly understanding the specifications of coupled inductors is essential to using them to their full advantage. Most of these coupled inductors have the same number of turns—i.e., a 1:1 turns ratio—but some newer ones have a higher turns ratio. The coupling coefficient, K, of coupled inductors is typically around 0.95, much lower than a custom transformer's coefficient of greater than 0.99. The mutual inductance of coupled inductors makes them perform somewhat inefficiently in flyback applications and can cause non-ideal (e.g., rounded instead of triangular) inductor waveforms. Also, the current specifications for a coupled inductor are different depending on whether its windings are physically connected in series or in parallel. For example, when the windings are connected in series, the equivalent inductance is more than twice the rated inductance due to the mutual inductance. The saturation and RMS current ratings must be applied to the current flowing simultaneously through both windings, unless otherwise stated in the data sheet. With this understanding of the specifications, some examples of coupled inductors in real applications can now be examined.

More efficient SEPIC with smaller footprint

While not new, the DC/DC single-ended primary inductance converter (SEPIC) topology was not popular until recently, despite the ever-present need for a converter capable of regulating an output voltage that is in-between a higher and lower input voltage (for example, an unregulated wall wart providing 12 V). Any boost converter/controller can be configured as a SEPIC, but this was rarely used until recently. Two factors have contributed to the SEPIC's newfound popularity: (1) IC manufacturers have begun making more boost controllers with current-mode control to simplify compensation, and (2) inductor manufacturers have begun making single-packaged coupled inductors that minimize the converter's overall PCB footprint. Specifically, the power-supply footprint of many applications with two separate inductors can be reduced by a third when a coupled inductor is used instead. Figure 1 shows a SEPIC using the Texas Instruments (TI) TPS61170 and the Wuerth 744877220.

Figure 1. SEPIC using the TI TPS61170 and Wuerth 744877220



Even more appealing, using a SEPIC with a 1:1 coupled inductor forces the inductor ripple current to split between the two windings, allowing the use of half the inductance that two single inductors would require for the same ripple current. Compared to two single inductors at twice the inductance value in a package of the same size, the coupled inductor has lower DC resistance, which helps increase overall converter efficiency. Specifically, with a 15-V input and a 12-V, 325-mA output, the SEPIC in Figure 1 exceeds 91% efficiency. See Reference 1 for more information.

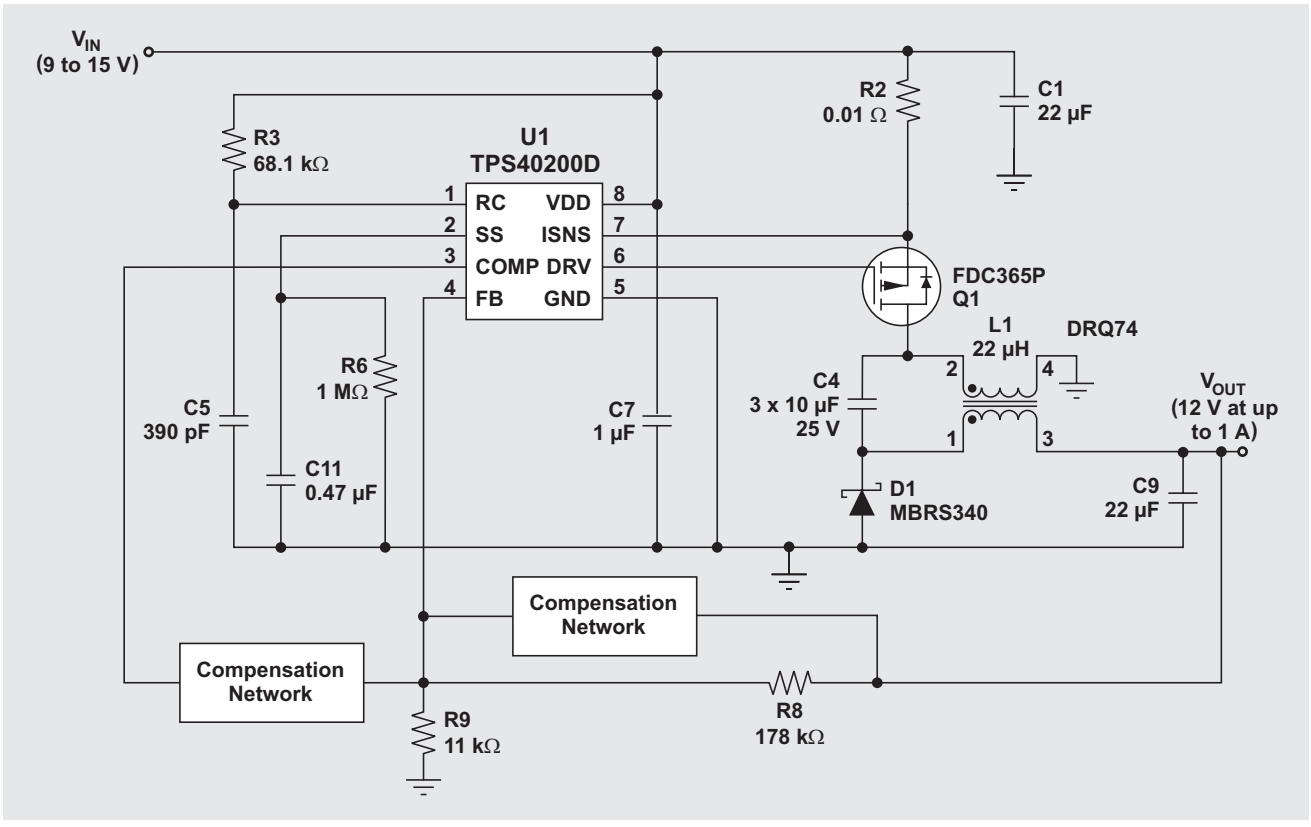
ZETA converter with smaller footprint

A ZETA converter provides the same buck and boost functionality as a SEPIC by using two inductors and a coupling capacitor, but with a buck controller instead of a boost controller. Figure 2 shows the TI TPS40200 and the Coiltronics DRQ74 in a ZETA configuration. Benefiting from the split-inductor ripple current like the SEPIC, this ZETA converter requires half the inductance for the same ripple current. Also like the SEPIC, its overall power-supply footprint is a third smaller than with two separate inductors. Since the output inductor current flows continuously to the output in a ZETA converter, the ZETA converter's output voltage has lower ripple than that of a SEPIC with the same inductance. Therefore, the ZETA may be a better fit for low-noise applications than a SEPIC. See Reference 2 for more information.

Split-rail supply

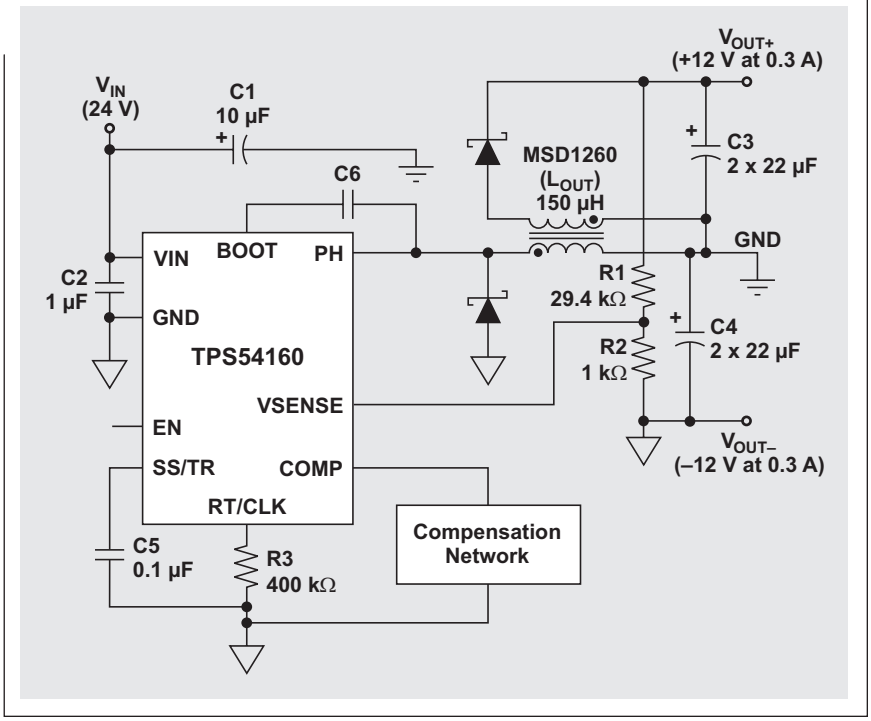
Matching positive and negative power rails are common requirements in industrial applications, especially for amplifiers. A wide-input-range buck converter can be configured to provide a negative output voltage. Replacing the inductor of this inverting buck converter with a coupled inductor and adding a diode and capacitor turns this

Figure 2. ZETA converter with TI TPS40200 and Coiltronics DRQ74



inverting buck converter into one with a dual output. Figure 3 shows the TI TPS54160 and the Coilcraft 150-µH MSD1260 used in this fashion. Even though the difference between each rail is regulated instead of each rail being individually regulated, as long as the loads on each rail are somewhat close together, the coupled inductor assists in providing excellent regulation of each rail. See Reference 3 for more information.

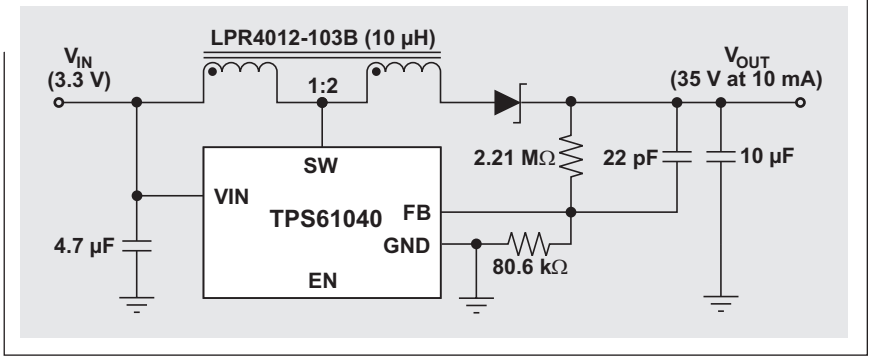
Figure 3. Split-rail buck converter using the TI TPS54160 and Coilcraft MSD1260



Higher output voltage

The output voltage of a DC/DC converter with integrated FETs is limited by the converter's switch current rating. Tying a coupled inductor with a turns ratio greater than 1:1 to the converter's switch (SW) pin can extend the effective output-voltage range of any boost converter. For example, Figure 4 shows the TI TPS61040 boost converter with a 30-V absolute maximum current rating configured to provide 35 V or more, and the Coilcraft LPR4012-103B, which is a 1:2 coupled inductor. When the coupled inductor is configured with the multiple-winding side in series with the diode, the single wound inductor—and therefore the converter's switch FET—has only a third of the output voltage, minus the input voltage, across it.

Figure 4. TI TPS61040 and Coilcraft LPR4012-103B providing extended output voltage



Conclusion

Most inductor manufacturers have a family of coupled inductors with a turns ratio of 1:1 or higher. So, think out of the box! Coupled inductors may expand the application space for a favorite DC/DC converter IC.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title **TI Lit. #**

1. Jeff Falin, "Designing DC/DC converters based on SEPIC topology," *Analog Applications Journal* (4Q 2008) slyt309
2. Jeff Falin, "Designing DC/DC converters based on ZETA topology," *Analog Applications Journal* (2Q 2010) slyt372
3. David G. Daniels, "Creating a split-rail power supply with a wide input voltage buck regulator," Application Report slva369

Related Web sites

power.ti.com

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Replace *partnumber* with TPS40200, TPS54160, TPS61040, or TPS61170

Computing power going "Platinum"

By Michael O'Loughlin
Senior Applications Engineer

Introduction

The 80 PLUS™ and Climate Savers Computing™ initiatives have set a very aggressive efficiency standard for computer power supplies. The "Platinum" level of these standards specifies that computer power supplies must have an efficiency of 90% at 20% of rated load, 94% at 50% load, and 91% at 100% load. To meet these standards, some power-supply designers have chosen to use a phase-shifted, full-bridge DC/DC converter with synchronous rectification. This topology is a good choice because it can achieve zero voltage switching (ZVS) on the primary FETs. A popular way to drive the synchronous rectifiers is with signals that are already present driving the primary FETs. The only problem with doing this is that dead times on these primary FETs are required to achieve ZVS. This results in both synchronous rectifiers being off simultaneously during the freewheeling period, allowing excessive body-diode conduction and reducing system efficiency. The purpose of this article is to propose different timing for driving these synchronous rectifiers to reduce body-diode conduction and improve overall system efficiency.

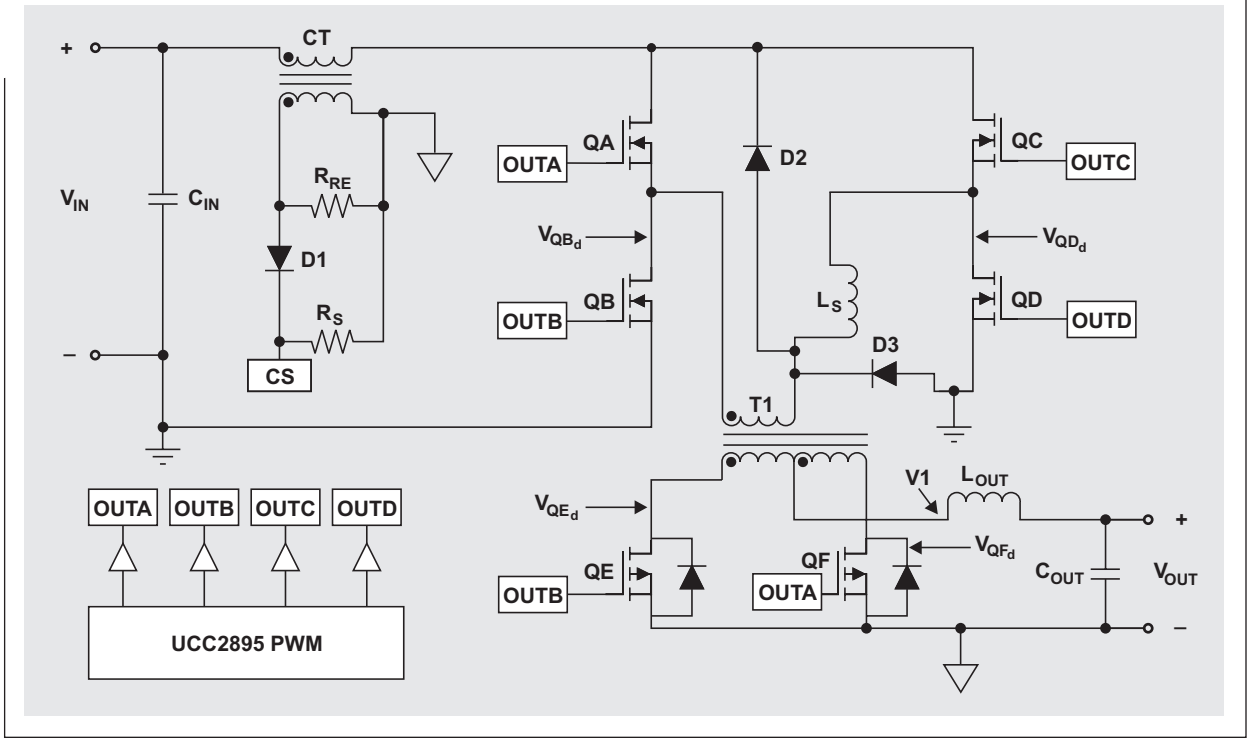
There are a few pulse-width modulators (PWMs) on the market that were developed for controlling a phase-shifted, full-bridge converter but were not set up for driving synchronous rectifiers (QE and QF). To use these controllers in this application, engineers have found they can control the synchronous FETs with control signals OUTA and OUTB from the PWM controller. Figure 1 shows a functional schematic of one of these converters.

The problem

The PWM controllers help achieve ZVS in these converters by delaying the turn-on of the FETs in the H bridge (QA, QB, QC, QD). The delay (t_{Delay}) between the turn-on and turn-off transitions of FETs QA and QB will cause synchronous FETs QE and QF to be off simultaneously, allowing their body diodes to conduct as already stated. The following equation is a good estimate of the body-diode conduction losses in QE and QF during the freewheeling period:

$$P_{Diode} = \frac{P_{OUT}}{V_{OUT}} \times V_D \times t_{Delay} \times f_s,$$

Figure 1. Phase-shifted, full-bridge converter modified for synchronous rectification



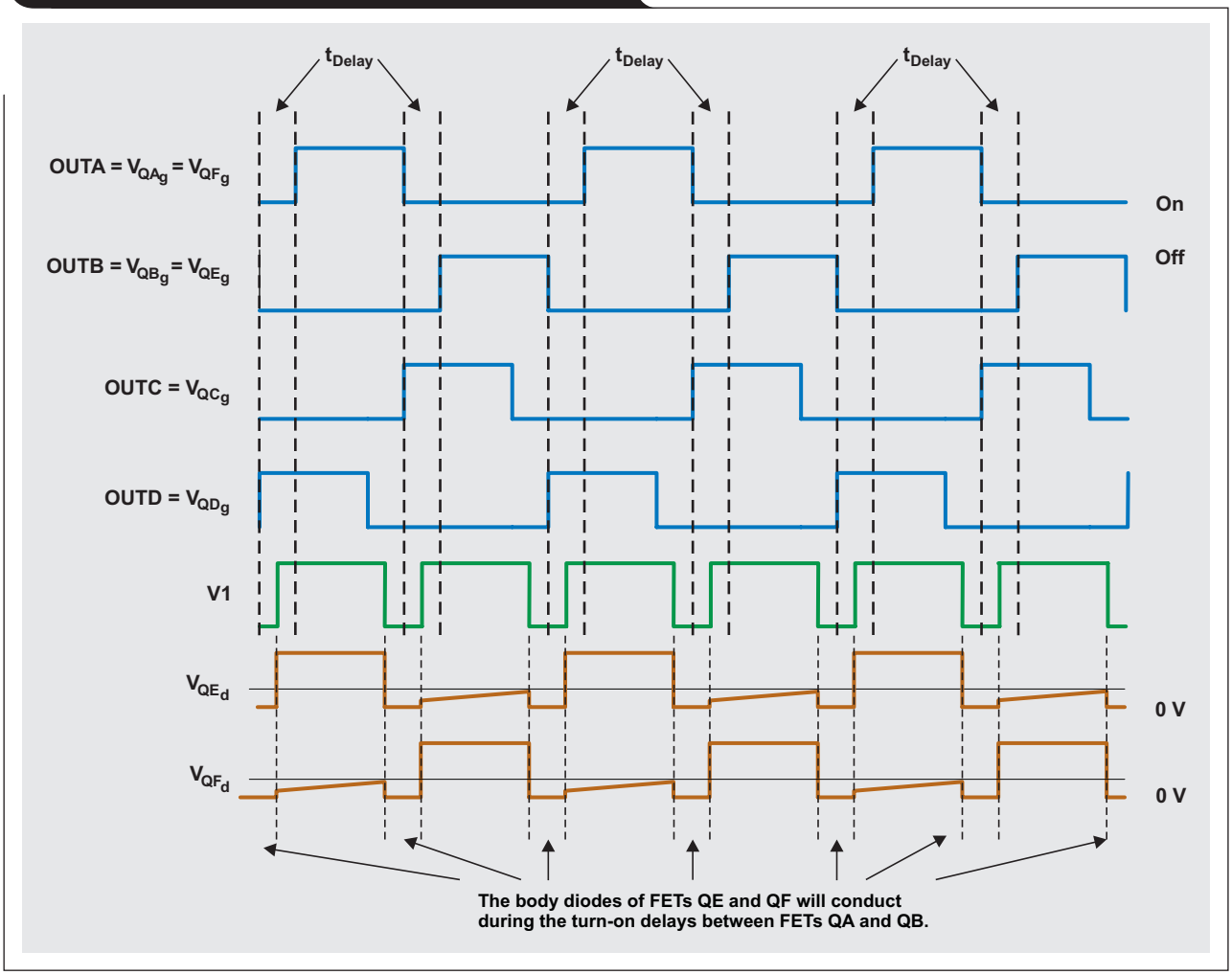
where P_{OUT} is the output power, V_{OUT} is the output voltage, V_D is the forward voltage drop of the body diode, and f_s is the inductor switching frequency.

The excessive body-diode conduction losses of QE and QF (P_{Diode}) could cause the design not to meet the Platinum standard. Please refer to Figures 1 and 2 for details. As shown, OUTA drives FETs QA and QF, while OUTB drives FETs QB and QE. V1 is the voltage presented to the input of the L_{OUT} and C_{OUT} filter network, and V_{QE_d} and V_{QF_d} are the voltages across the respective synchronous rectifiers QE and QF.

The solution

To reduce QE and QF body-diode conduction, it would be better to have these synchronous rectifiers on during the QA and QB delay periods (t_{Delay}). To accomplish this, FETs QE and QF would have to be driven with their own outputs where the ON times would overlap instead of the OFF

Figure 2. Timing diagrams for converter in Figure 1

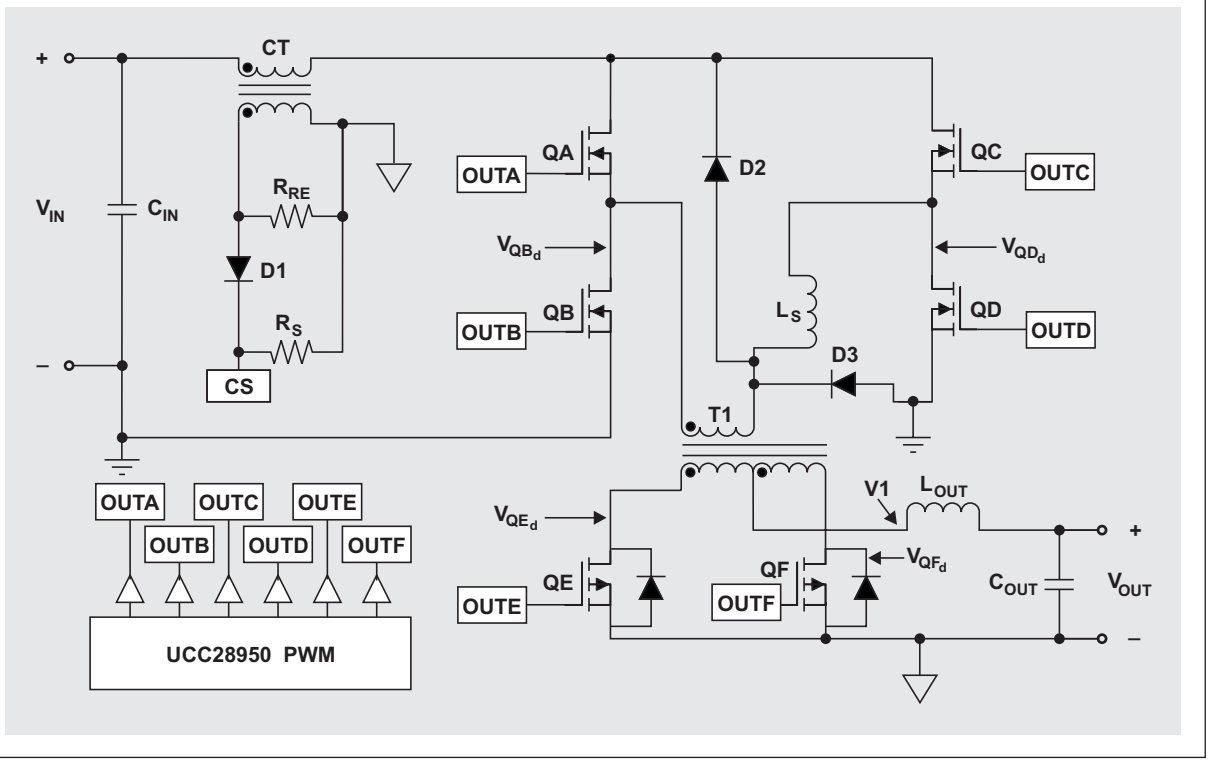


times being simultaneous. Figure 3 shows a functional schematic of the phase-shifted, full-bridge converter with six separate drive signals (OUTA through OUTF). The signals for QE (OUTE) and QF (OUTF) can be generated by turning OUTE and OUTF on and off based on the edges of QA through QD. The timing needed to accomplish this

Table 1. OUTE and OUTF on/off transitions

OUTE	Turns on when OUTC turns on	Turns off when OUTB turns off
OUTF	Turns on when OUTD turns on	Turns off when OUTA turns off

Figure 3. Phase-shifted, full-bridge converter using the timing from Table 1



is presented in Table 1 and Figure 4. The theoretical waveforms in Figure 4 show that this technique removes the body-diode conduction that would be present if both gate drives were off during t_{Delay} with the gate-drive signals presented in Figure 2.

Experimental results

To see how well this technique worked for reducing body-diode conduction, a 390- to 12-V phase-shifted, full-bridge converter was modified to drive the FETs with the signals shown in Figures 2 and 4.

Figure 4. Timing diagram for reducing QE and QF body-diode conduction

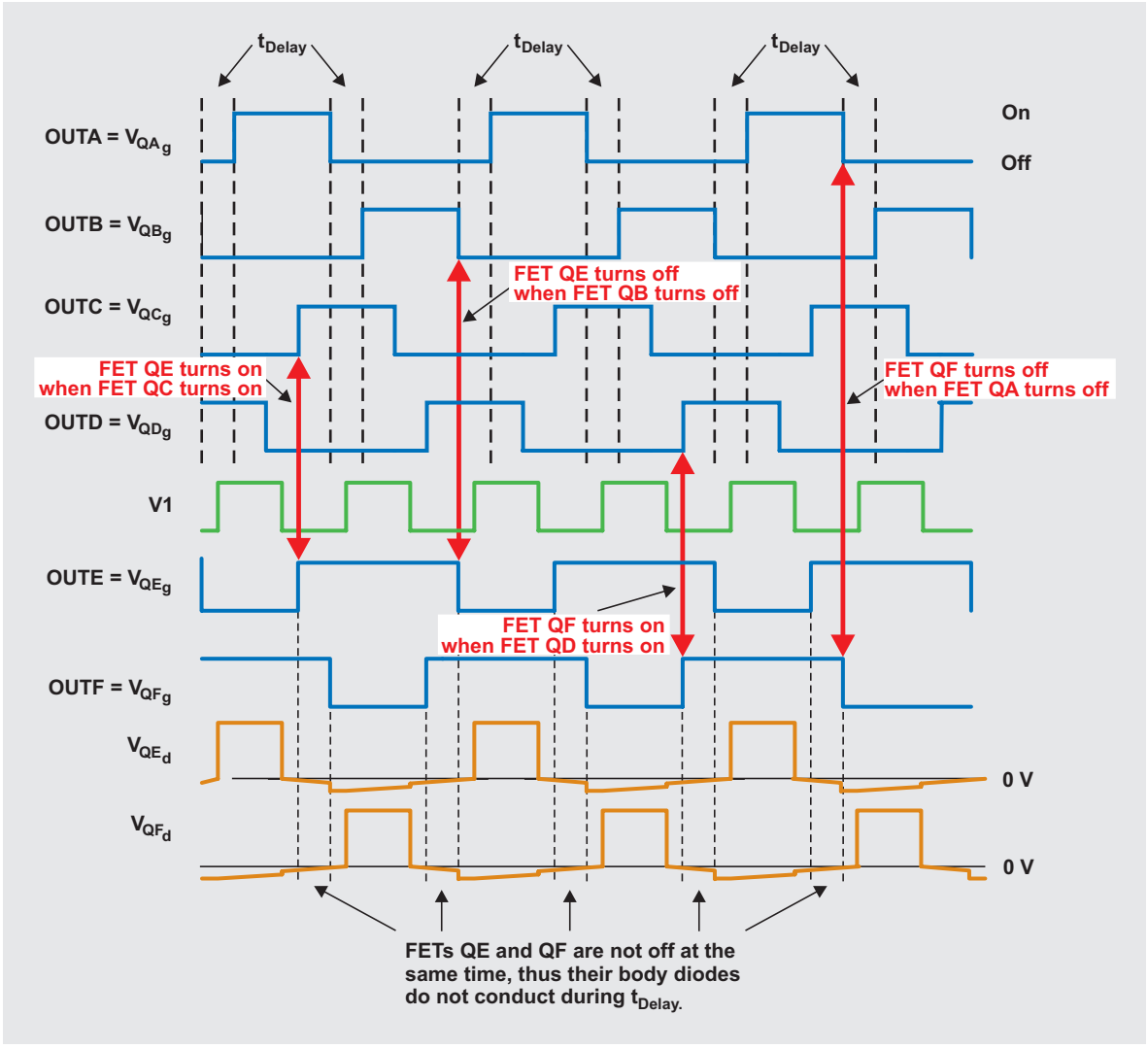


Figure 5 shows a scope plot of the gates of the synchronous FETs (QE and QF) while they were driven with the OUTA and OUTB PWM outputs. In this figure, body conduction can be observed during the delay times (t_{Delay}) between OUTA and OUTB.

Figure 6 on the next page shows a scope plot of the gates of the synchronous FETs (QE and QF) while they were driven with the OUTE and OUTF signals presented in Figure 3. These signals were generated from TI's new UCC28950 phase-shifted, full-bridge controller. Figure 6 shows that the body diodes did not conduct when FETs QE and QF were on at the same time. Some body-diode conduction is still visible, but there is not as much as in Figure 5.

The 600-W DC/DC converter's efficiency was measured for both drive schemes—OUTA and OUTB versus OUTE and OUTF—from 20% to full load. The efficiency data of the converter for these two drive schemes is presented in Figure 7 on the next page. It can be observed that using OUTE and OUTF was roughly 0.4% more efficient at a 50 to 100% load than using OUTA and OUTB. A 0.4% efficiency gain may not seem like a lot but could make a difference when the designer is trying to achieve the Platinum standard.

Conclusion

Even though it is possible to control a phase-shifted, full-bridge converter that has synchronous rectifiers with a phase-shifted, full-bridge controller that was not designed for synchronous rectification (OUTA and OUTB drive scheme), the turn-on delay between OUTA and OUTB required to achieve ZVS causes both synchronous FETs to be off at the same time (t_{Delay}). This delay results in excessive body-diode conduction during the FET's freewheeling period. This article has shown that it is more efficient to overlap the ON time of the synchronous rectifiers during the freewheeling time so that the body diodes do not conduct. Even though the body-diode conduction is not completely removed with this technique, it is drastically reduced, improving overall system efficiency and making the Platinum efficiency standard easier to meet.

Related Web sites

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www.ti.com/sc/device/UCC2895
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Figure 5. Scope plot of QE and QF body-diode conduction

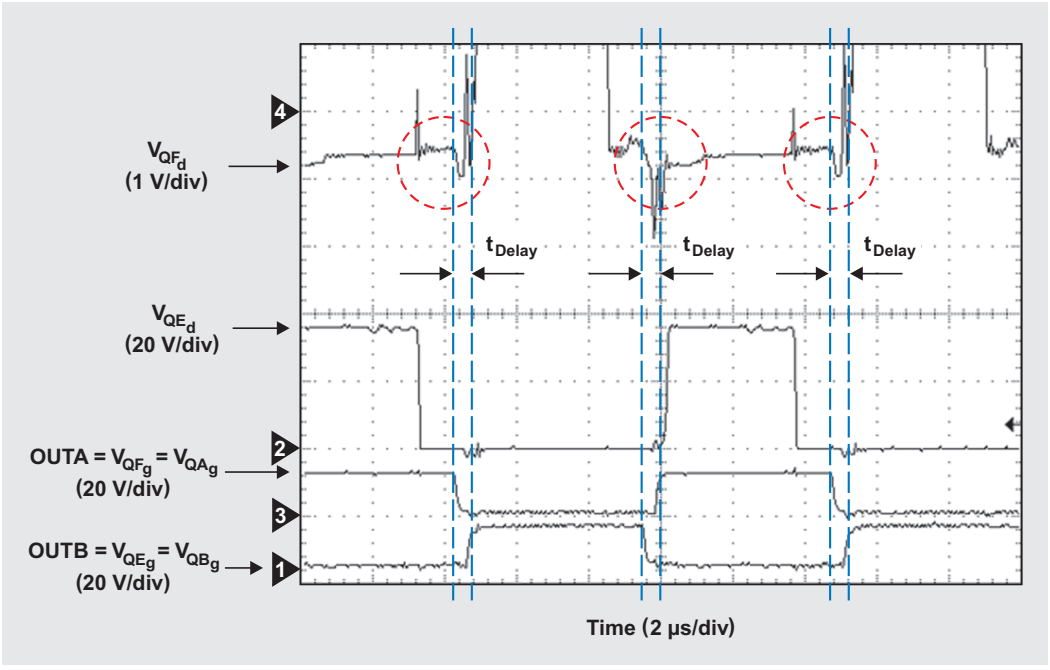


Figure 6. Scope plot showing reduced body-diode conduction of QE and QF

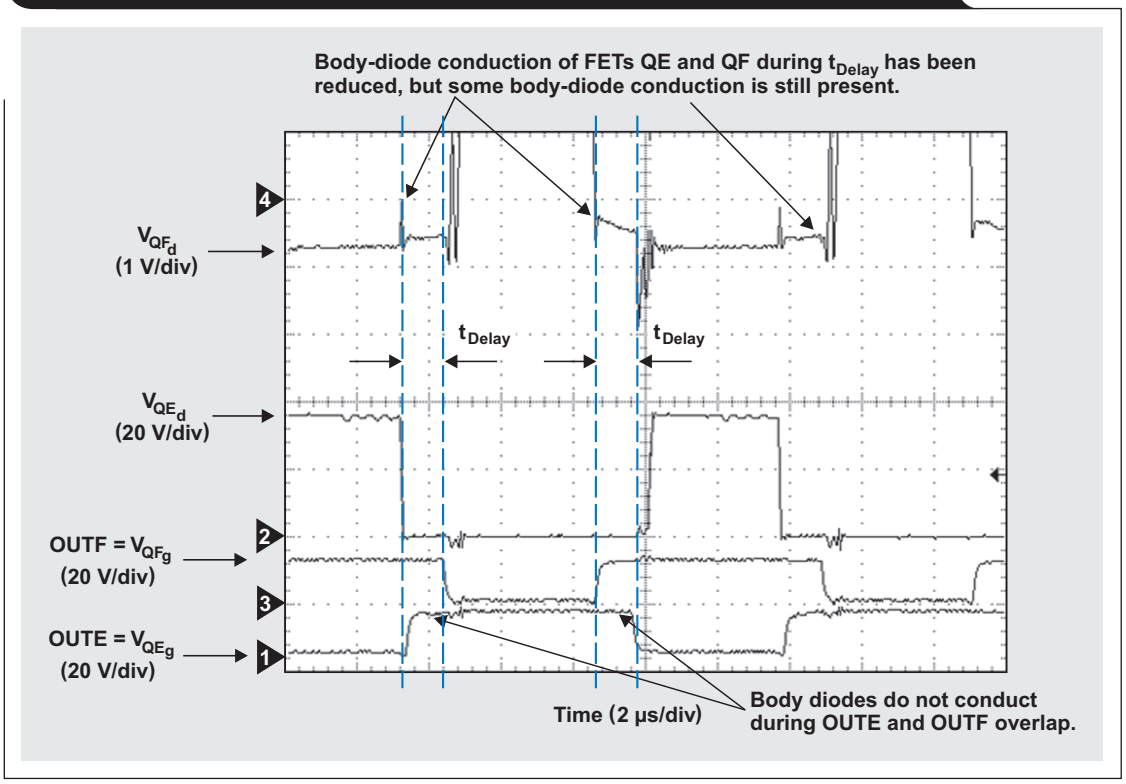
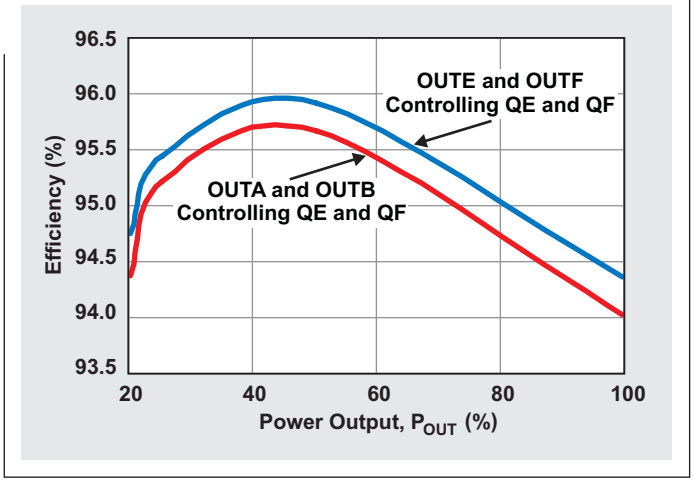


Figure 7. Efficiency of 600-W DC/DC converter with different QE and QF drive schemes



Magnetic-field immunity of digital capacitive isolators

By Thomas Kugelstadt
Senior Applications Engineer

The application environment of digital capacitive isolators often includes close proximity to large electric motors, generators, and other equipment that generates a large electromagnetic field. Exposure to these fields raises concern about the possibility of data corruption, as the electromotoric force (EMF), the voltage created by these fields, can interfere with the transferred data signal. Due to this potential threat, many users of digital isolators demand proof of an isolator's high magnetic-field immunity (MFI). While many digital-isolator technologies come with claims of having high MFI, capacitive isolators provide an almost infinitely high MFI due to their design and internal construction. This article explains the details of this design.

Some physical fundamentals

A current-carrying conductor, such as one of the supply lines to an electric motor, is said to be surrounded by a magnetic field created by the current flowing through it. The direction of the magnetic field is easily determined by applying the right-hand rule (see Figure 1). This rule says that when the conductor is grasped with the right hand and the thumb is pointing in the direction of the current, the fingers encircling the conductor indicate the direction of the magnetic field. Thus, the plane of the magnetic flux lines is always perpendicular to the current.

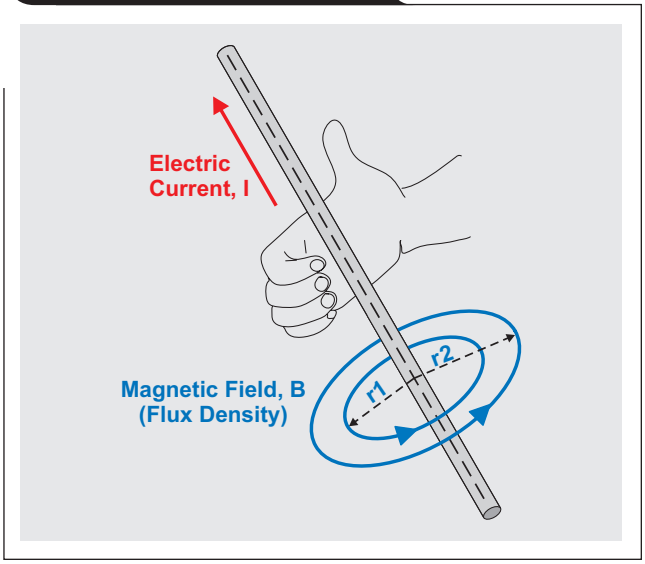
Figure 1 shows the magnetic flux density, B, for a DC current. For an AC current, the right-hand rule is applied in both directions, and the magnetic field changes with the same frequency, f, as the AC current: B(f) ~ I(f). The magnetic field—or, more accurately, the magnetic flux density and its corresponding magnetic-field strength—lessens with increasing distance from the center axis of the conductor. These relations are expressed as

$$B = \frac{\mu_0 I}{2\pi r} \quad (1)$$

and

$$H = \frac{B}{\mu_0} = \frac{I}{2\pi r}, \quad (2)$$

Figure 1. The right-hand rule



where B is the magnetic flux density in volt-seconds per square meter ($V \cdot s/m^2$), μ_0 is the magnetic permeability in free space (given by $4\pi \times 10^{-7}$ $V \cdot s/A \cdot m$), I is the current in amperes, r is the distance from the conductor in meters, and H is the magnetic-field strength in amperes per meter (A/m).

When the magnetic-field lines cross a nearby conductor loop, they generate an EMF whose magnitude depends on the loop area and the flux density and frequency of the magnetic field:

$$EMF(f) = B \times 2\pi f \times A, \quad (3)$$

where EMF is the electromotoric force in volts, f is the field frequency, and A is the loop area in square meters (m^2).

All isolators possess conducting loops in some shape or form for magnetic-field lines to cross and generate EMF. If large enough, this EMF, which is superimposed onto signal voltages, can lead to erroneous data transmission. In fact, some isolation technologies are highly susceptible to magnetic interference. To understand why capacitive isolators are unaffected by magnetic fields, their internal construction needs to be examined.

Figure 2. Simplified diagram of a capacitive isolator's internal construction

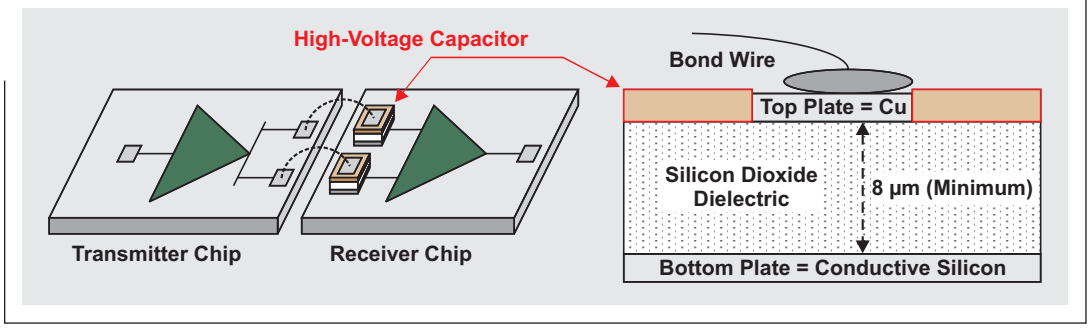
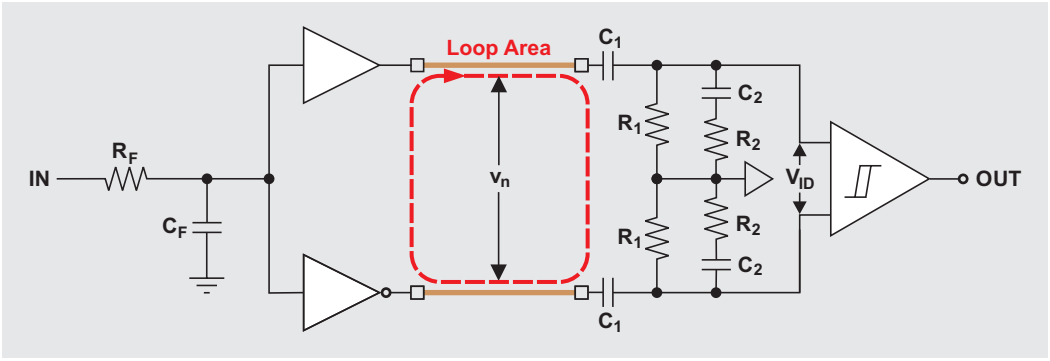


Figure 3. Equivalent-circuit diagram of the isolation barrier

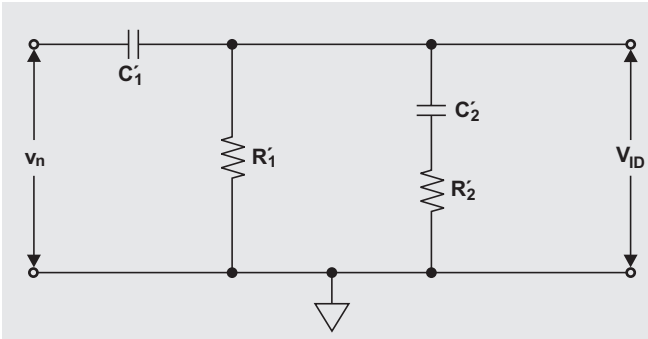


Construction of capacitive isolators

Capacitive isolators consist of two silicon chips—a transmitter and a receiver (Figure 2). Data transfer occurs across a differential isolation barrier formed by two capacitors, each with a copper top plate and a conductive silicon bottom plate on each side of a silicon dioxide (SiO_2) dielectric. The driver outputs of the transmitter chip connect via bond wires to the top plates of the isolation capacitors on the receiver chip. With the bottom plates of the capacitors connecting to the receiver inputs, a conducting loop is created. Figure 3 shows the equivalent-circuit diagram of the isolation barrier and points out the loop area between the gold bond wires. Evidently a magnetic field crossing this loop will generate an EMF that represents input-voltage noise, v_{n1}, to the following RC network. A second differential noise component often encountered, v_{n2}, is due to the conversion of common-mode noise to differential noise. Both noise components make up the combined noise, v_n. If only the effects of EMF are considered, v_n can be conservatively split in half:

$$EMF = \frac{v_n}{2} \quad (4)$$

Figure 4. Single-ended RC network



To trigger the receiver, the output of the RC network must provide a differential input voltage, V_{ID}, that exceeds the receiver input thresholds. Whether or not false triggering occurs depends on the gain response, G(f), of the RC network.

The conversion from a differential to a single-ended network (Figure 4) simplifies the derivation of G(f) but requires that $C_1' = 2C_1$, $R_1' = R_1/2$, $C_2' = 2C_2$, and $R_2' = R_2/2$.

A circuit simulation confirmed that the RC network is a first-order high-pass filter, with C_1' and R_1' being the dominant components up to 100 MHz (see the blue curve in Figure 5). Beyond this frequency, the parasitic components C_2' and R_2' become effective, causing a slight deviation from the linear slope. For up to 100 MHz, therefore, the gain response can be expressed as a ratio of V_{ID}/v_n:

$$\frac{V_{ID}}{v_n}(f) = |G(f)| = \frac{2\pi f}{\sqrt{(2\pi f)^2 + \left(\frac{1}{R_1' \times C_1'}\right)^2}} \quad (5)$$

Determining the maximum noise allowed that does not cause false receiver triggering requires Equation 5 to be solved for v_n:

$$v_n(f) < \frac{V_{ID}\sqrt{(2\pi f)^2 + \left(\frac{1}{R_1' \times C_1'}\right)^2}}{2\pi f} \quad (6)$$

Then, substituting v_n into Equation 4 provides the maximum tolerable EMF in volts:

$$EMF(f) < \frac{V_{ID}\sqrt{(2\pi f)^2 + \left(\frac{1}{R_1' \times C_1'}\right)^2}}{4\pi f} \quad (7)$$

Substituting EMF into Equation 3 then yields the maximum possible magnetic flux density:

$$B(f) < \frac{V_{ID}\sqrt{1 + \left(\frac{1}{2\pi f \times R_1' \times C_1'}\right)^2}}{4\pi f \times A} \quad (8)$$

Table 1. Current and magnetic values for a conductor that is 0.1 m from a capacitive isolator

FREQUENCY, f	MAGNETIC FLUX DENSITY, B (V·s/m²)	EMF (V)	MAGNETIC-FIELD STRENGTH, H (A/m)	CURRENT, I (A)
1 kHz	1.07×10^{7}	63738.5	8.55×10^{12}	5.37×10^{12}
10 kHz	1.07×10^{5}	6373.8	8.55×10^{10}	5.37×10^{10}
100 kHz	1.07×10^{3}	637.4	8.55×10^{8}	5.37×10^{8}
1 MHz	1.07×10	63.7	8.55×10^{6}	5.37×10^{6}
10 MHz	1.07×10^{-1}	6.4	8.55×10^{4}	5.37×10^{4}
100 MHz	1.07×10^{-3}	0.6	8.55×10^{2}	5.37×10^{2}

The frequency-dependent values listed in Table 1 for the magnetic flux density were derived by inserting the following numerical values into Equation 8:

V_{ID} = 10 mV (magnitude of the receiver's input thresholds)

$R_1' \times C_1'$ = 25 ps (effective time constant)

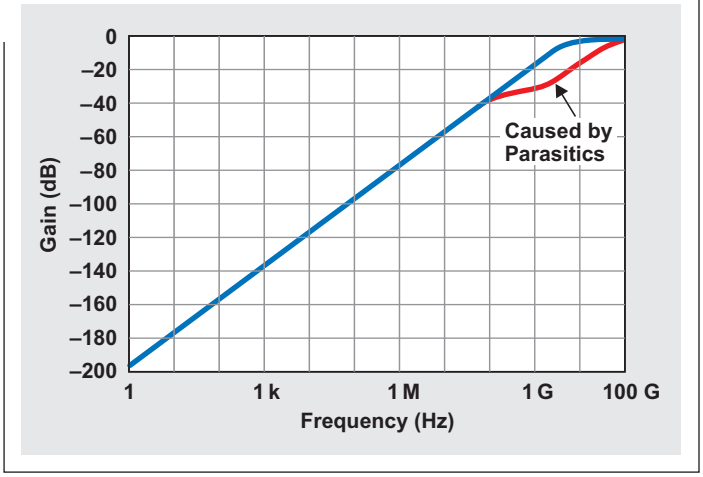
A = 944×10^{-9} m² (effective loop area)

f = 1 kHz to 100 MHz (frequency range of interest)

Using Equations 2 and 3 also provides the EMF, the magnetic-field strength (H), and the corresponding current (I) for a conductor here assumed to be 0.1 m from a prospective isolator.

From the enormously high values in Table 1, it is evident that neither a low-frequency current of 5 trillion amperes nor 500 A at 100 MHz is capable of stopping this isolator

Figure 5. Frequency response of the gain magnitude, |G(f)|

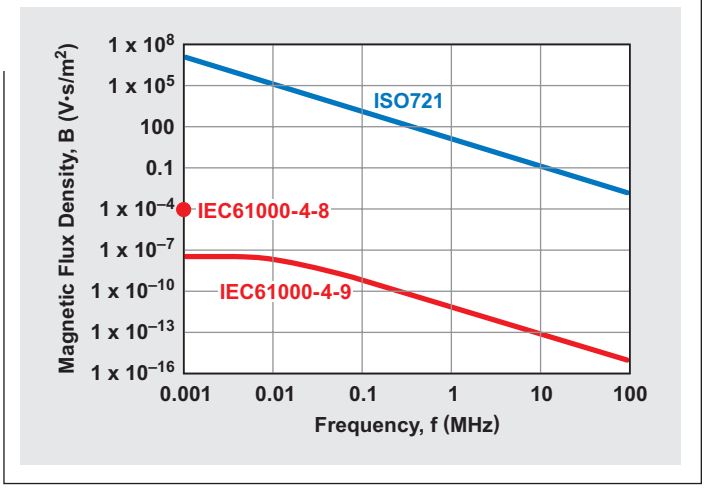


from working correctly. The reason for this almost infinite MFI lies in the location of the isolation capacitors. If these capacitors reside on the transmitter chip, any generated EMF in the bond wires reaches the receiver inputs undisturbed.

Evidently such high MFI values are impossible to test in practice. The data sheets of capacitive isolators therefore show the modest value of only 1000 A/m as the practical test field. However, unshielded capacitive isolators easily pass the Class 5 MFI requirements of the IEC61000-4-8 and IEC61000-4-9 standards. These standards respectively describe the application of power-frequency fields of up to 100 A/m and pulsed fields of up to 1000 A/m. Class 5 defines severe industrial environments with conductors, bus bars, or medium- or high-voltage lines, all of which carry tens of kiloamperes. Also included are the ground conductors of a lightning-protection system and high structures (such as line towers) carrying the whole lightning current. Switchyards of heavy industrial plants and power stations also represent this type of environment.

Figure 6 compares the calculated MFI thresholds of a capacitive isolator with the Class 5 (highest) test levels of IEC 61000-4-8 and IEC 61000-4-9.

Figure 6. MFI test thresholds



Conclusion

Magnetic coupling exceeding the noise budget in the differential circuit of a capacitive isolator requires a magnetic flux density greater than 11.7 V•s/m^2 (117 kilogauss) at 1 MHz. This would be the field generated by over 5 million amperes in a conductor that is 0.1 m away from the device. It is unlikely that this will occur in nature or any manufactured equipment. If it does, the designer can assume that surrounding circuitry will fail before the isolation barrier does.

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Related Web site

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Operational amplifier gain stability, Part 3: AC gain-error analysis

By Miroslav Oljaca, *Senior Applications Engineer,*
and Henry Surtihadi, *Analog Design Engineer*

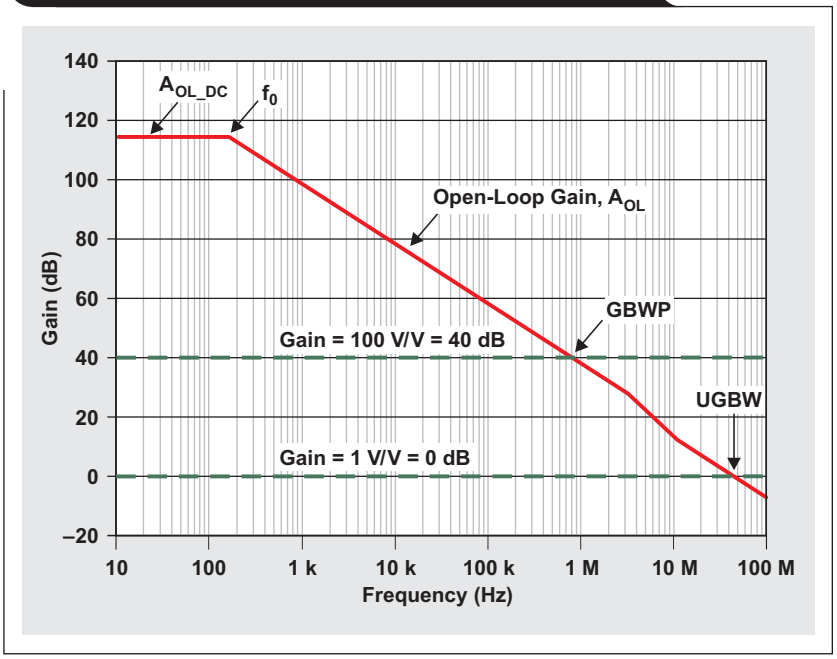
Introduction

The goal of this three-part series of articles is to provide readers with an in-depth understanding of gain accuracy in closed-loop circuits with the most typical operational amplifier (op amp) configurations: non-inverting and inverting. Often, the effects of various op amp parameters on the accuracy of the circuit's closed-loop gain are overlooked and cause an unexpected gain error both in the DC and the AC domains.

In Part 1 (Reference 1), two separate equations were derived for calculating the transfer functions of non-inverting and inverting op amps. Part 2 (Reference 2) showed how to use these two transfer functions and manufacturer data-sheet specifications to analyze the DC gain error of a closed-loop op amp circuit. The same article also discussed how open-loop gain dependency on temperature affects the op amp closed-loop gain error across its specified operating temperature range.

This final article, Part 3, explores the frequency dependency of the closed-loop gain, which will help designers avoid the common mistake of using DC gain calculations for AC-domain analysis.

Figure 1. OPA211 open-loop gain versus frequency



The significance of the gain-bandwidth product

This section will review the concept of the op amp gain-bandwidth product (GBWP), G × BW. The GBWP is a parameter that is needed before the AC closed-loop gain can be calculated. First, GBWP (or GBP, as it is sometimes referred to) is needed to calculate the op amp closed-loop cutoff frequency. GBWP is also needed to calculate the frequency of the dominant pole, f_0, of the op amp open-loop response. At frequencies below f_0, the DC gain-error calculation in Part 2 is valid because the open-loop gain of the op amp is constant; this gain is equal to the A_{OL_DC} (see References 1 and 2). However, beyond a frequency of f_0, the AC calculation must be used, as will be discussed in the following section.

In general, if an op amp has a straight, –20-dB/decade, open-loop-gain rolloff, it has a constant GBWP. For a chosen closed-loop gain, the cutoff frequency at which the closed-loop gain starts to roll off can be calculated by dividing the GBWP by the desired closed-loop gain. Note that in practice the resulting –3-dB point of the closed-loop response may not be exactly equal to the calculated rolloff point due to gain peaking and other non-ideal factors.

Figure 1 shows the simplified open-loop gain versus the frequency response for the Texas Instruments (TI) OPA211. In the product data sheet, the GBWP is specified for two different gains: 1 (GBWP = 45 MHz) and 100 (GBWP = 80 MHz). The reason for the two different gain specifications is that the OPA211's open-loop gain response has an additional pole-zero pair in the frequency region from about 4 to 20 MHz. This is a special case that is contrary to the earlier statement that op amps with straight –20-dB/decade rolloffs will have only one GBWP. For this reason, the GBWP of 80 MHz should be used for calculating the cutoff frequencies for op amps that have a closed-loop gain of 100 or higher, and the GBWP of 45 MHz should be used for op amps with a closed-loop gain of 2 or lower. If a more precise calculation is needed in the frequency region above 4 MHz, using SPICE simulation is suggested.

Using the specified GBWP lets the designer calculate cutoff frequencies for different closed-loop gains. When the op amp is in the unity-gain configuration (where the closed-loop gain is 1), the cutoff frequency is 45 MHz (45 MHz/1), which is also known as the unity-gain bandwidth (UGBW) of the op amp. If the op amp has a closed-loop gain of 100, the cutoff frequency is 800 kHz (80 MHz/100).

To calculate the OPA211's dominant-pole frequency (f_0), the GBWP of 80 MHz will be used. Again, 80 MHz is valid for a closed-loop gain of 100 or higher, up to the value of A_{OL_DC}. A value of 114 dB, which is the minimum ensured DC open-loop gain for the OPA211 at room temperature, will be used for A_{OL_DC}. Substituting all these parameters into Equation 1 yields

$$f_0 = \frac{GBWP}{A_{OL\_DC}} = \frac{80\ MHz}{10^{\frac{114\ dB}{20}}} = 159.62\ Hz. \quad \textbf{(1)}$$

This result will be used in the following section to calculate the AC closed-loop gain.

Calculating the AC closed-loop gain

In Part 1, the closed-loop transfer function of the non-inverting op amp configuration in the frequency domain was calculated. Specifically, the transfer function was derived with the assumption that the op amp had a first-order open-loop response. For calculating gain error, the magnitude response is of interest. For convenience, the result is repeated in the following equation:

$$\left|A_{CL}(f)\right|_{dB} = 20\log\frac{\frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}}}{\sqrt{1+\frac{f^2}{f_0^2}\times\frac{1}{(1+\beta\times A_{OL\_DC})^2}}}, \quad \textbf{(2)}$$

where β is defined as

$$\beta = \frac{V_{FB}}{V_{OUT}} = \frac{R_I}{R_I + R_F}. \quad \textbf{(3)}$$

Also derived in the same article was the equation for calculating the magnitude of the inverting configuration's closed-loop gain. The result is repeated in Equation 4:

$$\left|A_{CL}(f)\right|_{dB} = 20\log\frac{\alpha\frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}}}{\sqrt{1+\frac{f^2}{f_0^2}\times\frac{1}{(1+\beta\times A_{OL\_DC})^2}}} \quad \textbf{(4)}$$

Equation 4 uses the same variable β defined by Equation 3. Additionally, the variable α is defined by Equation 5:

$$\alpha = \frac{V_{FB}}{V_{IN}} = \frac{R_F}{R_I + R_F} \quad \textbf{(5)}$$

At this point, the closed-loop gain for non-inverting and inverting amplifiers is represented by Equations 2 and 4, respectively. These equations calculate the magnitude of the transfer functions and will be used for subsequent analysis.

In Part 2, the DC closed-loop transfer function of the non-inverting op amp configuration was calculated. Again, the transfer function was derived with the assumption that the op amp had a first-order open-loop response. The DC closed-loop gain of the non-inverting and inverting amplifiers can be derived by setting f equal to 0 in Equations 2 and 4, which yields the following two equations:

$$A_{CL\_DC} = \frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}} \quad \textbf{(6)}$$

$$A_{CL\_DC} = -\alpha\frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}} \quad \textbf{(7)}$$

The DC closed-loop gain was derived in slightly different ways in other published articles (References 3 to 8); however, the results agree with this analysis. Unfortunately, in these same articles, the expressions for the AC closed-loop gain were derived by simply replacing A_{OL_DC} with $A_{OL}(f)$ in Equations 6 and 7, which represent the simple transfer functions. The results are shown in Equations 8 and 9:

$$A_{CL}(f) = \frac{A_{OL}(f)}{1+\beta\times A_{OL}(f)} \quad \textbf{(8)}$$

$$A_{CL}(f) = -\alpha\frac{A_{OL}(f)}{1+\beta\times A_{OL}(f)} \quad \textbf{(9)}$$

In these two equations, assuming a first-order system, $A_{OL}(f)$ is defined as

$$A_{OL}(f)\big|_{dB} = A_{OL\_DC}\big|_{dB} - 20\log\sqrt{1+\frac{f^2}{f_0^2}}. \quad \textbf{(10)}$$

However, this is not the correct way to calculate AC closed-loop gain. Instead, Equations 2 and 4, which are the magnitude expressions of the closed-loop transfer function, should be used. Equation 2 should be used instead of Equation 8 for a non-inverting configuration, and Equation 4 should be used instead of Equation 9 for an inverting configuration. The next two sections will show the difference in results when the correct and incorrect equations are used to calculate the gain.

Figure 2. Closed-loop response of OPA211 in non-inverting configuration (G = 200 V/V)

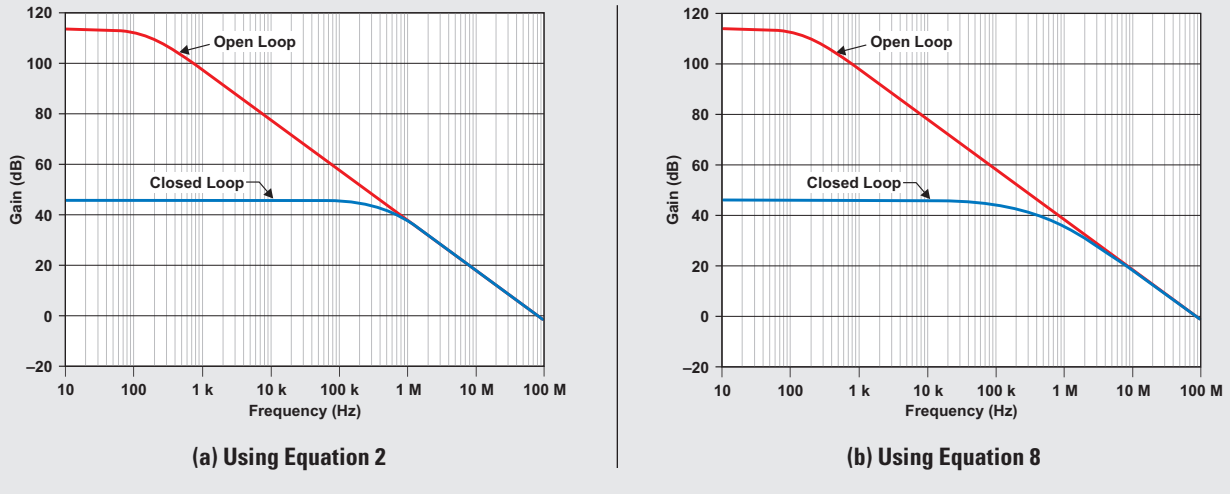


Table 1. Closed-loop gain of OPA211 in non-inverting configuration (G = 200 V/V or 46 dB)

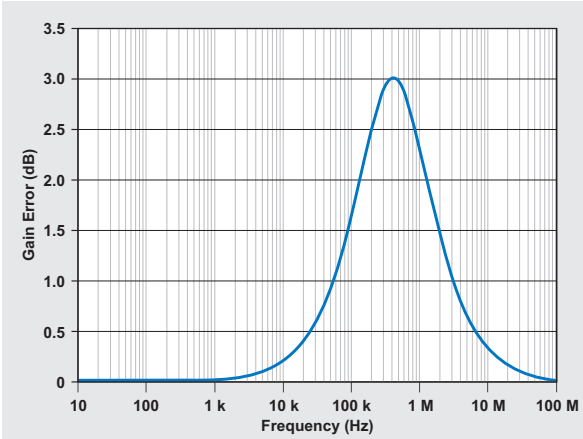
FREQUENCY (kHz)	CLOSED-LOOP GAIN CALCULATED WITH EQUATION 8		CLOSED-LOOP GAIN CALCULATED WITH EQUATION 2		CLOSED-LOOP GAIN ERROR RESULTING FROM EQUATION 8	
	(V/V)	(dB)	(V/V)	(dB)	(%)	(dB)
10	195.121	45.806	199.86	46.014	2.37	0.208
30	186.046	45.392	199.361	45.993	6.679	0.6
60	173.913	44.807	197.71	45.921	12.036	1.114
100	160	44.082	193.956	45.754	17.507	1.672
300	114.286	41.16	159.959	44.08	28.553	2.92
600	80	38.062	110.926	40.901	27.88	2.839
1000	57.143	35.139	74.274	37.417	23.065	2.278

AC gain error for non-inverting configuration

As just stated, there is a tendency for system designers to substitute Equation 10 into Equation 8 to calculate AC gain for a non-inverting configuration. Figure 2 shows the difference in the OPA211's closed-loop response when that method is used versus using Equation 2. In this example, the closed-loop gain is set to 200 V/V (β = 1/200). From Figure 2 it is evident that the difference between using the two equations is primarily in the region of a decade before and after the theoretical intersection between the open-loop and closed-loop curves (that is, the cutoff frequency).

From the previous discussion of the GBWP, it is expected that the OPA211 with a gain of 200 V/V will have a cutoff frequency of 400 kHz (80 MHz/200). Table 1 shows the values in Figure 2 in tabular form for a few selected frequencies. For the frequencies of 10 kHz and 100 kHz, the table shows that there is quite a bit of difference in the frequency responses. The closed-loop gain calculated with Equation 8 drops from about 195 V/V to 160 V/V, compared to a drop of about 199 V/V to 194 V/V with Equation 2. The biggest difference occurs at the cutoff frequency of 400 kHz, where the error is 29%, or 3 dB. These differences, which can be considered as gain error, are plotted in Figure 3.

Figure 3. OPA211 closed-loop gain error resulting from Equation 8



The foregoing analysis shows that a proper understanding of gain error is extremely important in selecting proper components. If a design requires that the flatness of the closed-loop gain be kept within a specified margin, using

Figure 4. Closed-loop response of OPA211 in inverting configuration (G = –200 V/V)

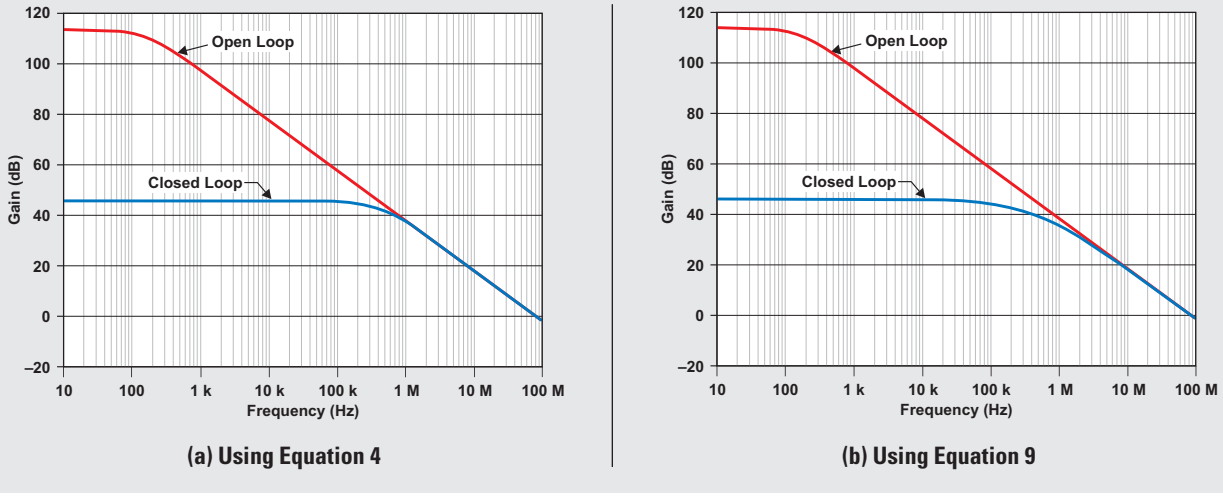


Table 2. Closed-loop gain of OPA211 in inverting configuration (G = –200 V/V or 46 dB)

FREQUENCY (kHz)	CLOSED-LOOP GAIN CALCULATED WITH EQUATION 9		CLOSED-LOOP GAIN CALCULATED WITH EQUATION 4		CLOSED-LOOP GAIN ERROR RESULTING FROM EQUATION 9	
	(V/V)	(dB)	(V/V)	(dB)	(%)	(dB)
10	195.098	45.805	199.857	46.014	2.381	0.209
30	185.981	45.389	199.355	45.993	6.708	0.603
60	173.8	44.801	197.688	45.92	12.084	1.119
100	159.84	44.074	193.898	45.751	17.565	1.678
300	114.041	41.141	159.671	44.065	28.577	2.923
600	79.761	38.036	110.543	40.871	27.847	2.835
1000	56.94	35.108	73.955	37.379	23.008	2.271

Equation 8 will lead the designer to select an op amp with a UGBW 10 times higher than what is needed.

AC gain error for inverting configuration

Similar to the non-inverting configuration, most system designers will use Equations 9 and 10 to calculate the AC gain for an inverting configuration. The difference in the resulting closed-loop gains when Equations 4 and 9 are used is shown in Figure 4. In this example, the op amp is set to an inverting gain of –200 V/V (β = 1/201, α = 200/201). From Figure 4 it can be seen that once again the most significant difference in the results is in the region about a decade before and after the cutoff frequency.

Table 2 shows the values in Figure 4 in tabular form for a few selected frequencies. For the frequencies of 10 kHz and 100 kHz, Table 2 shows the same differences in frequency response as for the non-inverting configuration. The closed-loop gain calculated with Equation 9 drops from about 195 V/V to 160 V/V, compared to a drop of about 199 V/V to 194 V/V with Equation 4. Again, the biggest difference occurs at the cutoff frequency of 400 kHz, where the error is 29%, or 3 dB. These differences, which can be considered as gain error, are plotted in Figure 5 and lead to a conclusion similar to that for the non-inverting configuration: If a design requires that the flatness of the closed-loop gain be kept within a specified margin, using Equation 9 will lead the designer to select an op amp with a UGBW 10 times higher than what is needed.

Figure 5. OPA211 closed-loop gain error resulting from Equation 9

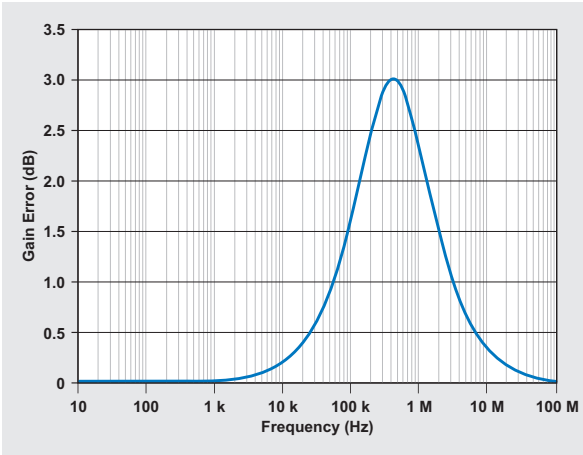


Table 3. Calculated and SPICE-simulation values for AC closed-loop gain

FREQUENCY (kHz)	CLOSED-LOOP GAIN FOR NON-INVERTING CONFIGURATION (V/V)		CLOSED-LOOP GAIN FOR INVERTING CONFIGURATION (V/V)	
	FROM EQUATION 2	FROM SPICE SIMULATION	FROM EQUATION 4	FROM SPICE SIMULATION
10	199.86	199.91	199.86	199.91
30	199.36	199.43	199.36	199.42
60	197.71	197.85	197.69	197.82
100	193.96	194.24	193.89	194.18
300	159.96	161.18	159.67	160.89
600	110.93	112.53	110.54	112.12
1000	74.27	75.5	73.96	75.18

Comparison to SPICE simulation

To verify the validity of Equations 2 and 4 for calculating the AC closed-loop gain in non-inverting and inverting configurations, the results were compared to those of a TINA-TI™ SPICE simulation. For this analysis, the OPA211 macromodel was used. This simulation model can be downloaded at:

http://focus.ti.com/docs/prod/folders/print/opa211.html#toolssoftware

Table 3 shows that the calculated results from Equations 2 and 4 closely match the results from the SPICE simulation, confirming that Equations 2 and 4 are indeed the correct equations to use to calculate the AC closed-loop gain. The slight discrepancies between the calculated and simulated results can be attributed to the fact that the SPICE simulation included non-ideal op amp factors (such as input bias currents, etc.) that were ignored in this simplified analysis.

Conclusion

Part 1 of this article series explored general feedback-control-system analysis and synthesis as they apply to first-order transfer functions. The analysis technique was applied to both non-inverting and inverting op amp circuits, resulting in a frequency-domain transfer function for each configuration.

Part 2 showed how to use these two transfer functions and manufacturer data-sheet specifications to analyze the DC gain error of a closed-loop op amp circuit. This analysis also took into consideration the temperature dependency of the open-loop gain as well as its finite value.

Part 3 of this article series has explored how to calculate the closed-loop gain error for AC input signals. Instead of using the magnitude equations, system designers have a tendency to use the simple transfer-function equations. As has been shown, using these equations will lead to incorrect results, specifically in the vicinity of the circuit's cut-off frequency, where the error will be more significant. By using the magnitude equations to calculate the closed-loop gain, system designers should be able to choose a more appropriate op amp that will meet the design requirements.

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