# How delta-sigma ADCs work, Part 1

**By Bonnie Baker**
*Signal Integrity Engineer*

Analog techniques have dominated signal processing for years, but digital techniques are slowly encroaching into this domain. The design of delta-sigma (ΔΣ) analog-to-digital converters (ADCs) is approximately three-quarters digital and one-quarter analog. ΔΣ ADCs are now ideal for converting analog signals over a wide range of frequencies, from DC to several megahertz. Basically, these converters consist of an oversampling modulator followed by a digital/decimation filter that together produce a high-resolution data-stream output. This two-part article will look closely at the ΔΣ ADC's core. Part 1 will explore the basic topology and function of the ΔΣ modulator, and Part 2 will explore the basic topology and function of the digital/decimation filter module.

## ΔΣ converters: An overview

The rudimentary ΔΣ converter is a 1-bit sampling system. An analog signal applied to the input of the converter needs to be relatively slow so the converter can sample it multiple times, a technique known as oversampling. The sampling rate is hundreds of times faster than the digital results at the output ports. Each individual sample is accumulated over time and "averaged" with the other input-signal samples through the digital/decimation filter.

The ΔΣ converter's primary internal cells are the ΔΣ modulator and the digital/decimation filter. The internal ΔΣ modulator shown in Figure 1 coarsely samples the input signal at a very high rate into a 1-bit stream. The digital/decimation filter then takes this sampled data and converts it into a high-resolution, slower digital code. While most converters have one sample rate, the ΔΣ converter has two—the input sampling rate ($f_S$) and the output data rate ($f_D$).

## The ΔΣ modulator

The ΔΣ modulator is the heart of the ΔΣ ADC. It is responsible for digitizing the analog input signal and reducing noise at lower frequencies. In this stage, the architecture implements a function called noise shaping that pushes low-frequency noise up to higher frequencies where it is outside the band of interest. Noise shaping is one of the reasons that ΔΣ converters are well-suited for low-frequency, high-accuracy measurements.

The input signal to the ΔΣ modulator is a time-varying analog voltage. With the earlier ΔΣ ADCs, this input-voltage signal was primarily for audio applications where AC signals were important. Now that attention has turned to precision applications, conversion rates include DC signals. This discussion will use a single cycle of a sine wave for illustration.

**Figure 1. Block diagram of ΔΣ ADC**

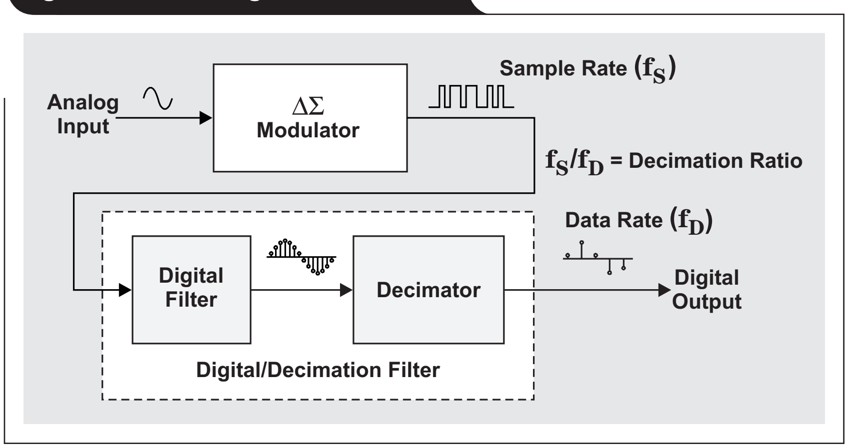


Figure 2. Input signal to the ΔΣ modulator

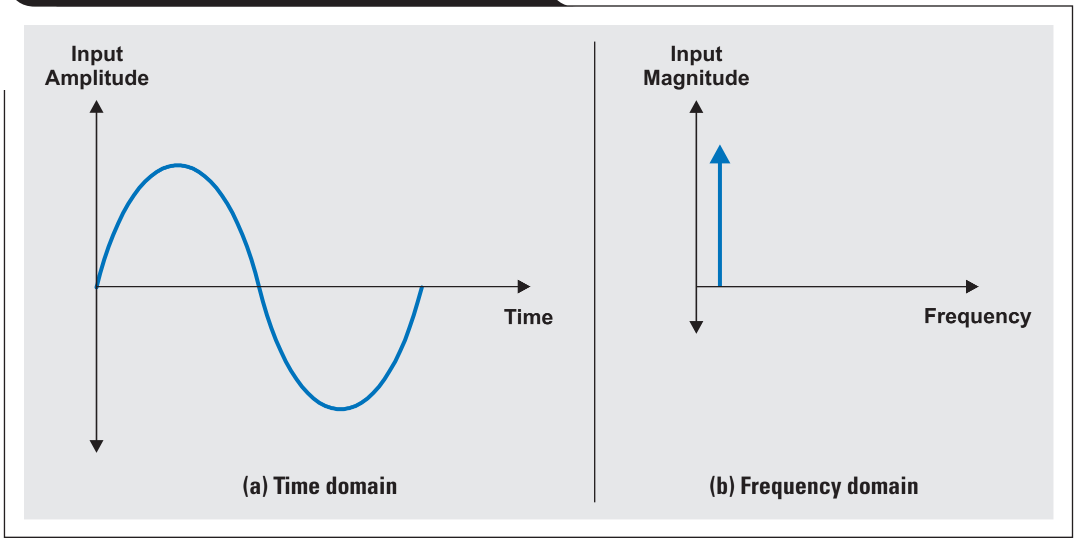



Figure 2a shows a single cycle of a sine wave for the input of a ΔΣ modulator. This single cycle has voltage amplitude that changes with time. Figure 2b shows a frequency-domain representation of the time-domain signal in Figure 2a. The curve in Figure 2b represents the continuous sine wave in Figure 2a and appears as a straight line or a spur.

There are two ways to look at the ΔΣ modulator—in the time domain (Figure 3) or in the frequency domain (Figure 4). The time-domain block diagram in Figure 3 shows the mechanics of a first-order ΔΣ modulator. The modulator converts the analog input signal to a high-speed, single-bit, modulated pulse wave. More importantly, the frequency analysis in Figure 4 shows how the modulator affects the noise in the system and facilitates the production of a higher-resolution result.

The ΔΣ modulator shown in Figure 3 acquires many samples of the input signal to produce a stream of 1-bit codes. The system clock implements the sampling speed, $\mathbf{f_S}$, in conjunction with the modulator's 1-bit comparator. In this manner, the quantizing action of the ΔΣ modulator is produced at a high sample rate that is equal to that of the system clock. Like all quantizers, the ΔΣ modulator produces a stream of digital values that represent the voltage of the input, in this case a 1-bit stream. As a result, the ratio of the number of ones to zeros represents the input analog voltage. Unlike most quantizers, the ΔΣ modulator includes an integrator, which has the effect of shaping the quantization noise to higher frequencies. Consequently, the noise spectrum at the output of the modulator is not flat.

In the time domain, the analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage at $\mathbf{x_2}$. This voltage is presented to the integrator, whose output progresses in a negative or positive direction. The slope and direction of the signal at $\mathbf{x_3}$ is dependent on the sign and magnitude of the voltage at $\mathbf{x_2}$. At the time the voltage at $\mathbf{x_3}$ equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative,

Figure 3. First-order ΔΣ modulator in the time domain

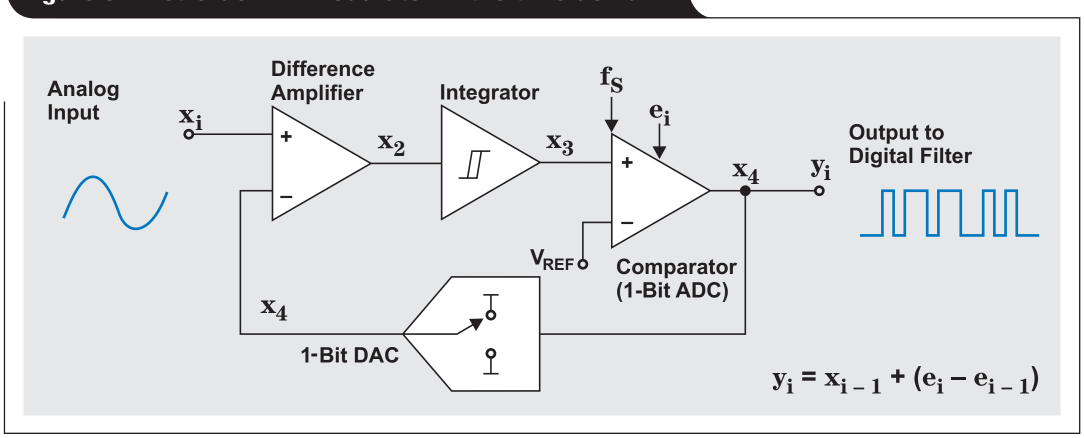
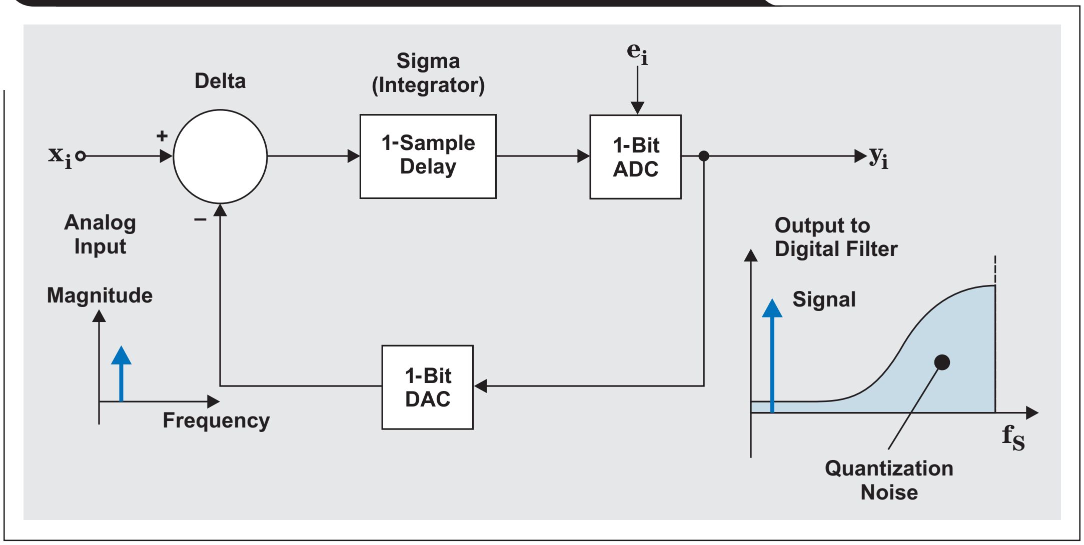


**Figure 4. First-order ΔΣ modulator in the frequency domain**




depending on its original state. The output value of the comparator, $\mathbf{x_4}$, is clocked back into the 1-bit DAC, as well as clocked out to the digital filter stage, $\mathbf{y_i}$. At the time that the output of the comparator switches from high to low or vice versa, the 1-bit DAC responds by changing the analog output voltage of the difference amplifier. This creates a different output voltage at $\mathbf{x_2}$, causing the integrator to progress in the opposite direction. This time-domain output signal is a pulse-wave representation of the input signal at the sampling rate ($\mathbf{f_S}$). If the output pulse train is averaged, it equals the value of the input signal.

The discrete-time block diagram in Figure 3 also shows the time-domain transfer function. In the time domain, the 1-bit ADC digitizes the signal to a coarse, 1-bit output code that produces the quantization noise of the converter. The output of the modulator is equal to the input plus the quantization noise, $\mathbf{e_i - e_{i-1}}$. As this formula shows, the quantization noise is the difference between the current quantization error ($\mathbf{e_i}$) and the previous quantization error ($\mathbf{e_{i-1}}$). Figure 4 illustrates the frequency location of this quantization noise.

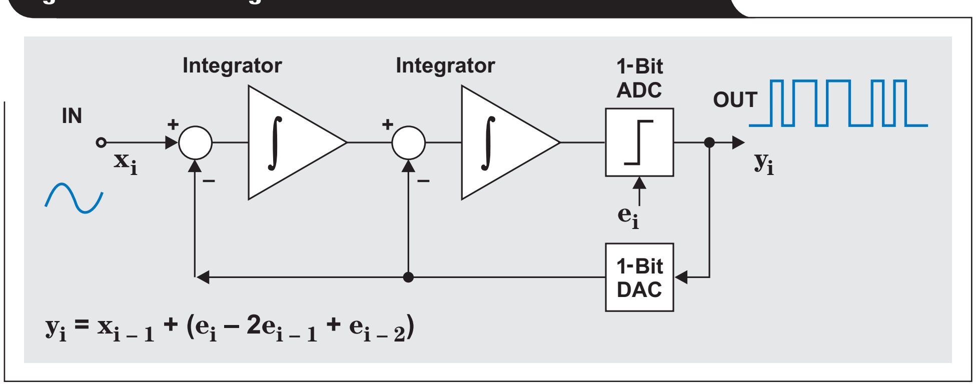
Figure 4 also shows that the combination of the integrator and sampling strategy implements a noise-shaping filter on the digital output code. In the frequency domain, the time-domain output pulses appear as the input signal (or spur) and shaped noise. The noise characteristics in Figure 4 are the key to understanding the modulator's frequency operation and the ability of the ΔΣ ADC to achieve such high resolution.

The noise in the modulator is moved out to higher frequencies. Figure 4 shows that the quantization noise for a first-order modulator starts low at zero hertz, rises rapidly, and then levels off at a maximum value at the modulator's sampling frequency ($\mathbf{f_S}$).

Using a circuit that integrates twice instead of just once is a great way to lower the modulator's in-band quantization noise. Figure 5 shows a 1-bit, second-order modulator that has two integrators instead of one. With this second-order modulator example, the noise term depends on not just the previous error but the previous two errors.

Some of the disadvantages of the second- or multi-order modulators include increased complexity, multiple loops,

**Figure 5. Block diagram of a second-order ΔΣ modulator**



and increased design difficulty. However, most ΔΣ modulators are higher-order, like the one in Figure 5. For instance, Texas Instruments ΔΣ converters include second- through sixth-order modulators.

Multi-order modulators shape the quantization noise to even higher frequencies than do the lower-order modulators. In Figure 6, the highest line at the frequency $\mathbf{f_S}$ shows the third-order modulator's noise response. Note that this modulator's output is very noisy all the way out at its sampling frequency of $\mathbf{f_S}$. However, down at lower frequencies, below $\mathbf{f_D}$ and near the input-signal spur, the third-order modulator is very quiet. $\mathbf{f_D}$ is the conversion frequency of the digital/decimation filter. Selecting a value for $\mathbf{f_D}$ will be discussed in Part 2 of this article series.

## Modulators: The first half of the story

The modulator of the ΔΣ ADC successfully reduces low-frequency noise during the conversion process. However, the high-frequency noise is a problem and is undesirable in the final output of the converter. Part 2 of this article series will discuss how to get rid of this noise with a low-pass digital/decimation filter.

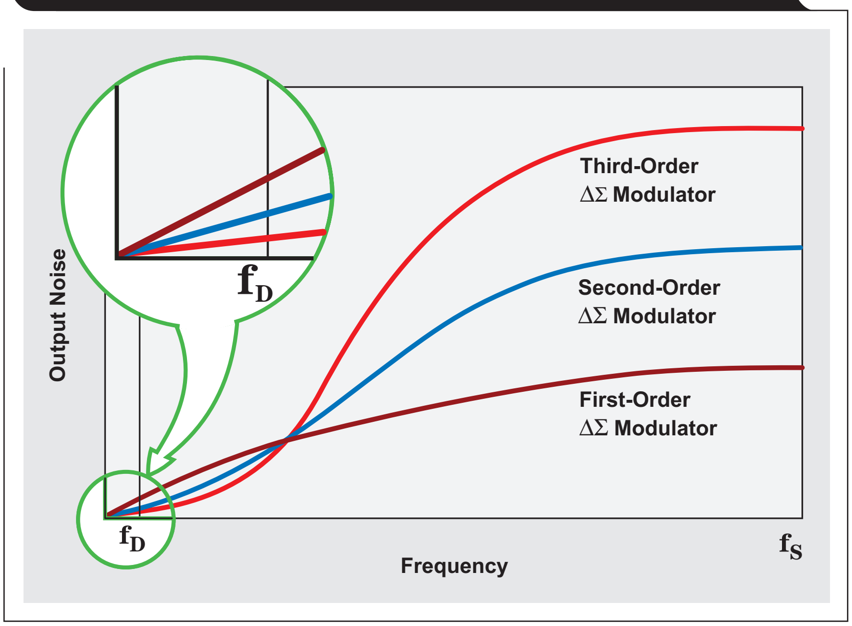
## References


1. R. Jacob Baker, *CMOS: Mixed-Signal Circuit Design*, Vol. II. John Wiley & Sons, 2002.
2. Texas Instruments, *Nuts and Bolts of the Delta-Sigma Video Tutorial* [Online]. Available: http://focus.ti.com/docs/training/catalog/events/event.jhtml?sku=WEB408001


## Related Web site

**dataconverter.ti.com**

**Figure 6. ΔΣ modulator noise shaping versus modulator order with a sampling frequency of $f_S$**



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SLYT423A
Revised September 2016