Advantages of PMIC converters with enhanced hysteretic-mode control for wearable and IoT devices

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Recent advances in wearable products and the Internet of Things (IoT) have increased the need for integrated power management ICs (PMICs) that provide high efficiency and low I_Q in a smaller footprint. When operating from coin cells or Li-ion batteries, PMIC solutions that meet these specifications now include switch-mode DC/DC converters with hysteretic mode control.

Typical wearable products spend the majority of their time in a sleep mode or low-power state. They only wake up for user-generated or timed events that result in CPU data processing and/or information transfer via radio link or wired link. For example, a wearable slave device with *Bluetooth*® technology that monitors heart rate may be connected for less than a one hour per day and consume only 10 to 20 µA in sleep mode. The peak consumption of 25 to 50 mA during a connection may last less than three milliseconds. This means that power-supply performance must be optimized when the device is asleep or active. Space constraints and battery chemistries also impose restrictions on the external passives.

The role of DC/DC converters in a PMIC

Figures 1, 2, and **3** show block diagrams of a generic wearable device, a connected programmable thermostat, and a smart payment terminal. While parametric specifications differ by application, an integrated PMIC with efficient DC/DC converters could be used to power one or more of the loads – a 32-bit processor core, memory (Flash, DDR), I/O bus, display, and peripherals such as motors and sensors.

When a processor changes between sleep and active states, the profiles for step-load current require fast start-up times and fast transient responses. Compliance with RF interference standards also requires switching noise to lie outside specific bands, such as FM transmission.

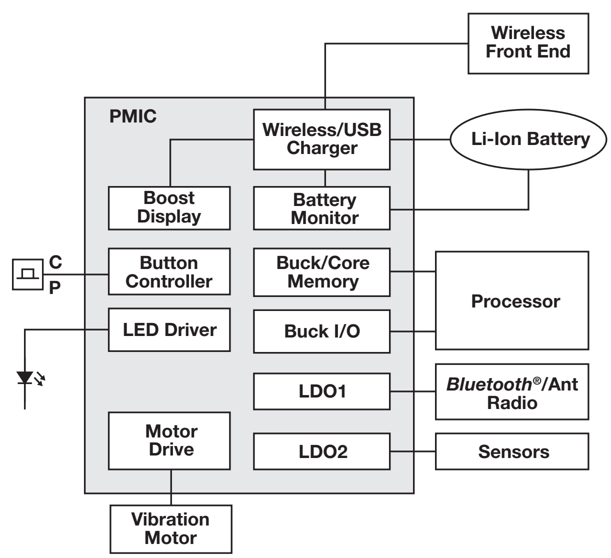

***Figure1**: Wearable device.*

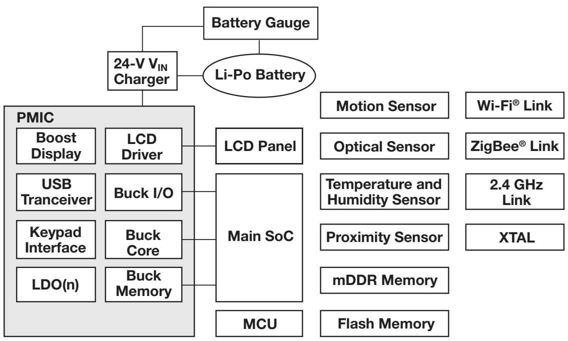

Figure 2: *Connected programmable thermostat.*

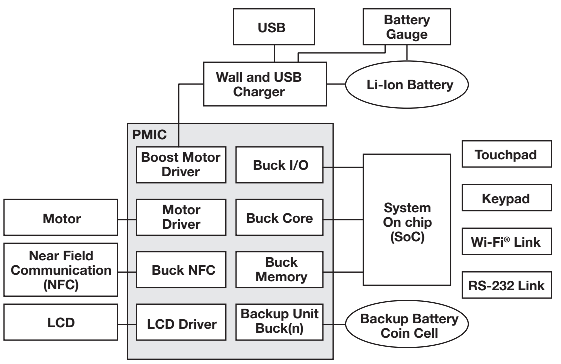

Figure 3: *Smart payment terminal.*

Limitations of classic hysteretic control

The design goal for single-phase, hysteretic PWM switch-mode converters employed in PMICs is to meet load requirements that range from very low (<30 mA) to very high (up to 3 A). A block diagram of the classic switching converter is shown in **Figure 4.** The control method of this converter can have fast transient response because the loop delay is primarily governed by the comparator and the delay of the driver circuit. The control circuit consists of a comparator with hysteresis, and ideally, an error amplifier and clock generator are not required [Reference 1]. The basic converter requires no phase compensation because the feedback signal is a close replica of the inductor current. The switching frequency equation presented in Reference 1 is

$$f_S = \frac{D(1-D)}{\tau_{RC}\left(\frac{V_H}{V_{IN}}\right) + \tau_D}$$

where V_{IN} is the input voltage to the converter, V_H is the hysteresis of the comparator, D is the PWM-signal duty cycle set by desired output voltage (V_{OUT}), $\tau_{RC} = R_F C_F$ is the time constant of the feedback network, and τ_D is the finite converter propagation delay, which includes delay from the driver stage and output bridge. These variables are shown in Figure 4 (Figure 1 in Reference 2). Clearly, f_S is not constant versus D, and this could cause spurs in unwanted spectral regions or cause resonance-induced voltage excursions in the power supply network. This scenario has been a key concern with classic hysteretic control in the past.

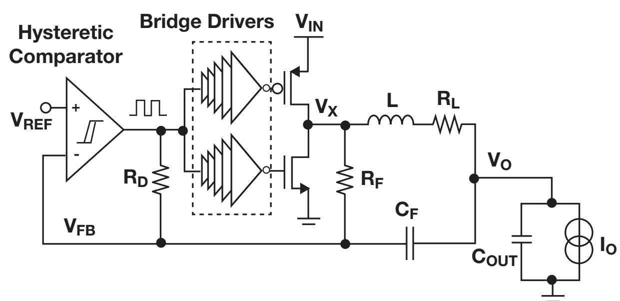

Figure 4: *Classic hysteretic-control buck converter.*

PMICs with enhanced DC/DC converters

Texas Instruments offers several PMICs with enhancements to overcome some limitations of classic hysteretic control. Devices such as the TPS65910, TPS65911, TPS65912, TPS80032 and TPS65218, contain several single-phase converters that provide tighter control over switching frequency. They also provide a simpler choice of L and C that will simplify system integration. **Table 1** lists a few key features and benefits of the PMIC devices.

PMIC Device Features	Benefits
A single PMIC can power multiple core domains, I/O, memories, and pre-regulation of other supply rails like LDOs	Reduce board space due to multiple discrete supply rails
Load currents up to 3 A with integrated FETs	Reduce BOM
Advanced modes of dynamic voltage scaling (DVS) for various processor low-power configurations	Enable sleep-state power control
Low I_Q of 20 to 30 µA	Enable "always ON" functionality
Peak efficiencies as high as 90%	Maximize battery life
Light-load (10 to 100 mA) efficiencies as high as 85%	Maximize battery life

Table 1: *Features and benefits of PMIC devices from Texas Instruments.*

The extensive portfolio of PMICs from Texas Instruments provides many unique features to help solve specific problems. In the TPS65910 family, switch-mode power supplies (SMPSs) (VDD1 and VDD2) provide advanced dynamic voltage scaling (DVS) and are suitable for processor core-voltage rails. In the TPS65911x family, the SMPSs (VDD1 and VDD2) allow programmable transition slew rate of the output voltage and sub-50-ns minimum ON time. These features enable higher switching frequencies, reduced output ripple, and smaller inductor footprint. The TPS80032 features a patented on-chip, frequency-locked PWM control that allows tighter spread of the switching frequency compared to a classic hysteretic buck converter.

All of the example SMPS converters in References 3 through 6 incorporate on-chip overcurrent protection either on the switching (high side) FET or on both switching and rectifier (low side) FETs. Internal soft-start circuitry to limit in-rush current is another feature that supports processors. These enhanced SMPS converters are also optimized for effective external L values between 1.0 to 2.2 µH (1.5 µH typ) and output C values from 4 to 15 µF. The inductor chosen must be rated for DCR and ISAT. Higher inductance reduces the ripple current but degrades transient response (di/dt). The output capacitors can be small-footprint ceramic with X5R or X7R dielectric for low ESR. Input capacitors are also recommended to be low ESR and can be ceramic 4.7 µF, typically with additional electrolytic or tantalum capacitors to reduce supply ringing when distance between the power source and converter is large (such as a wall adapter).

For more details on how TI PMICs can help build a compact, power-efficient wearable, portable, or industrial device to meet your power supply needs, please consult the product information below.

References

1 T. Nabeshima et.al. "Analysis and Design Considerations of a Buck Converter with a Hysteretic PWM Controller," 35th Annual IEEE Power Electronics Specialists Conference 2004, vol. 2, pp 1711-1716.

2. P. Li et.al., "A Delay-Locked Loop Synchronization Scheme for High-Frequency Multiphase Hysteretic DC-DC Converters," IEEE Journal of Solid-State Circuits, Nov. 2009, Vol. 44, No. 11, pp 3131-3145.

3. TPS65910 Datasheet, http://www.ti.com/product/tps65910

4. TPS65911x Datasheet, http://www.ti.com/lit/ds/symlink/tps659113.pdf

5. TPS80032 Datasheet, http://www.ti.com/lit/ds/symlink/tps80032.pdf

6. TPS65218 Datasheet, http://www.ti.com/product/tps65218

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