LM98714

Simplify CCD/CIS Image Capturing with a 3-Channel 16-Bit AFE/Timing

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ANALOG edge℠

Simplify CCD/CIS Image Capturing with a 3-Channel 16-Bit AFE/Timing Generator

Application Note AN-1583

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When designing equipment that deals with amplifying and processing delicate signals, engineers are often faced with the decision of what to mount close to the source, and what can exist further away. These are typically sources like antennas and high impedance audio/video sources. Constraints are more severe with mechanical motion or space. National's LM98714 3-channel, 45 MSPS Analog Front End (AFE) with integrated CCD timing generator and LVDS/CMOS outputs addresses many of these issues.

Multi-Function Peripherals

Multi Function Peripherals (MFPs) are relatively small image copy, scan, and print devices found in thousands of home desktop settings. Historically, these devices have had modest reproduction speeds (gauged in pages per minute) and offered the home user an inexpensive solution to document reproduction. With the speeds of MFPs increasing rapidly, more businesses are finding the MFP satisfies many office tasks once only practical with high speed, industrial-sized digital copiers. The increase in MFP performance comes with new design challenges for the system level architect.

As the speed requirements of the MFP market increase, the system level partitioning shown in ***Figure 1*** exposes new problems. Among the major concerns are increased EMI emissions from high-speed CMOS data traveling across long cables (several hundred mm in most cases) and degraded analog performance. The LM98714 facilitates a breakthrough in system-level partitioning that addresses these concerns.

Analog Front Ends

The LM98714 is an extremely versatile Analog Front End (AFE) with a fully programmable CCD Timing Generator capable of clocking most any sensor. The ADC Data Outputs can be programmed for CMOS levels for legacy designs or slower speed applications (typically <30 MSPS). More importantly, it can also be configured as serialized LVDS for reliable 45 MSPS data transmission. The combination of the full feature AFE, CCD Timing Generator, and LVDS outputs allow the merging of the analog signals onto one board, which eliminates most of the high-speed CMOS digital signaling on the cable.

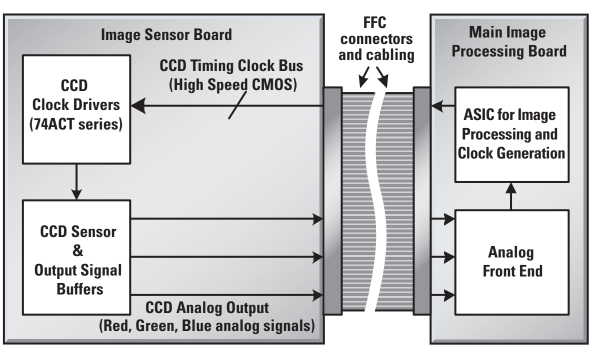

Figure 1. Legacy MFP Image Sensor Block Diagram

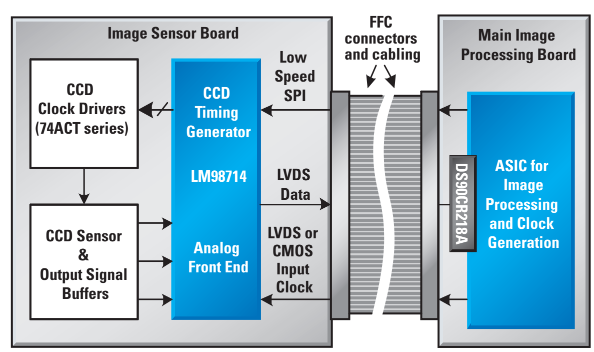

Figure 2. New MFP Image Sensor Block Diagram Partitioning

Engineers designing copiers and scanners are often faced with mechanical and electrical constraints which challenge the system-level budget. The heart of any copier, whether it is a low-cost MFP or high-performance office model, is the image sensor board whose main component is the Charge Coupled Device (CCD) or Contact Image Sensor (CIS). In older MFP applications, as depicted in ***Figure 1***, the image sensor board receives high speed CMOS timing clocks to drive the CCD and sends sensitive analog pixel data to the AFE on the image processing board.

The LVDS output data can be deserialized by the ASIC, or by using one of National's LVDS Channel Link receivers, such as the DS90CR218A as shown in ***Figure 2***.

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In addition to the EMI reduction when using LVDS outputs, the LM98714 allows the use of an LVDS input clock. To achieve an even further reduction in EMI, the input clock can be sent to the LM98714 at the pixel rate instead of the full sampling rate.

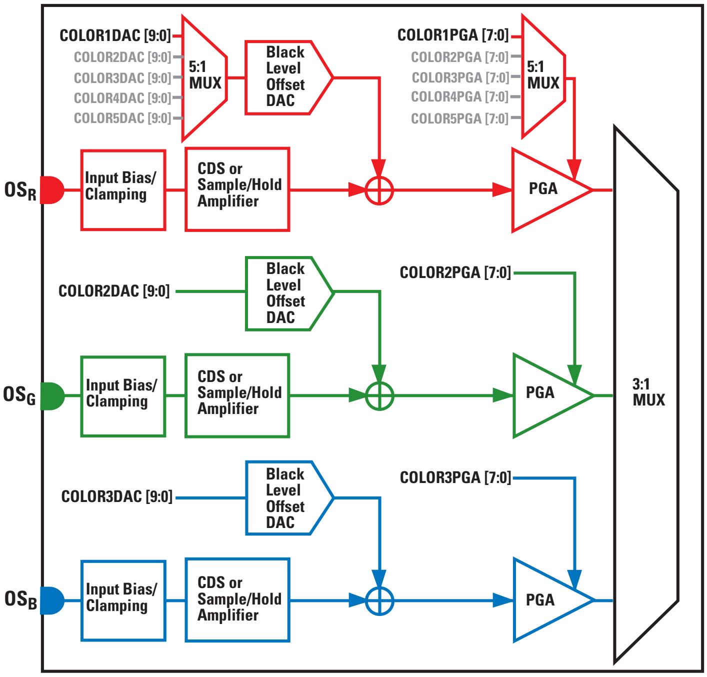

Figure 3. LM98714 Input Diagram

For example, if the CCD has three channels of color per pixel (i.e. Red, Green, and Blue), the LM98714's internal A/D Converter (ADC) runs at 3x the incoming pixel rate. At the maximum sample rate of 45 MSPS, the input clock to the LM98714 can be set to 15 MHz (pixel rate), or 45 MHz (ADC rate). A simple configuration register change via the SPI of the LM98714 makes this feature readily available by applying a multiplication factor to the input clock (3x or 1x respectively). The only remaining non-LVDS signals on the cable with this new architecture are in the SPI interface. The SPI can be run at very low frequencies if found to be a source of significant EMI.

The CCD is a linear image sensor with three color arrays (red, green, and blue) of 10680 elements and an additional array for black-and-white image captures.

In 3-channel mode, OSB, OSG, and OSR are sampled synchronously at the pixel rate. The sampled signals are processed with each channel's offset and gain adjusted independently via the control registers. The order in which pixels are processed from the input to the ADC is fully programmable and is synchronized by the SH pulse. The signals are then routed through a 3-1 MUX to the ADC. *Figure 3* shows a diagram of the channels, and how they are conditioned before the MUX.

The 3 RGB signals are inputted from the left and enter the input bias and clamping block. After the signal is sampled via Sample and Hold or CDS, a unique black offset may be added to each color. This signal may now be gained in the analog domain using the PGAs shown. The MUX now switching at 3 times the pixel rate sends the RGB signals to the ADC to be digitized.

The LM98714 is a fully integrated, high performance 16-bit, 45 MSPS signal processing solution with a maximum input level of 1.2 or 2.4V modes (both with + or – polarity option). Other key specifications include: INL +/- 23 LSB (typ), SNR -74 dB at 0 dB PGA gain, 15/22.5/30 MSPS channel sampling rate, 256 PGA gain steps, and a PGA gain range of 0.7 or 7.84x. The power dissipation is 505 mW (LVDS) and 610 mW (CMOS).

The feature set of the LM98714 is too large to encompass in this article, however, this is one example of its application. Powerful features, such as an analog front end timing generator (used to adjust the sampling points of the analog inputs) and the automatic black level calibration loops are a few of the additional benefits included in the LM98714 architecture. ■

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