*Application Note*

# *Sine to Square Wave Conversion Using Clock Buffers*

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**ABSTRACT**

Applications requiring extremely low phase noise often use OCXO (Oven Controlled Crystal Oscillator) or TCXO (Temperature Compensated Crystal Oscillator) as reference clock in the system. OCXO and TCXO's sinewave output often becomes a bottle neck for slew rate sensitive devices in the clock tree due to fixed amplitude and frequency. Slew rate sensitivity of the subsequent clock devices results in phase noise degradation throughout the clock chain.

There are multiple ways to get around this problem by using external circuity or integrated chips like clock buffers. In this application note, we compare performance improvements in clock trees with TI clock buffer devices with various output format, input power levels and frequencies. This document is to serve as reference to choose the best sine to square wave clock buffer based on application requirements.

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## Trademarks

# 1 Generic Clock Tree

Generally, a clock tree in a system consists of primary reference that is either fanned-out using clock buffers or multiplied / divided through synthesizers (PLL / DPLL) to generate different frequencies. Figure 1-1 shows a generic clock tree of a system containing ADCs, FPGAs or transceivers.

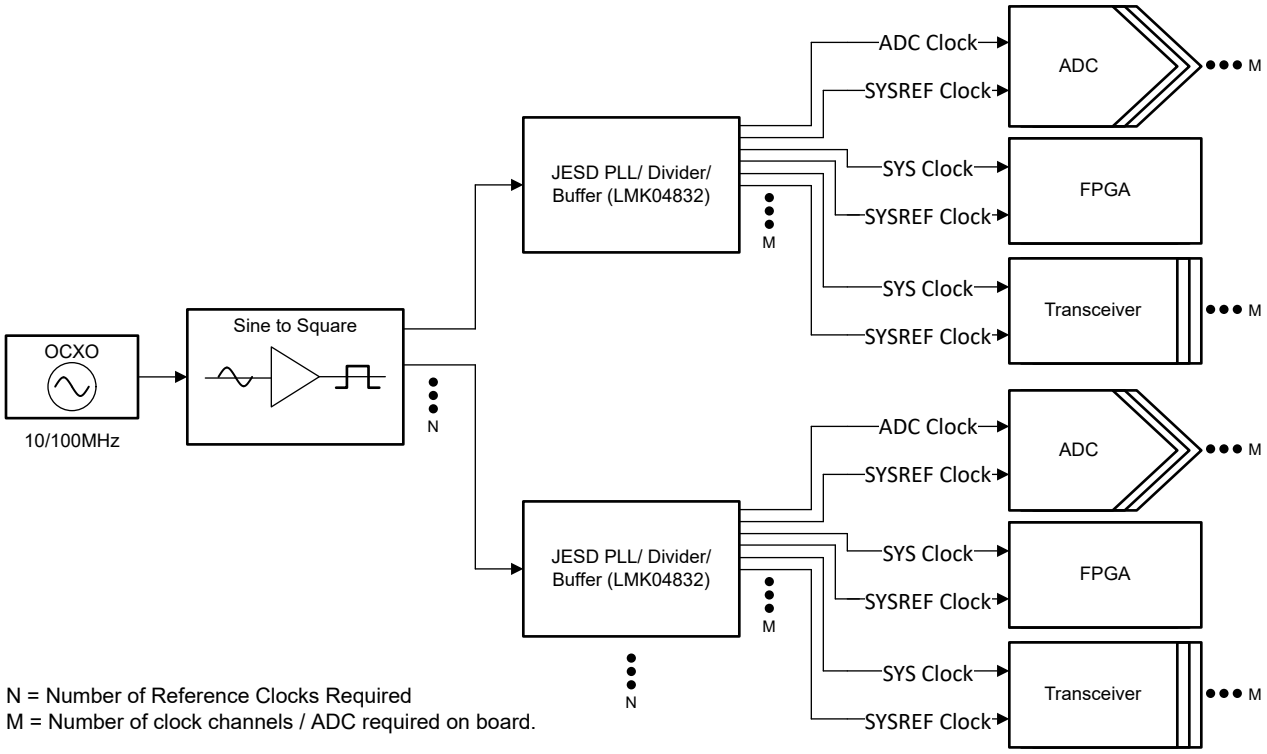



**Figure 1-1. General Clock Tree**

Applications requiring low phase noise requirements that utilizes sine wave reference are found in medical, communication, T&M and A&D systems. For example, radars are dependent on low phase noise to detect one or more objects accurately.

Additive phase noise gradually adds up with each device in the clock tree. Good system design practices are crucial to avoid any additional degradation. One of those consideration is due to the input slew rate and amplitude requirements for different devices when converting sine wave to logic levels.

# 2 Sine Wave Slew Rate Requirement

Slew rate of sine wave is dependent on frequency of operation and voltage of signal. Complying with input slew rate requirement for clock devices is necessary to provide certain phase noise performance.

To imporve phase noise of clock devices, higher slew input is recommended. Most vendors have this recommendation outlined in the data sheet for buffer, synthesizer, and jitter cleaners.

Slew rate of sine wave input signal can be changed by increasing/decreasing frequency or voltage as shown in Equation 1.

$$2 \times \pi \times f \times V \tag{1}$$

Both of these variables cannot be controlled when using a fixed output amplitude and frequency source which often is the case for systems using OCXO/TCXOs.

# 3 Current Approach vs Clock Buffer

Current approaches to solve slew rate sensitivity problem use additional circuitry is input of clock devices that takes additional space on the board. The overall system becomes costly and dependency of multiple discrete components also adds complexity in design. Furthermore, using an amplifier or comparator stage adds noise in the subsequent clock tree because amplifier or comparators are usually not optimized for phase noise performance like clock buffers. Figure 3-1 shows a generalized version of current approach without clock buffers. A better approach is to use integrated chip like clock buffer which has all the required circuity to amplify slow slew rates signals and optimized for all clocking parameters. Clock buffer converts the slow slew rate inputs to logic levels with very low additive phase noise, thus boosting the signal slew rate to also minimize phase noise degradation though the device in clock tree. Also, clock buffers reduces external BOM (bill of materials) depending on different features like internal biasing and AC coupling mode, and so on.

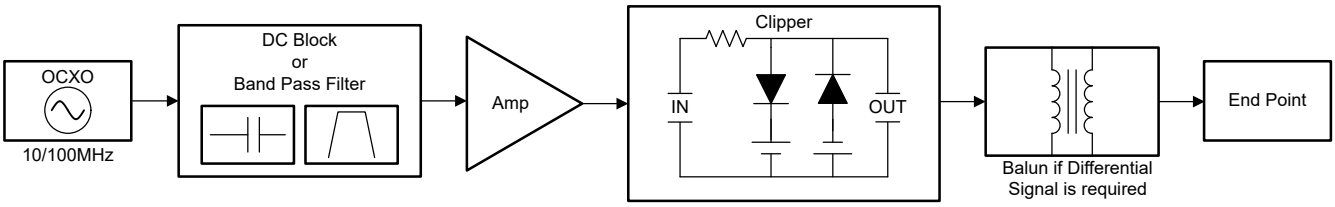



**Figure 3-1. Generic Slew Rate Improvement Approach**

TI has a wide portfolio of clock buffers that support sine wave input for single ended, differential and configurable buffers. TI clock buffers covers all the logic levels from LVCMOS (LMK1C110x), LVDS (LMK1D1xxx), LVPECL (CDCLVP12xx), and Universal buffers that support all industry standard output and inputs formats (LMK0030x, LMK01000, CDCLVC1310). This application note specifically uses LMK1C110x family of buffers for performance measurements due to inherent low additive phase noise.

# 4 Clock Buffer Implementation

While using the clock buffer as sine to square wave conversion, make sure to consider specific input VOH, VOL, VOD, input common mode, AC coupled inputs and internal or external biasing requirements of each clock buffer.

In the following sections, most commonly used input interface, external or internal biasing tips are discussed for TI buffers. Since the input architecture for different generation of buffers get improvements over time. There are subtle differences to keep in mind interfacing clock signal to the input of each buffer.

## 4.1 Clock Buffer Common Input Stages

There are two major buffer input stages, single ended (LVCMOS) or differential (LVDS, LVPECL, CML, LP-HCSL, HCSL, HTSL). The differential inputs can be standard specific or universal inputs. Universal inputs accept all the supported standard input driver interface.

Differential inputs can also be used as single ended input. Inverting or non-inverting input is selected as reference clock input and the other input is DC biased to the mid point reference clock input. Both clock reference and DC biased inputs are set within the input swing and common mode range requirements of each device.

In the following sections, we discuss internal or external DC bias use, single ended input and differential input re-bias techniques across different TI clock buffer families.

## 4.2 Choosing Between Internal or External DC Bias

Generally, TI differential clock buffer families have two different DC biasing options, internal bias with small DC offset or internal DC bias with hysteresis. Both DC bias options are used to set the outputs to low state and avoid glitches on the outputs when there is loss of signal or clock. Figure 4-1 and Figure 4-2 shows both biasing techniques.

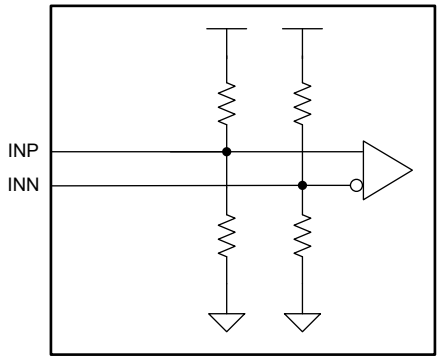



**Figure 4-1. Internal DC Bias Offset Architecture**

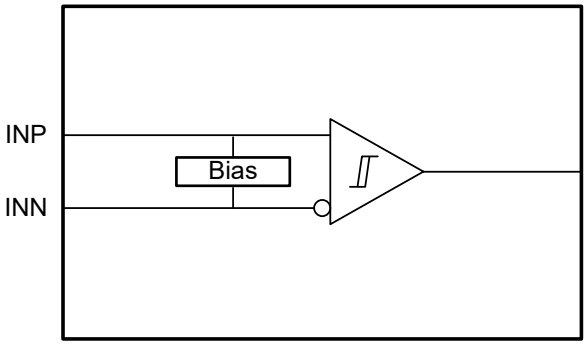



**Figure 4-2. Internal DC Bias with Hysteresis**

Things to consider before opting for internal and external DC bias.

- Check if the part has internal DC bias option, otherwise use external bias through a voltage divider. Internal bias at the inputs can be checked by probing the inputs with a high impedance on scope. Some TI devices offer VAC _REF pin for external biasing which can be used instead of voltage divider.
- In case of internal DC bias with an offset at the input. External DC bias is recommended when using sine wave input to avoid duty cycle distortion on the output. Duty cycle distortion is result of sine wave imbalance at the switching threshold as shown in Figure 4-3.
- When using large input signals at the differential input stage. Make sure that internal bias is good enough that the low or high level of the input signal doesn't violate the input absolute maximum values in the data sheet. Otherwise re-bias the input signal with an external bias to avoid VIH and VIL absolute maximum values violations.
- Refer to device data sheet for specific input termination needs due to any specific input requirements.

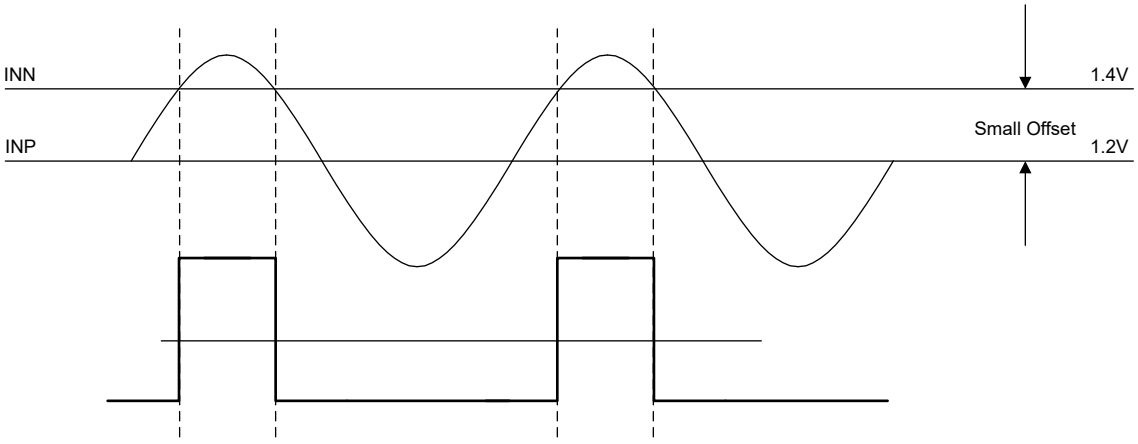



**Figure 4-3. Duty Cycle Distortion with Imbalanced Sine Wave**

## 4.3 Single Ended or LVCMOS Signal

Single ended or LVCMOS input stage detects 0 or 1 based on input signal level around threshold (Vt) point. VIH and VIL limits are recommended to avoid detection issues over temperature and voltage across multiple devices.

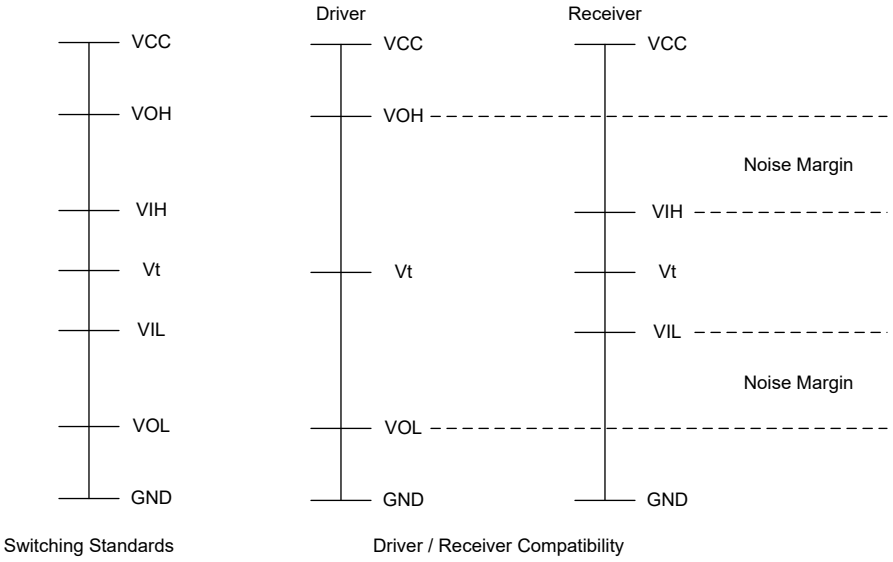



**Figure 4-4. LVCMOS Thresholds**

To use sine wave with a LVCMOS buffers input stage, LVCMOS receiver threshold specification applies for the input signal. Since most of the time the sine wave signal generated from OCXO or other sources is centered around 0V DC offset. The input signal is re-biased to threshold Vt or VDD/2 value either externally or internally (if available).

Figure 4-5 shows a simplified diagram on biasing using voltage divider at the input. LMK1C110x use the same biasing configuration.

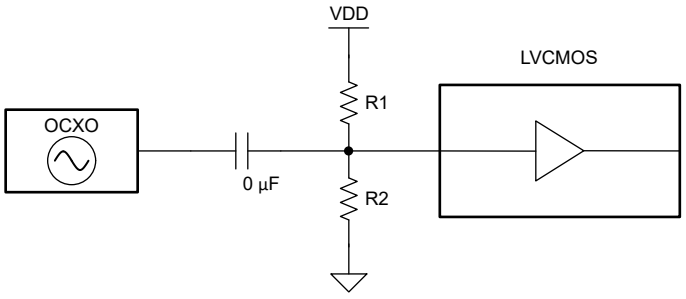



**Figure 4-5. Re-biasing to LVCMOS Levels**

R1 and R2 are same value resistor to get the VDD/2. Matching the transmission line impedance can be done with 100Ω resistor for both R1 and R2 which results in more power consumption due to higher current through the resistor. To reduce power consumption 1K or 10K resistor values can be used as well.

**Table 4-1. Current Consumption for Voltage Divider**

| VDD | 100Ω | 1kΩ | 10kΩ |
|---|---|---|---|
| 3.3V | 16.5mA | 1.65mA | 0.165mA |
| 2.5V | 12.5mA | 0.125mA | 0.125mA |
| 1.8V | 9mA | 0.9mA | 0.09mA |

## 4.4 Differential Inputs

Input swing, amplitude, input common mode, and proper DC bias are important requirements to know when differential AC or DC coupled mode is used.

For sine wave input signals, INN pin or reference pin is always the biased at mid-point of active clock input signal. This avoids duty cycle distortion as shown below in the Figure 4-6.

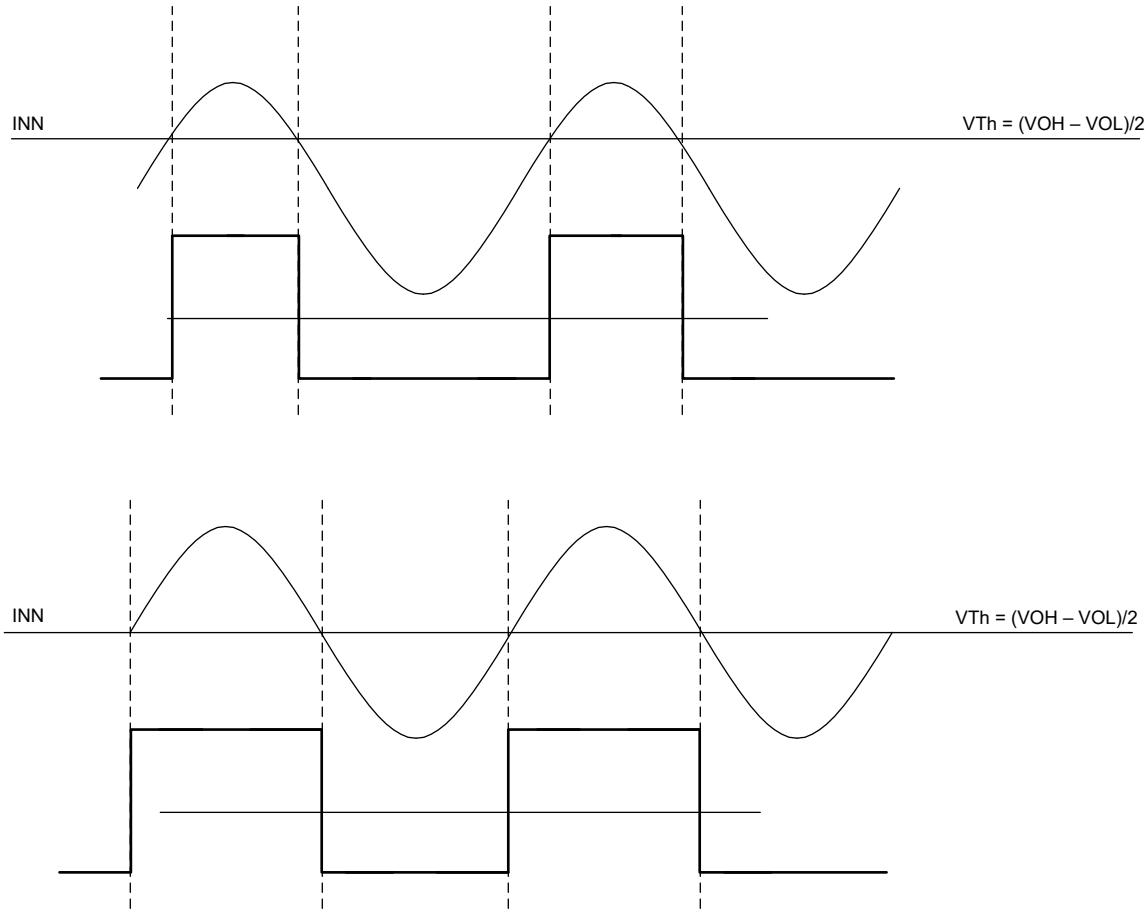
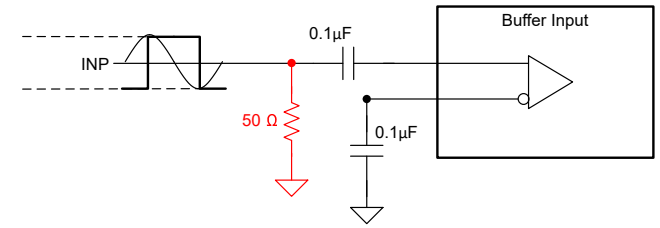



**Figure 4-6. Duty Cycle Distortion**

Following are some common DC re-bias techniques and considerations which are shared across TI devices.

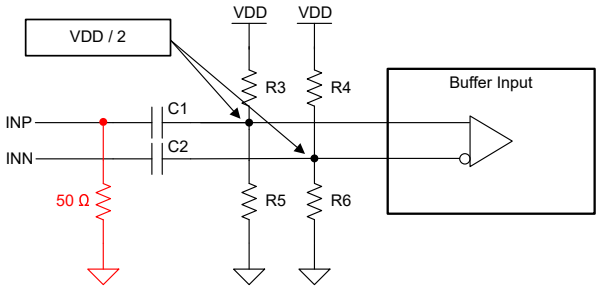
- AC Coupled Internal DC Bias Option: Most TI devices have internal DC bias of some sort that is specified in the data sheet. User can AC couple either single ended or differential inputs without the need for external components. For this type of use case, make sure to consider the input amplitude requirements, internal bias type specified for each device. AC coupled single ended internal options in shown in Figure 4-7.
- AC Coupled External DC Bias Option: If there is no internal bias is available on the clock input of device or the duty cycle is a concern due to any DC offset between internal bias of INP and INN pins while dealing with smaller amplitude or sine wave input. External voltage divider is recommended to re-bias the signals to desired DC levels within the input common mode requirement of the device. External bias is helpful for start-up times because capacitors charging time can be controlled compared to internal weak bias option. An example of external bias for both single ended and differential case is shown in Figure 4-8.
- DC Coupled single Ended Input using Differential Input: When using DC coupled LVCMOS or any other format single-ended waveform. INN or the unused input is set to the mid point of input signal as shown in Figure 4-9.
- External DC Bias with VAC_Pin: Some TI devices offer a VAC_REF pin to re-bias inputs shown in Figure 4-10. This reduces start-up times while using fewer components than external DC bias option with voltage divider circuit.

Using differential inputs as single ended input case (sinewave or LVCMOS), if there is a need to reduce the input swing to meet data sheet input requirements, a 50Ω resistor to ground shown in Figure 4-7, Figure 4-8 andFigure 4-10 usually applied. Furthermore, INN pin also AC coupled to ground or left floating for single ended use case of differential inputs.




If the input amplitude or Vpp is greater than datasheet specification a 50Ω resistor to ground is used to meet the input requirements.

**Figure 4-7. AC Coupled Internal DC Bias Option**




If the input amplitude or Vpp is greater than datasheet specification a 50Ω resistor to ground is used to meet the input requirements. This is usually not required in this case because bias point is set around VDD/2 and there is usually enough room for the input swing between GND and VDD for absolute maximum specification. This re-biasing is true for both differential (using INP and INN) and single ended input waveforms(using just INP).

**Figure 4-8. AC Coupled External DC Bias Option**

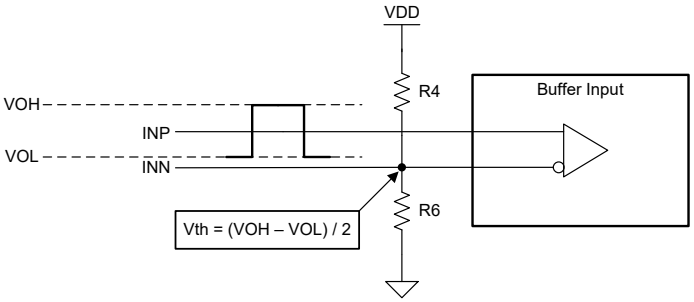
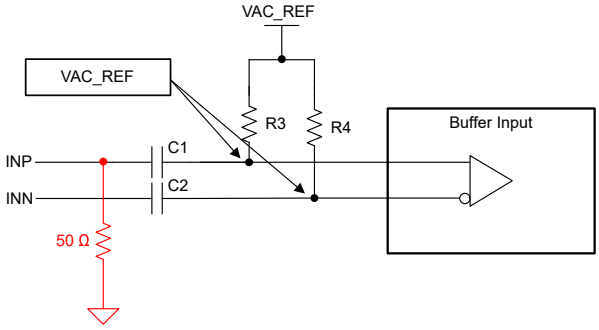



**Figure 4-9. DC Coupled Single Ended Input with Differential Input Stage**




If the input amplitude or Vpp is greater than datasheet specification a 50Ω resistor to ground is used to meet the input requirements. This re-biasing is true for both differential (using INP and INN) and single ended input waveforms(using just INP).R3 and R4 are usually 50Ω.

**Figure 4-10. External DC Bias with VAC_REF Pin Option**

# 5 Performance Improvements, Results With Clock Buffer

Adding a low noise clock buffer between OCXO/TCXO input and the slew-rate sensitive clock devices helps minimize the phase noise degradation. Phase noise improvement in PLL based clock devices is often debated because input buffer stage on the PLLs devices critical for phase noise is extremely low noise so adding a buffer to improve slew rate ends up elevating the total phase noise. In the following section, we present a study with and without low noise sine to square buffer before the LMX2820 synthesizer device and note the results.

## 5.1 FSWP Phase Noise Analyzer Measurements Case

When dealing at lower frequency, phase noise using low noise clock buffer (LMK1C110x) shows better performance than the source input at lower frequencies from SMA100B on the FSWP phase noise analyzer as shown in Figure 5-2. This shows that slew rate sensitivity is impacting the internal circuitry of the FSWP at lower frequencies and the source measurement comes out to be pessimistic. When the same input from SMA100B at lower frequencies is buffered through LMK1C110x shows better results at lower offsets frequencies. Similar concept applies to all the PLL based synthesizer device which are slew rate sensitive.

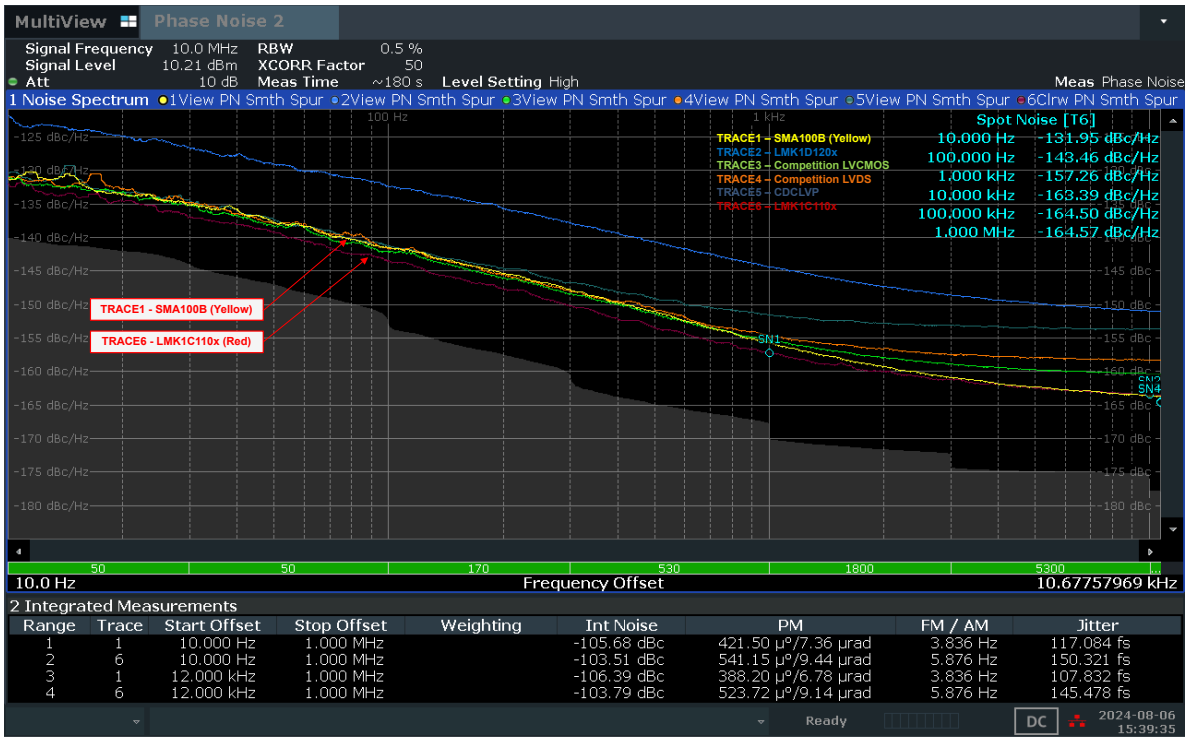



**Figure 5-1. LMK1C110x 10MHz Output Phase Noise Gap Between Source and Buffer**

At higher frequencies the gap between source noise measurement and buffer measurement reduces on the FSWP since better slew rate is helping the measurement instrument at higher frequencies as shown in Figure 5-2. Adding a low noise buffer still helps improve the buffer noise performance specifically at lower input amplitudes but at some point addition of clock buffer is not going to help at all because of higher slew rates. Since most of the systems where close in phase noise is important start at lower frequencies, addition of buffer significantly improves the margins.

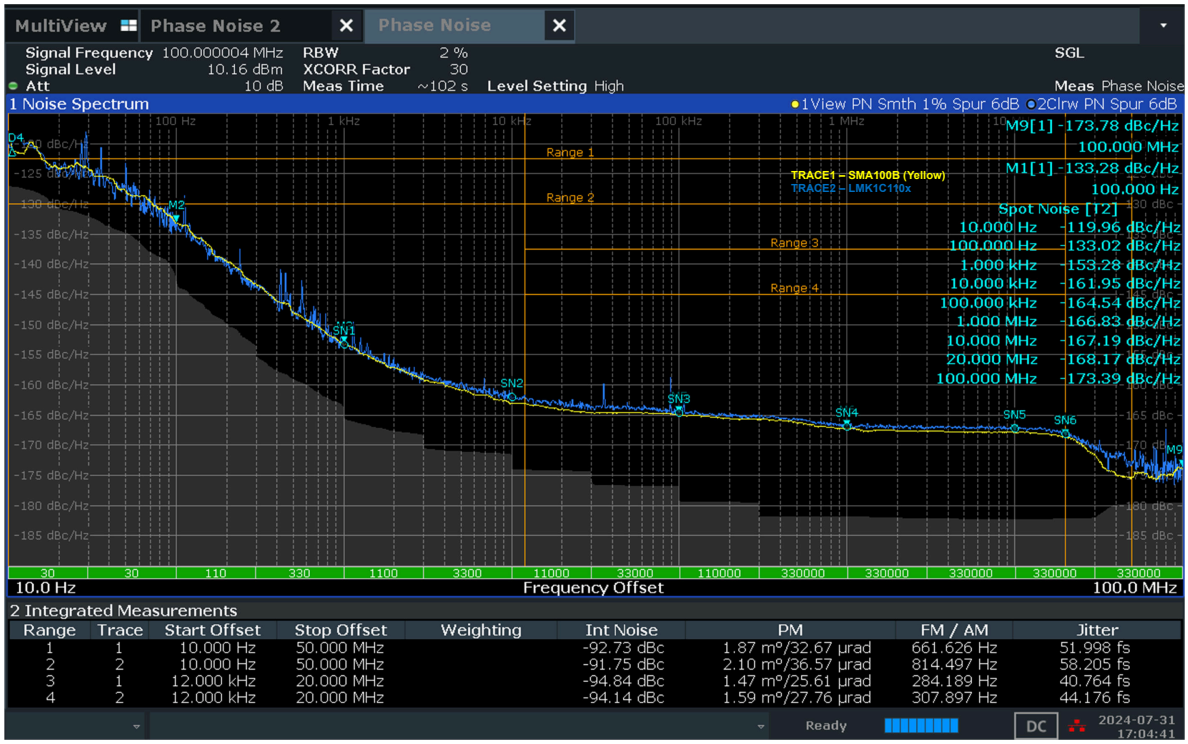



**Figure 5-2. LMK1C110x 100MHz Output Phase Noise Gap Between Source and Buffer**

Synthesizer devices like LMX2820 running at higher frequencies have a wide input frequency range, input stage is usually optimized for higher frequencies. Phase noise degradation is pronounced when using a 10MHz input source or other lower frequencies. At 100MHz since the slew rate is much higher performance degradation is not significant but there is still some improvement specifically at lower input power levels when using the low noise sine to square wave conversion buffers.

## 5.2 TI LMX2820 Noise Improvements With Sine to Square Wave Clock Buffer

Based on FSWP noise analyzer findings we performed the same experiment on TI PLL based synthesizer LMX2820. A 10MHz sine wave input at different power levels was injected directly and through the low noise buffer (LMK1C110x).

There were two cases in the experiment,

- Case 1: Sine wave input from SMA100B to LMX2820 at different power levels.
- Case 2: Sine wave input from SMA100B at same power levels as Case 1 amplified with LMK1C110x clock buffer into LMX2820.

Different power levels at the input were used to see the impact on the performance of PLL vs buffer input stage.

As shown in the Figure 5-3, there is significant improvement in phase noise of the PLL which results in improved jitter performance across different bands. PLL performance gap increases as we lower the power at 10MHz input reference shown between Trace 1 (Yellow) and Trace 4 (Orange) in Figure 5-3. This is due to further degradation in slew rate at the input.

At higher input frequencies shown in Figure 5-4, the performance gaps between the sine to square wave case gets smaller but if the input amplitude is small then buffer helps imporve phase noise.

Adding a buffer stage at lower power helps improve the performance margins in the system. Even at 14dBm and 10dBm (Trace 6: Red ) input power level, better slew rates from the clock buffer outperforms the PLL input stage. This shows that clock buffer can still be used even at higher power levels to further enhance the phase noise.

**Figure 5-3. 10MHz Reference Input to LMX2820 100MHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

**Figure 5-4. 100MHz Reference Input to LMX2820 1GHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

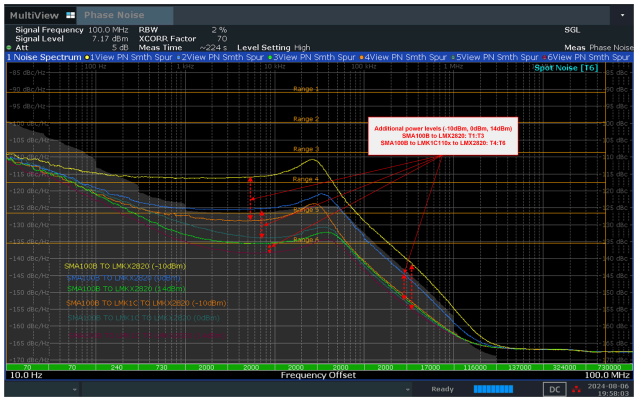


**Figure 5-5. 10MHz Reference Input to LMX2820 100MHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -10dBm, 0dBm, 14dBm)**

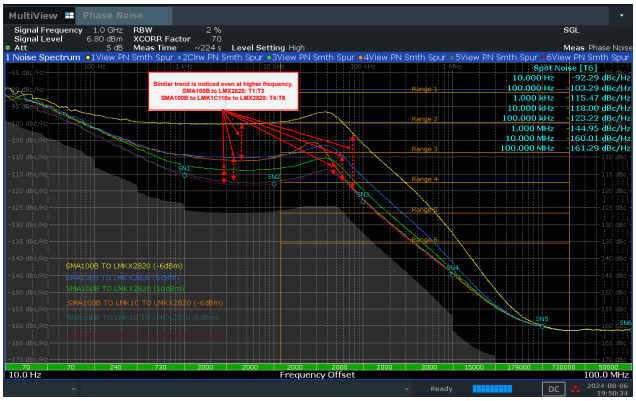


**Figure 5-6. 10MHz Reference Input to LMX2820 1GHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

Following jitter measurement plots show the jitter impact at different bands when using the direct sinewave input to LMX2820 versus sinewave input through LMK1C110x clock buffer . Integrated jitter for the worst-case option improve approximately 5 times when using the clock buffer shown in Figure 5-11.

**Figure 5-7. Total RMS Jitter (12kHz - 20MHz) 10MHz Reference Input to LMX2820 100MHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

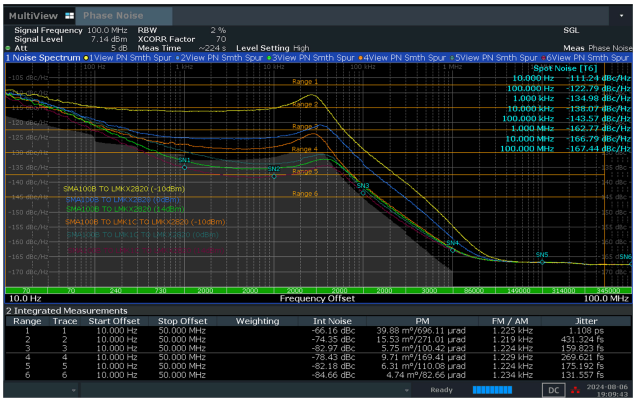


**Figure 5-8. Total RMS Jitter (12kHz - 20MHz: 10MHz Reference Input to LMX2820 100MHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -10dBm, 0dBm, 14dBm)**

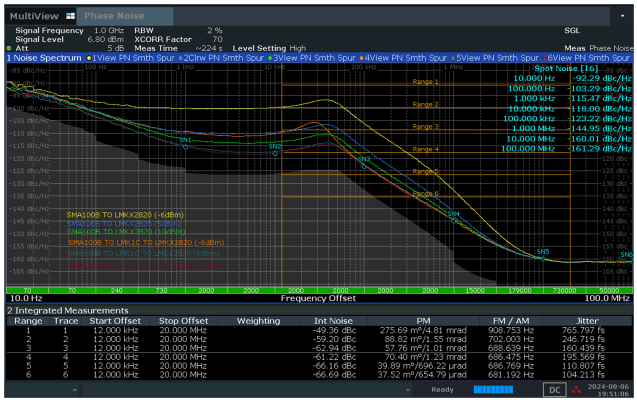


**Figure 5-9. Total RMS Jitter (12kHz - 20MHz): 10MHz Reference Input to LMX2820 1GHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

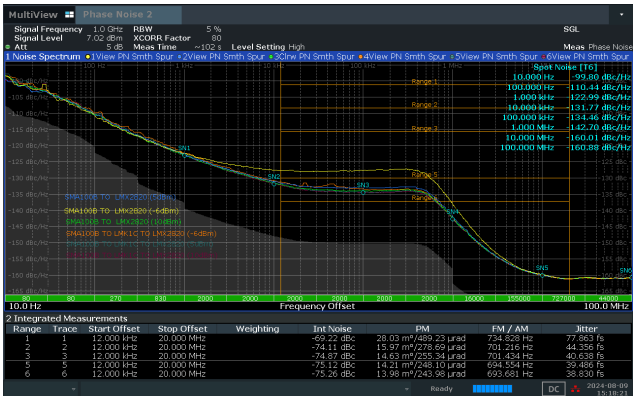


**Figure 5-10. Total RMS Jitter (12kHz - 20MHz): 100MHz Reference Input to LMX2820 1GHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

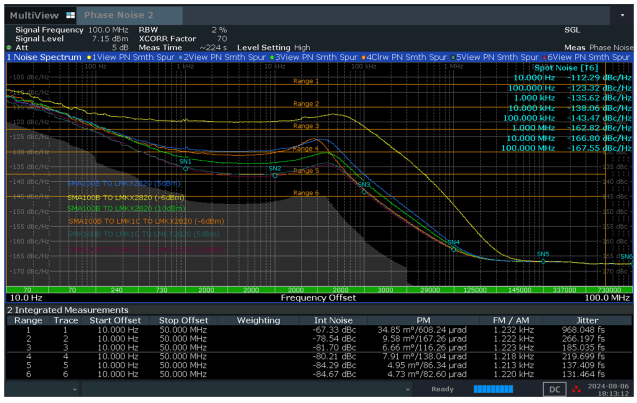


**Figure 5-11. Total RMS Jitter (10Hz - 50MHz) 10MHz Reference Input to LMX2820 100MHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

**Figure 5-12. Total RMS Jitter (10Hz - 50MHz: 10MHz Reference Input to LMX2820 100MHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -10dBm, 0dBm, 14dBm)**

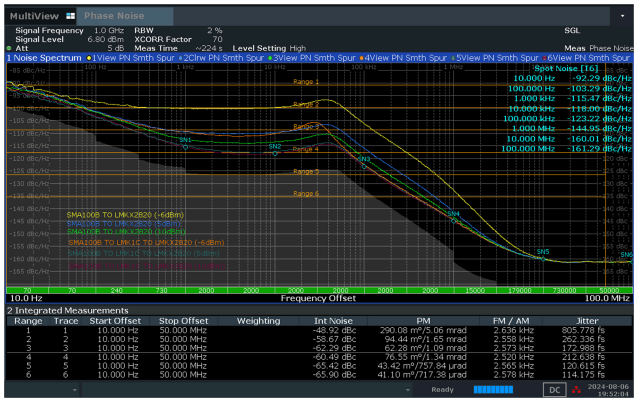



**Figure 5-13. Total RMS Jitter (10Hz - 50MHz): 10MHz Reference Input to LMX2820 1GHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

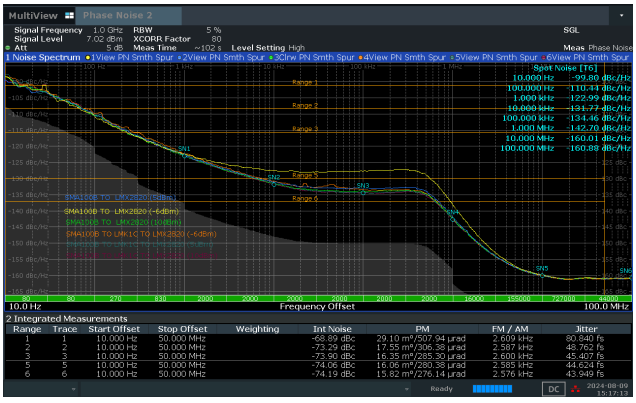



**Figure 5-14. Total RMS Jitter (10Hz - 50MHz): 100MHz Reference Input to LMX2820 1GHz Output With or Without Buffer (Case 1: T1 to T3, Case 2: T4 to T6, Input power: -6dBm, 5dBm, 10dBm)**

### *5.2.1 LMX2820 Phase Noise and RMS Jitter Results Summary*

Table 5-1, Table 5-2 and Table 5-4 shows a quantitative summary of improvements when using sine to square wave buffer. Few key observations to note.

- LMX2820 PLL noise is significantly improved around 10kHz offset. Far out noise is dominated by VCO.
- RMS jitter and phase noise at higher power level is better with buffer compared to without buffer case. For worst case ((lowest power level) jitter reduced by 75.6% while the best case (highest power level) buffers reduces the jitter by 20%.
- There is slight improvement at 100MHz input frequency as well but improvement is not significant compared to lower frequency use case as shown in Table 5-3 and Table 5-5. One reason for this is the doubler stage used on the LMX2820 to improve slew rate on the device input.

**Table 5-1. Phase Noise: 10MHz Input, 100MHz Output**

| Parameter | | Data | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Power | | -10 | -6 | 0 | 5 | 10 | 14 | dBm |
| Trace | | Trace 1: Yellow | | Trace 2: Blue | | Trace 3: Green | | - |
| Case 1: Phase Noise without buffer | 10Hz | -108.93 | -109.24 | -110.16 | -111.43 | -111.28 | -110.3 | dBC |
| | 100Hz | -114.68 | -117.08 | -119.04 | -120.96 | -121.32 | -120.84 | |
| | 1kHz | -116.29 | -119.31 | -125.16 | -128.95 | -131.84 | -132.96 | |
| | 10kHz | -115.2 | -119.78 | -124.95 | -129.29 | -133.58 | -135.34 | |
| | 100kHz | -128.82 | -121.58 | -134.10 | -137.62 | -140.04 | -141.22 | |
| | 1MHz | -154.72 | -147.92 | -158.94 | -161.33 | -162.04 | -162.20 | |
| | 10MHz | -166.76 | -166.75 | -166.87 | -166.79 | -166.80 | -166.84 | |
| | 100MHz | -167.49 | -167.53 | -167.57 | -167.54 | -167.46 | -167.57 | |
| Trace | | Trace 4: Orange | | Trace 5: Dusty Blue | | Trace 6: Red | | - |
| Case 2: Phase Noise with buffer | 10Hz | -109.73 | -111.12 | -110.34 | -112.72 | -112.29 | -111.24 | dBC |
| | 100Hz | -121.17 | -122.06 | -119.96 | -123.5 | -123.32 | -122.79 | |
| | 1kHz | -127.26 | -129.94 | -129.64 | -135.14 | -135.62 | -134.98 | |
| | 10kHz | -128.17 | -130.12 | -133.81 | -137.32 | -138.06 | -138.07 | |
| | 100kHz | -140.83 | -142.73 | -142.23 | -142.97 | -143.47 | -143.57 | |
| | 1MHz | -162.13 | -162.50 | -162.52 | -162.75 | -162.82 | -162.77 | |
| | 10MHz | -166.79 | -166.77 | -166.71 | -166.82 | -166.80 | -166.79 | |
| | 100MHz | -167.51 | -167.51 | -167.6 | -167.54 | -167.56 | -167.44 | |
| Phase Noise Delta: Case 2 - Case 1 | 10Hz | -0.8 | -1.88 | -0.18 | -1.29 | -1.01 | -0.94 | dBC |
| | 100Hz | -6.49 | -4.98 | -0.92 | -2.54 | -2 | -1.95 | |
| | 1kHz | -10.97 | -10.63 | -4.48 | -6.2 | -3.78 | -2.02 | |
| | 10kHz | -12.97 | -10.34 | -8.86 | -8.03 | -4.48 | -2.73 | |
| | 100kHz | -12.01 | -21.15 | -8.13 | -5.32 | -3.43 | -2.35 | |
| | 1MHz | -7.41 | -14.58 | -3.58 | -1.42 | -0.78 | -0.57 | |
| | 10MHz | -0.03 | -0.02 | 0.16 | -0.03 | 0 | 0.05 | |
| | 100MHz | -0.02 | 0.02 | -0.03 | 0 | -0.1 | 0.13 | |

**Table 5-2. Phase Noise: 10MHz Input, 1GHz Output**

| Parameter | | Data | | | Unit |
|---|---|---|---|---|---|
| Input Power | | -6 | 5 | 10 | dBm |
| Trace | | Trace 1: Yellow | Trace 2: Blue | Trace 3: Green | - |
| Case 1: Phase Noise without buffer | 10Hz | -89.51 | -90.23 | -91.79 | dBC |
| | 100Hz | -97.59 | -101.37 | -101.54 | |
| | 1kHz | -100.09 | -109.46 | -112.42 | |
| | 10kHz | -99.74 | -109.75 | -113.45 | |
| | 100kHz | -106.25 | -116.11 | -119.71 | |
| | 1MHz | -132.78 | -141.33 | -143.48 | |
| | 10MHz | -159.69 | -160.05 | -160.09 | |
| | 100MHz | -161.12 | -161.08 | -161.21 | |
| Trace | | Trace 4: Orange | Trace 2: Dusty Blue | Trace 3: Green | - |

**Table 5-2. Phase Noise: 10MHz Input, 1GHz Output (continued)**

| Parameter | | Data | | | Unit |
|---|---|---|---|---|---|
| Case 1: Phase Noise without buffer | 10Hz | -91.55 | -93.20 | -92.29 | dBC |
| | 100Hz | -101.64 | -103.60 | -103.29 | |
| | 1kHz | -109.23 | -114.71 | -115.47 | |
| | 10kHz | -110.154 | -117.31 | -118.00 | |
| | 100kHz | -122.66 | -122.68 | -123.22 | |
| | 1MHz | -144.60 | -144.63 | -144.95 | |
| | 10MHz | -159.83 | -159.94 | -160.01 | |
| | 100MHz | -161.17 | -161.04 | -161.29 | |
| Phase Noise Delta: Case 2 - Case 1 | 10Hz | -2.04 | -2.97 | -0.5 | dBC |
| | 100Hz | -4.05 | -2.23 | -1.75 | |
| | 1kHz | -9.14 | -5.25 | -3.05 | |
| | 10kHz | -10.414 | -7.58 | -4.55 | |
| | 100kHz | -16.41 | -6.57 | -3.51 | |
| | 1MHz | -11.81 | -3.3 | -1.47 | |
| | 10MHz | -0.14 | 0.111 | 0.08 | |
| | 100MHz | -0.05 | 0.04 | -0.08 | |

**Table 5-3. Phase Noise: 100MHz Input, 1GHz Output**

| Parameter | | Data | | | Unit |
|---|---|---|---|---|---|
| Input Power | | -6 | 5 | 10 | dBm |
| Trace | | Trace 1: Yellow | Trace 2: Blue | Trace 3: Green | - |
| Case 1: Phase Noise without buffer | 10Hz | -98.37 | -99.46 | -98.25 | dBC |
| | 100Hz | -110.61 | -110.59 | -110.44 | |
| | 1kHz | -122.42 | -122.73 | -123.05 | |
| | 10kHz | -127.55 | -131.08 | -131.60 | |
| | 100kHz | -127.63 | -133.04 | -133.93 | |
| | 1MHz | -138.10 | -142.00 | -142.47 | |
| | 10MHz | -159.88 | -159.90 | -159.97 | |
| | 100MHz | -160.91 | -161.00 | -160.94 | |
| Trace | | Trace 4: Orange | Trace 2: Dusty Blue | Trace 3: Green | - |
| Case 1: Phase Noise without buffer | 10Hz | -98.28 | -97.79 | -99.78 | dBC |
| | 100Hz | -109.90 | -110.39 | -110.44 | |
| | 1kHz | -122.34 | -122.71 | -122.99 | |
| | 10kHz | -130.77 | -131.49 | -131.77 | |
| | 100kHz | -133.43 | -134.26 | -134.46 | |
| | 1MHz | -142.43 | -142.67 | -142.70 | |
| | 10MHz | -160.06 | -159.93 | -160.01 | |
| | 100MHz | -161.08 | -161.07 | -161.88 | |
| Phase Noise Delta: Case 2 - Case 1 | 10Hz | 0.08 | 1.67 | -1.54 | dBC |
| | 100Hz | 0.70 | 0.12 | 0 | |
| | 1kHz | 0.08 | 0.02 | 0.05 | |
| | 10kHz | -3.23 | -0.40 | -0.17 | |
| | 100kHz | -5.80 | -1.22 | -0.52 | |
| | 1MHz | -4.33 | -0.66 | -0.23 | |
| | 10MHz | -0.18 | -0.04 | -0.03 | |
| | 100MHz | -0.17 | -0.07 | -0.06 | |

**Table 5-4. Total RMS Jitter 10MHz Input, 100MHz and 1GHz Output**

| Parameter | | | Data | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Input PowerCondtion | | | -10 | -6 | 0 | 5 | 10 | 14 | dBm |
| Trace | | | Trace 1: Yellow | | Trace 2: Blue | | Trace 3: Green | | - |
| Case 1: RMS Jitter without Buffer | FOUT = 100MHz | 12kHz - 20MHz | 1027 | 931.858 | 403.643 | 244.971 | 165.222 | 138.81 | fs |
| | | 10kHz - 50MHz | 1108 | 968.048 | 431.324 | 266.197 | 185.035 | 159.823 | |
| | FOUT = 1GHz | 12kHz - 20MHz | - | 765.797 | - | 246.719 | 160.439 | - | |
| | | 10kHz - 50MHz | - | 805.778 | - | 262.336 | 172.988 | - | |
| Trace | | | Trace 4: Orange | | Trace 5: Dusty Blue | | Trace 3: Red | | - |
| Case 1: RMS Jitter without Buffer | FOUT = 100MHz | 12kHz - 20MHz | 243.679 | 197.268 | 150.522 | 118.663 | 111.924 | 110.943 | fs |
| | | 10kHz - 50MHz | 269.621 | 219.699 | 175.192 | 137.409 | 131.464 | 131.557 | |
| | FOUT = 1GHz | 12kHz - 20MHz | - | 195.569 | - | 110.807 | 104.213 | - | |
| | | 10kHz - 50MHz | - | 212.638 | - | 120.615 | 114.175 | - | |
| RMS Jitter Delta: Case 2 - Case 1 | FOUT = 100MHz | 12kHz - 20MHz | -783.321 | -734.59 | -253.121 | -126.308 | -53.298 | -27.867 | fs |
| | | 10kHz - 50MHz | -838.379 | -748.349 | -256.132 | -128.788 | -53.571 | -28.266 | |
| | FOUT = 1GHz | 12kHz - 20MHz | - | -570.228 | - | -135.912 | -56.226 | - | |
| | | 10kHz - 50MHz | - | -593.140 | - | -141.721 | -58.813 | - | |

**Table 5-5. Total RMS Jitter 100MHz Input, 1GHz Output**

| Parameter | | | Data | | | Unit |
|---|---|---|---|---|---|---|
| Input PowerCondtion | | | -6 | 5 | 10 | dBm |
| Trace | | | Trace 1: Yellow | Trace 2: Blue | Trace 3: Green | - |
| Case 1: RMS Jitter without Buffer | FOUT = 1GHz | 10kHz - 50MHz | 80.840 | 48.762 | 45.407 | fs |
| Trace | | | Trace 4: Orange | Trace 5: Dusty Blue | Trace 3: Red | - |
| Case 1: RMS Jitter without Buffer | FOUT = 1GHz | 10kHz - 50MHz | 47.177 | 44.624 | 43.949 | fs |
| RMS Jitter Delta: Case 2 - Case 1 | FOUT = 1GHz | 10kHz - 50MHz | -33.663 | -4.138 | -2.458 | fs |

# 6 Sine to Square Wave Clock Buffer Comparison

Since our previous findings shows that low noise clock buffers can help improve the phase noise performance when doing the sine to square conversion. In this section, we provide a comparison of different clock buffers from TI and other vendors to use as a reference for sine to square conversion.

We used 10MHz sine wave input at 10dBm input power level for all the buffers under the same conditions. LMK1C110x shows the lowest total phase noise among all the buffers in the comparison. Table 6-1 provides additive phase noise numbers when using the direct sine wave input to each buffer as this is the main use case in actual systems when sine to square wave conversion is needed.

Since the equipment can suffer from slew rate issues described in FSWP Phase Noise Analyzer Measurements Case, cascaded configuration is used for actual additive phase noise modeling of LMK1C110x and other devices in the later sections.

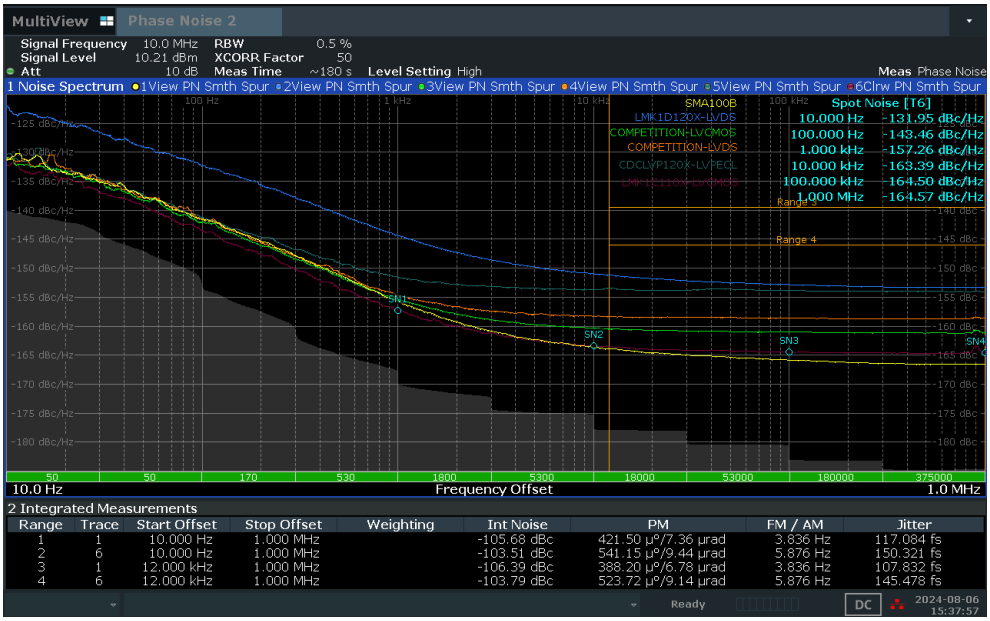



**Figure 6-1. Sine to Square Wave Buffer Comparison**

**Table 6-1. Additive Jitter Comparison with Sine Wave 10MHz, 10dBm**

| Parameter | LMK1C110x | CDCLVP120x | COMP.LVCMOS | COMP.LVDS | Unit |
|---|---|---|---|---|---|
| Source RMS Jitter (10Hz - 1MHz) | 117.084 | 117.084 | 117.084 | 117.084 | fs |
| Total RMS Jitter (10Hz - 1MHz) | 150.321 | 457.152 | 210.055 | 271.11 | |
| Additive RMS Jitter (10Hz - 1MHz) | 94.274 | 441.904 | 174.397 | 244.524 | |
| Source RMS Jitter (10Hz - 1MHz) | 107.832 | 107.832 | 107.832 | 107.832 | |
| Total RMS Jitter (12kHz - 1MHz) | 145.478 | 452.119 | 204.935 | 266.091 | |
| Additive RMS Jitter (12kHz - 1MHz) | 97.653 | 439.071 | 174.271 | 243.263 | |

## 6.1 LMK1C110x Additive Noise vs Others

As described in Section 5.1 that noise measurement equipment can give optimistic results for additive phase noise results due to slew rate issue. An alternative cascaded setup is used to model the actual additive phase noise of LMK1C110x vs competition's best performing buffer. We use cascaded buffers and treat the first buffer as source. Phase noise setup for the buffer is shown in Figure 6-2

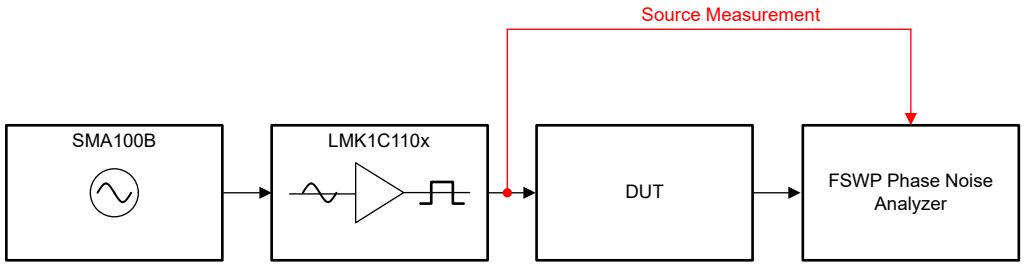



**Figure 6-2. Additive Noise Buffer Setup**

Following additive phase noise plots compare the performance of TI buffer vs competition.

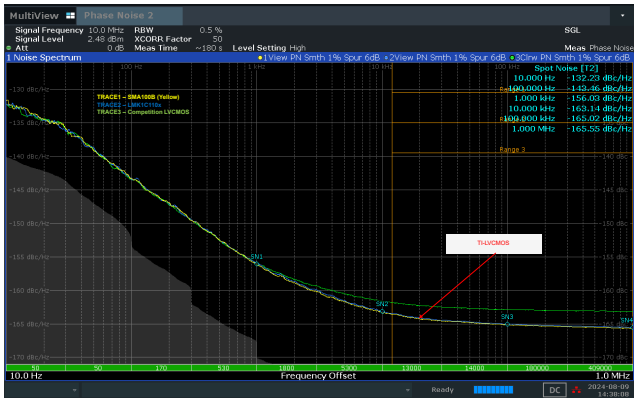
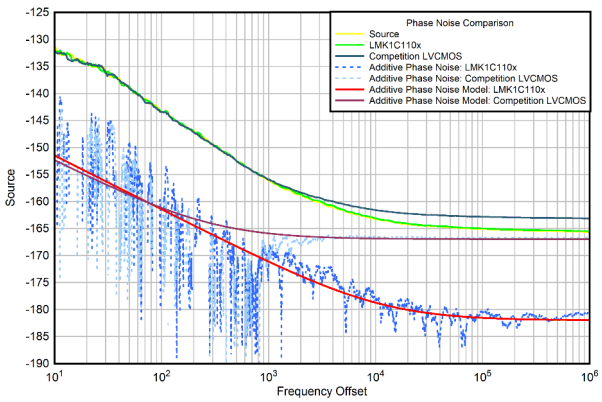


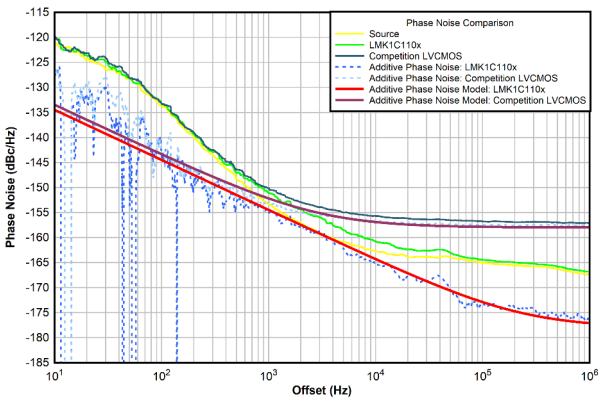

**Figure 6-3. Total Phase Noise at 10MHz Output**




Noise Floor = –181.9dBc/Hz, 1/f Noise = 178.5dBc/Hz at 10kHz

**Figure 6-4. Additive Phase Noise at 10MHz Output**


**Figure 6-5. Total Phase Noise at 100MHz Output**




Noise Floor = –177.9dBc/Hz, 1/f Noise = –164.3dBc/Hz at 10kHz

**Figure 6-6. Additive Phase Noise at 100MHz Output**


**Figure 6-7. RMS Jitter (12kHz - 1MHz): 10MHz Output - LMK1C110x vs Competition**


**Figure 6-8. RMS Jitter (10Hz - 1MHz): 12MHz Output - LMK1C110x vs Competition**


**Figure 6-9. RMS Jitter (12kHz - 20MHz): 100MHz Output - LMK1C110x vs Competition**


**Figure 6-10. RMS Jitter (10Hz - 50MHz): 100MHz Output - LMK1C110x vs Competition**

**Table 6-2. LMK1C110x Additive Jitter Comparison vs Competition**

| Parameter | LMK1C110x | | Competition LVCMOS | | Unit |
|---|---|---|---|---|---|
| Frequency | 10MHz | 100MHz | 10MHz | 100MHz | fs |
| Additive Jitter (10Hz - 1MHz) | 21.87 | - | 104.82 | - | |
| Additive Jitter (12kHz - 1MHz) | 21.39 | - | 104.41 | - | |
| Additive Jitter (12kHz - 20MHz) | - | 4.51 | - | 133.35 | |
| Additive Jitter (10Hz - 50MHz) | - | 16.38 | - | 200.90 | |

## 7 Summary

TI clock buffers helps reduce the overall phase noise impact due to slew rate sensitivity problem and provides comprehensive portfolio for all end application use case. Improved results using LMK1C110x shows that phase noise and jitter can be improved for low reference frequency sources (OCXO/TCXOs) in phase noise critical applications. This performance comparison for sine to square enables users to select the appropriate device for each use case to improve design margins in the system.

## 8 References

1. Texas Instruments, *LMK1C110x 1.8-V, 2.5-V, and 3.3-V LVCMOS Clock Buffer Family* , data sheet.
2. Texas Instruments, *LMK00301 3-GHz 10-Output Ultra-Low Additive Jitter Differential Clock Buffer and Level Translator* , data sheet.
3. Texas Instruments, *LMK1D120x Low Additive Jitter LVDS Buffer*, data sheet.
4. Texas Instruments, *CDCLVP1208 Eight LVPECL Output, High-Performance Clock 2:8 Buffer*, data sheet.

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