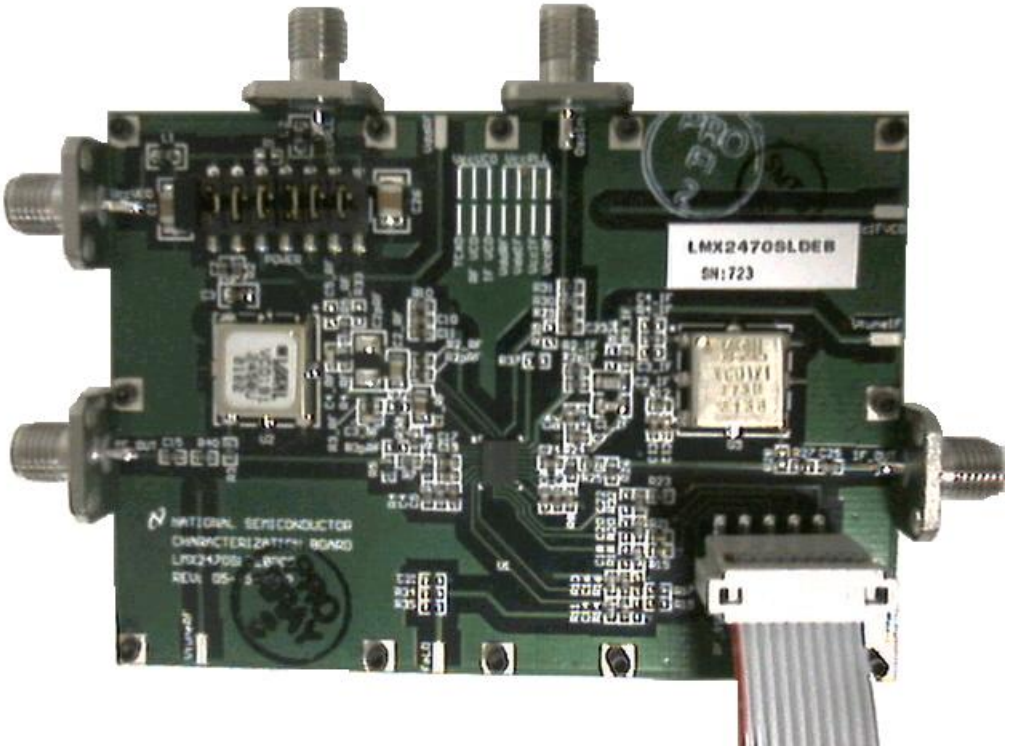
LMX2470SLE
Evaluation Board Operating Instructions



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LMX2470SLEFPEBI Rev 02.22.2004

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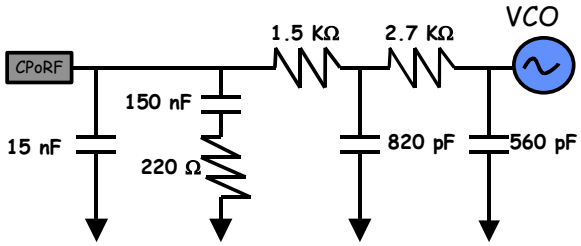
General Description

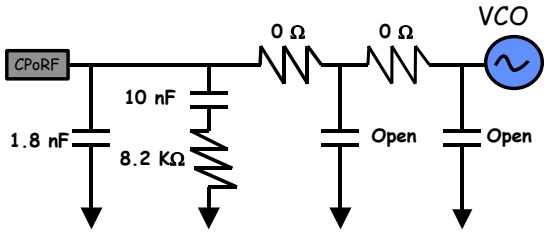
The LMX2470 Evaluation Board simplifies evaluation of the LMX2470 2.6 GHz/0.8 GHz ***PLLatinum™ dual frequency synthesizer***. The board enables all performance measurements with no additional support circuitry. The evaluation board consists of a LMX2470 device, a RF VCO module and IF VCO & RF/IF loop filters built by discrete components. The SMA flange mount connectors are provided for external reference input, RF and IF VCO outputs, and the power and grounding connection. A cable assembly is bundled with the evaluation board for connecting to a PC through the parallel printer port. By means of ***MICROWIRE™*** serial port emulation, the *CodeLoader* software included can be run on a PC to facilitate the LMX2470 internal register programming for the evaluation and measurement.

RF LOOP FILTER			
Theoretical (NOT Measured) Simulation (Done with EasyPLL at wireless.national.com)			
Phase Margin	39.1 deg	Pole Ratio T3 /T1	51.2 %
Loop Bandwidth	11.6 KHz	Pole Ratio T4/T3	31.1 %
Lock Time	2400 – 2480 MHz to 1 KHz tolerance in 249 uS w/o Fastlock	Spur Gain @ 200 KHz	-9.0 dB



Settings for Operation	
Kϕ	800 uA
Comparison Frequency	20 MHz
Output Frequency	2400 - 2480 MHz
PLL Supply	2.5 Volts
VCO Supply	3 Volts
Other Information	
VCO Used	VARIL2450U
VCO Gain	55 MHz/Volt
VCO Input Capacitance	22 pF

IF LOOP FILTER			
Theoretical (NOT Measured) Simulation (Done with EasyPLL at wireless.national.com)			
Phase Margin	47.1 deg	Lock Time	760 - 780 MHz MHz to 1 KHz tolerance in 453 uS
Loop Bandwidth	5.1 KHz	Spur Gain @ 200 KHz	22.1 dB



Settings for Operation	
Kϕ	1 mA
Comparison Frequency	200 kHz
Output Frequency	760 - 780 MHz
PLL Supply	2.5 Volts
VCO Supply	3 Volts
Other Information	
VCO Used	VARIL191-773U
VCO Gain	18 MHz/Volt
VCO Input Capacitance	100 pF

Setup and Measurement Procedures

The LMX2470 Evaluation Board is fully assembled and factory tested. Follow the instructions below to set up the hardware platform for the measurement of interest.

Recommended Test Equipment

- Spectrum analyzer (operating frequency range ≥ 2 GHz)
- Modulation domain analyzer
- DC power supply with adjustable voltage outputs
- 100 MHz signal source/generator or ultra-clean 10 MHz signal source. Actually, a 20 MHz (or 19.2, 19.68, or 19.8) MHz crystal can be used. If so, just disable the oscillator doubler bit ***OSC2X***.

Connection and Setup

1. Verify that seven jumper blocks are placed in the power header that is located on the upper left hand corner of the board and assigned the designator "POWER".
2. Connect the ***VccPLL*** power source to a 2.5 volt power supply. .
3. Connect the ***VccVCO*** power source to a 3.0 volt power supply. .
4. Connect the reference source to the SMA connector labeled ***OSCin.*** Plug the DB25 connector end of the cable assembly to the parallel port of the PC. Connect the other end of the cable to the on-board 5x2-pin header. Refer to the *Data cable configuration* section of the *Applications Information, CodeLoader Operation* for pin #1 position. Connect the ***RF_OUT***/***IF_OUT*** output port to the input of a spectrum analyzer for phase noise and reference spur measurement or the input of a modulation analyzer for lock time measurement.
5. Run the *CodeLoader* software on the PC for LMX2470 register programming. Refer to Appendices D and E for more details. Ensure proper port setup, and make sure that the frequency of the reference source on the CodeLoader matches that actually used for the board.
6. Verify that the CodeLoader software is properly programming the PLL by monitor the current going into the VccPLL pin. Power the RF PLL down and then back up again using the ***RF_PD*** bit. There should be a several mA change in the current.

Phase Noise Measurement Using A Spectrum Analyzer

1. Use the *CodeLoader* software to set the desired frequency and to program the LMX2470 device. Refer to Appendix E for more details.
2. Set the spectrum analyzer to the desired center frequency, and adjust the span so the appropriate offset frequency can be viewed.
3. Turn on the video-averaging feature of the analyzer for better determination of the noise level.
4. If using a spectrum analyzer, use the marker noise function. If the spectrum analyzer does not support this, then subtract 10●log(Resolution Bandwidth) from the measurement. Realize that this method does not account for the spectrum analyzer correction factor (typically ~ 2.5 db).
5. Note that these measurements are taken in the default setup.
6. For these measurements, the PLL not being used was powered down via microwire and the corresponding VCO power supply jumper was removed.

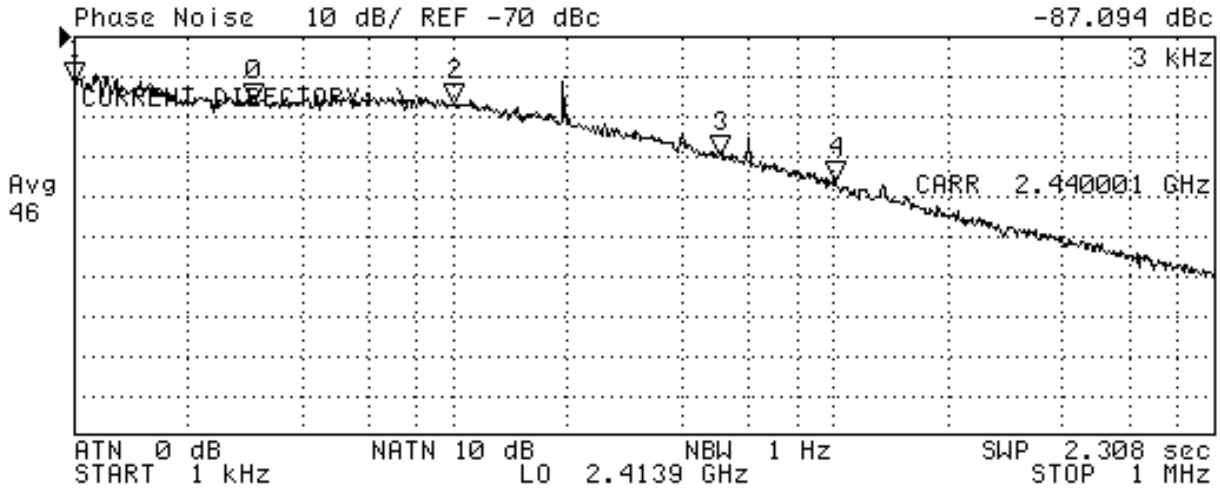
Reference Spur Measurement Using A Spectrum Analyzer

1. Use the *CodeLoader* software to set the desired frequency and to program the LMX2470 device. Refer to Appendix E for more details.
2. Set the spectrum analyzer to the desired center frequency, and set the span to allow the reference sidebands to be viewed. For example, the span can be set to 250 kHz during RF VCO measurement because its loop filter design is based on 100 kHz channel spacing.
3. The reference spur is the difference between the level of the VCO output frequency tone and the level of the reference spur (at the center frequency +/- the reference frequency).
4. Note that fractional spurs are dependent on voltage, fractional modulus, delta sigma modulator order, CPUD bit, and frequency. When measuring spurs, it is important to measure them at the lowest, middle, and highest frequency to get a realistic idea of the worst case. For these measurements, the PLL not being used was powered down via microwire and the corresponding VCO power supply jumper was removed.

Lock Time Measurement Using A Modulation Domain Analyzer

1. Decide the maximum and minimum frequency to be switched alternately. Enter ***Burst Mode*** menu of *CodeLoader* software to create a macro to program the LMX2470 to the maximum and minimum frequency alternately over time. It is necessary to put a sufficient delay between PLL programming (i.e. 100,000). Refer to the *Burst Mode configuration and operation* section of the *Application Information, CodeLoader Operation* for more details.
2. Set the slope of the trigger appropriately. For a positive lock time, choose a positive slope. For a negative lock time, choose a negative slope.
3. Set the trigger frequency just past the starting frequency. For instance, when measuring the lock time from 2400 to 2480 MHz, set the trigger at 2401 MHz.
4. Set the center frequency to the desired frequency and the span to 10 KHz.
5. Press ***[Start/Stop]*** button to capture the switching curve. Repeat this many times to get an idea of how much this measurement may vary. The graphs shown in this report are considered representative of the average lock time seen.
6. The lock time is the time difference between the point the frequency starts to change and the point that the PLL frequency settles within +/- 1 kHz range.

RF PLL Phase Noise



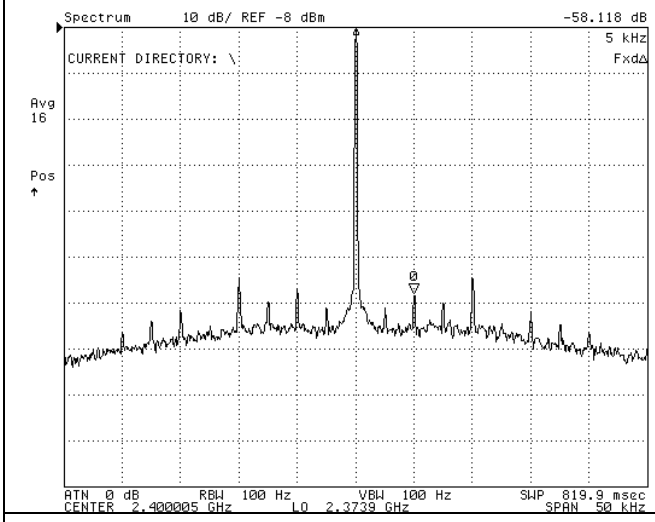
N	SWP PARAM	VAL
0	3 kHz	-87.094 dBc
1	1 kHz	-81.86 dBc
2	10 kHz	-87.412 dBc
3	50 kHz	-100.05 dBc
4	100 kHz	-106.87 dBc

- Close-in phase noise is –87.1 dBc/Hz.
- Phase noise at 100 KHz offset is –106.9 dBc/Hz.
- Note how the phase noise degrades at offsets less than 3 KHz. This may be partially due to the reference noise and measurement system. However, part of this is due to the part. If the comparison frequency is lowered, this effect is reduced.
- The loop bandwidth is about 10 KHz.
- The in-band phase noise can be improved by using a higher charge pump current setting, but the 800 uA setting was used so that higher current settings could be used for with fastlock/cycle slip reduction.
- The plot above was taken with an HP4352B phase noise system with the Agilent E4426B signal generator. The reference source was a Wetzel 10 MHz crystal with +12 dBm output.
- The phase noise system accounts for correction factors, which makes the measurement appear about 2.5 dB worse than not accounting for this factor.

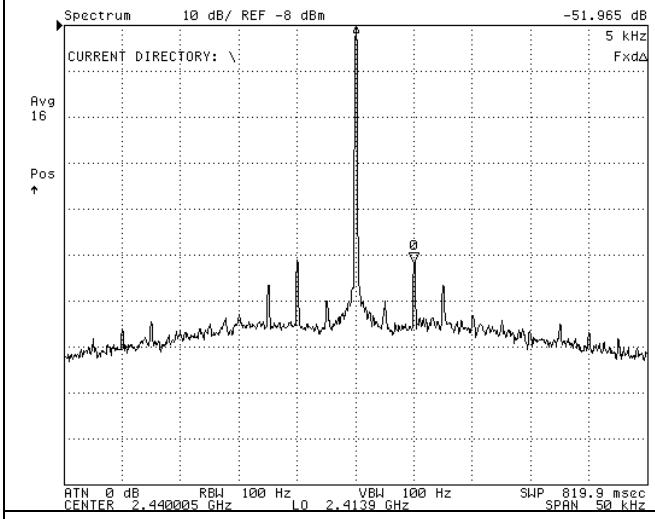
RF PLL In-Band Fractional Spurs

In-band fractional spurs are a good metric to qualify fractional spurs because they are practically indepenRF_FDt of the loop filter used, provided that they are inside the loop bandwidth. The worst case is when the fractional numerator is one. If a different fractional numerator is used, these spurs could be considerably better, or not even present. The worst case in-band spur is the most relevant number.

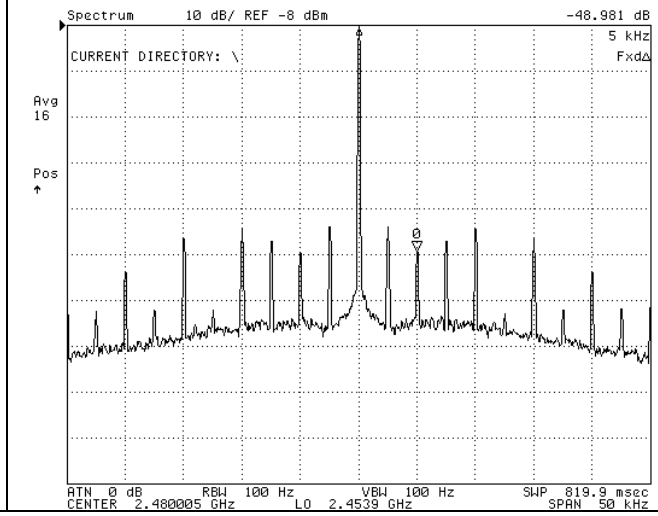
RF_FN = 1
FRF_FD = 4000
Spur Offset Frequency = 5 KHz



In-band fractional spur at 2400.005 MHz is –58.1 dBc.



In-band fractional spur at 2440.005 MHz is –52.0 dBc.



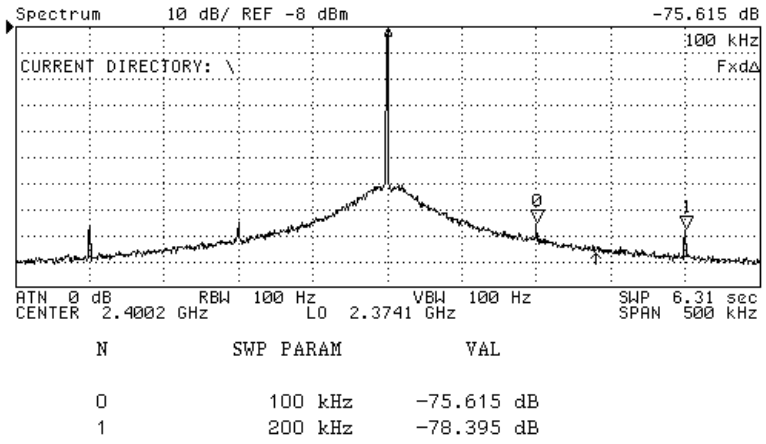
In-band fractional spur at 2480.005 MHz is –49.0 dBc. This is the worst case fractional spur.

Note the sub-fractional spurs at 2.5 KHz. Decreasing the FM Bit (Sigma Delta Order) makes these spurs completely disappear, but increases the spur at 5 KHz. These spurs are also impacted by the CPUD bit.

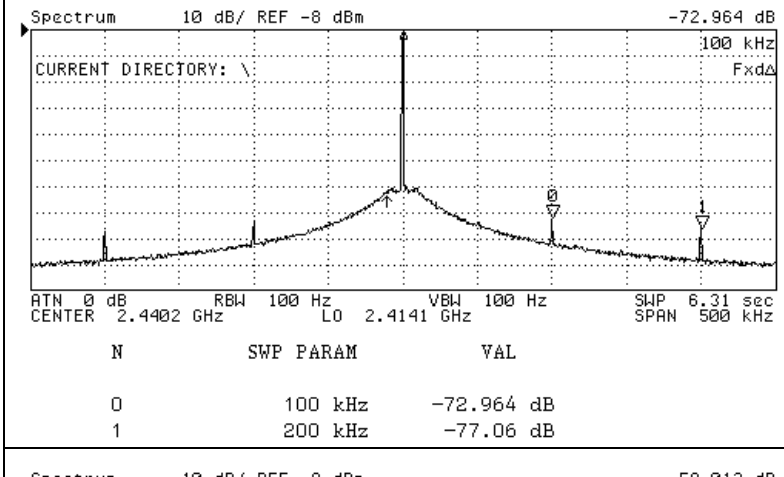
RF PLL Fractional Spurs

These spurs are impacted by the FM (Sigma Delta Order) and CPUD (Charge Pump User Definition) bits. There are 9 valid combinations that can be used. The combination used here is considered a good trade-off with FM = 3rd Order Sigma Delta PLL and CPUD = Maximum. By tinkering with the FM and CPUD bits, it is possible to find the desired trade-off between sub-fractional spur levels and lowest first fractional spur at 200 KHz.

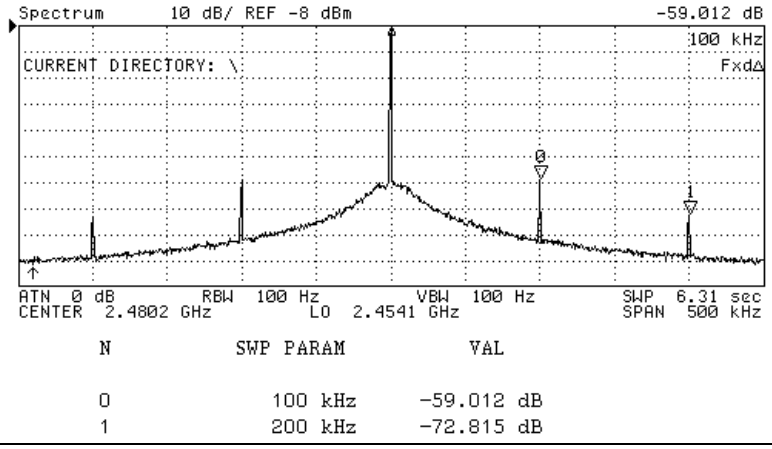
RF_FN = 1
FRF_FD = 100
Spur Offset Frequency = 200 KHz



First fractional spur at 200 KHz offset is –78.4 dBc. Note that the is also a sub-fractional spur at 100 KHz of –75.6 dBc.



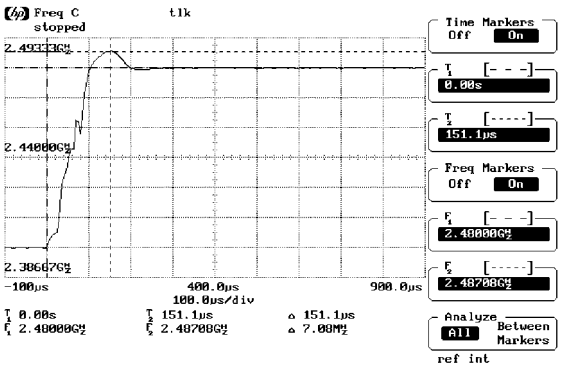
First fractional spur at 200 KHz offset is –77.1 dBc. Note that the is also a sub-fractional spur at 100 KHz of –73.0 dBc.



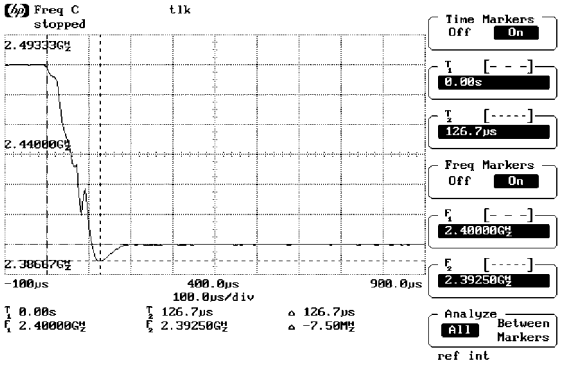
First fractional spur at 200 KHz offset is –72.8 dBc. Note that the is also a sub-fractional spur at 100 KHz of –59.0 dBc. This is the worst case for both the sub-fractional spur and the fractional spur.

RF PLL Lock Time

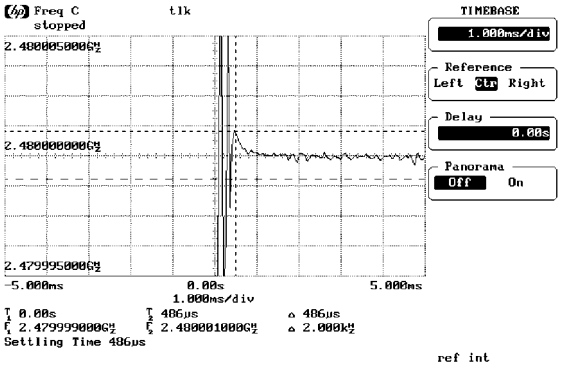
RF_TOC=700
PDCP = X2 Fastlock
RF_CPF=1600 uA



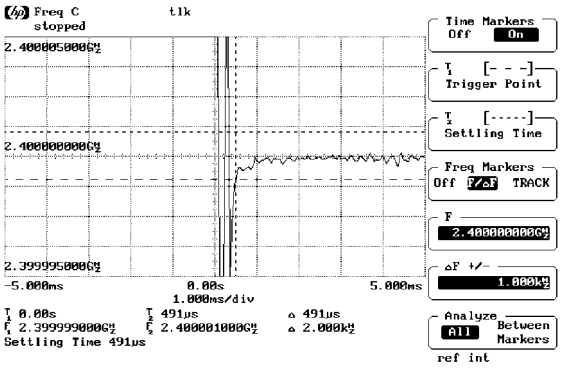
Positive peak time is 151 uS. Note the cycle slip. The frequency overshoot is 7.1 MHz.



Negative peak time is 127 uS. Note the cycle slipping. The negative undershoot is –7.5 MHz.

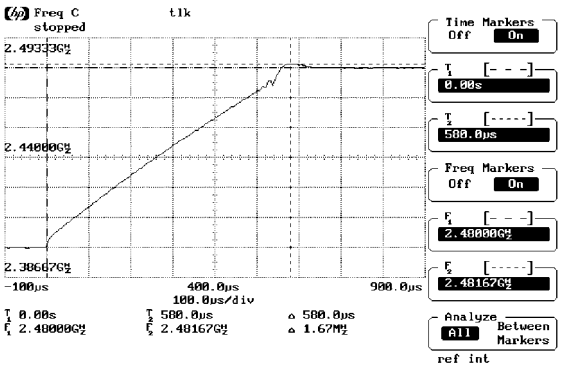
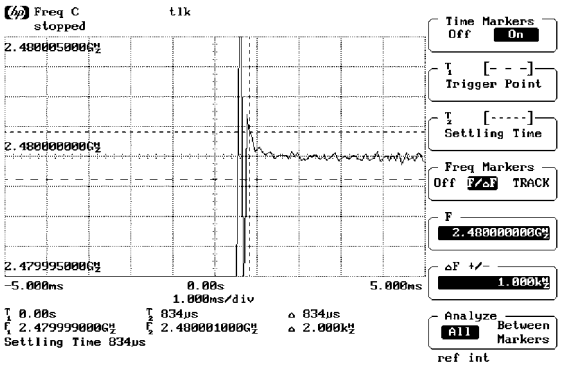
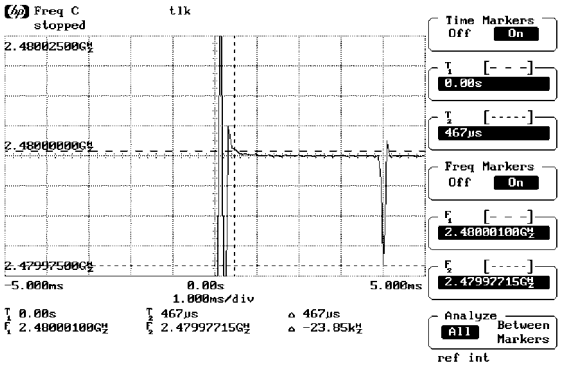
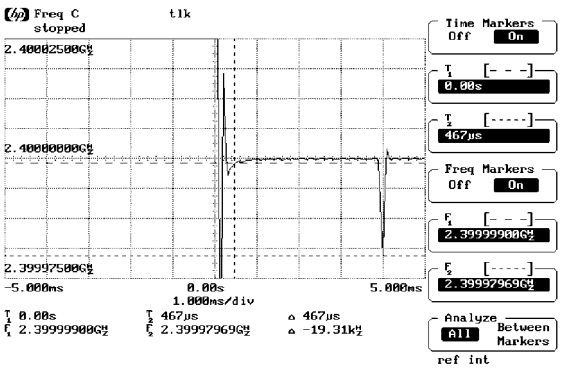


Positive lock time from 2400 to 2480 MHz to a 1 KHz tolerance is 486 uS.

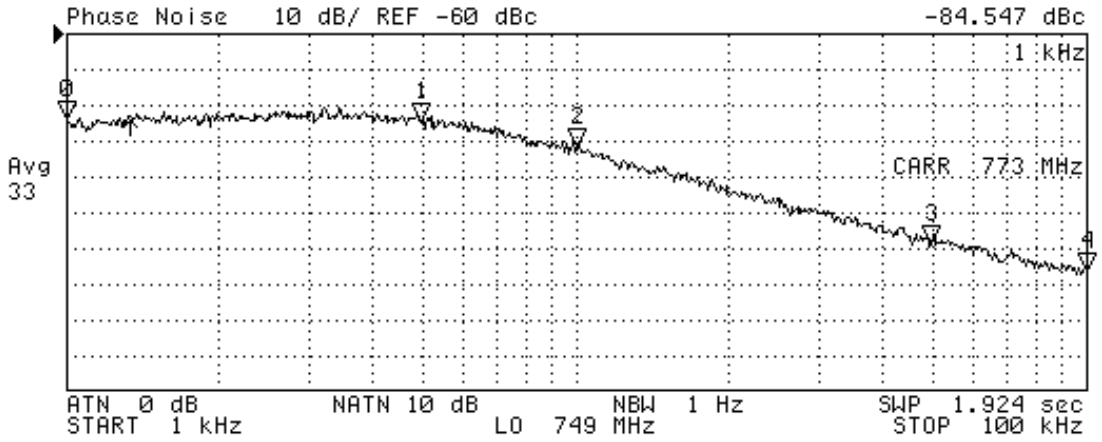


Negative lock time from 2480 to 2400 MHz to a 1 KHz tolerance is 491 uS.

RF PLL Lock Time Attributes

RF_TOC = 0 PDCP = X2 Fastlock RF_CPF=1600uA		The peak time without using fastlock is a whopping 561 uS due to excessive cycle slipping. Note that the overshoot is only 1.8 MHz. This is due to distortion caused by the cycle slipping. Recall from the previous page that the cycle slip reduction circuitry reduces this peak time by 489 uS.
		Positive lock time from 2400 to 2480 MHz to 1 KHz tolerance is 834 uS. Note that this is 348 uS longer than when fastlock was used. The above picture shows that the peak time was increased by 410 uS. So most of the increase in lock time is a result of increased peak time due to excessive cycle slipping.
RF_TOC = 10000 PDCP = X2 Fastlock RF_CPF=1600uA		Lock time from 2400 to 2480 MHz to 1 KHz tolerance with fastlock engaged all the time is 467 uS. The fastlock disengagement glitch is about 23 KHz.
		Lock time from 2480 to 2400 MHz to 1 KHz tolerance with fastlock engaged all the time is 467 uS. The fastlock disengagement glitch is about 20 KHz.

IF PLL Phase Noise and Loop Bandwidth

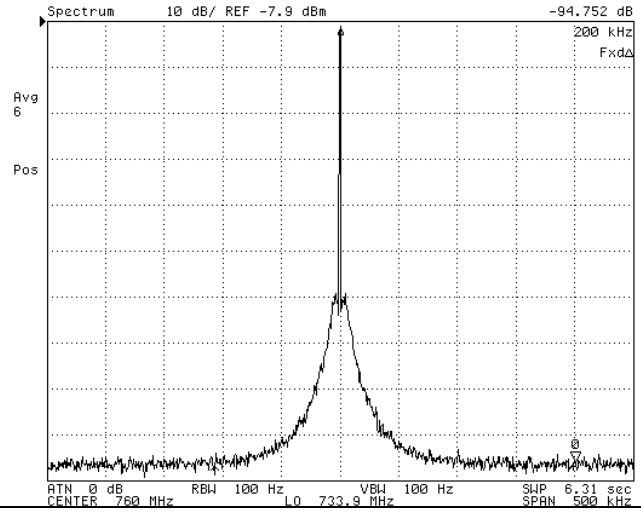


N	SWP PARAM	VAL
0	1 kHz	−84.547 dBc
1	5 kHz	−84.62 dBc
2	10 kHz	−91.725 dBc
3	50 kHz	−119.16 dBc
4	100 kHz	−127.14 dBc

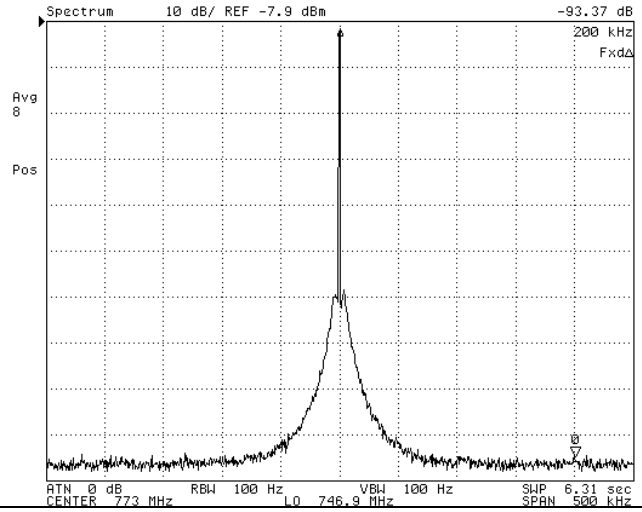
- The plot above shows close in phase noise of –84.6 dBc/Hz.
- Phase noise at 100 KHz offset is –127 dBc/Hz
- The loop bandwidth is about 5 KHz.
- The in-band phase noise can be improved by about 1 dB by using a higher charge pump current setting, but the 1 mA setting was used so that the higher current setting could be used for fastlock.
- The plot above was taken with an HP4352B phase noise system with the Agilent E4426B signal generator. The reference source was a Wetzel 10 MHz crystal with +12 dBm output.
- The phase noise system accounts for correction factors, which makes the measurement appear about 2.5 dB worse than not accounting for this factor.

IF PLL Reference Spurs

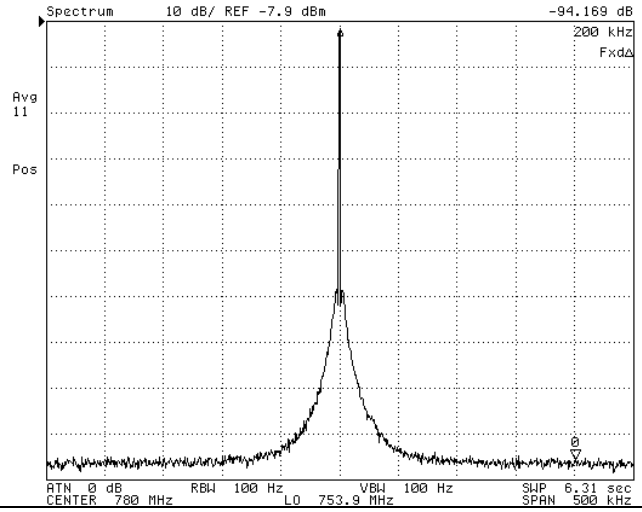
Note that the noise floor on the measurement device was –95 dBc, and all the spurs are below this noise floor. The LMX2470 IF PLL spurs are approximately 20 dB better than the LMX2330L family. Note that these measurements were taken with the RF PLL powered down. If the RF PLL is powered up, there could be some larger spurs at 200 KHz.



Spurs at 760 MHz are too low to measure.



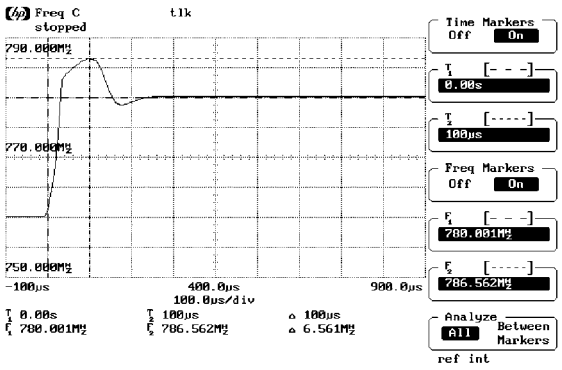
Spurs at 773 MHz are too low to measure.



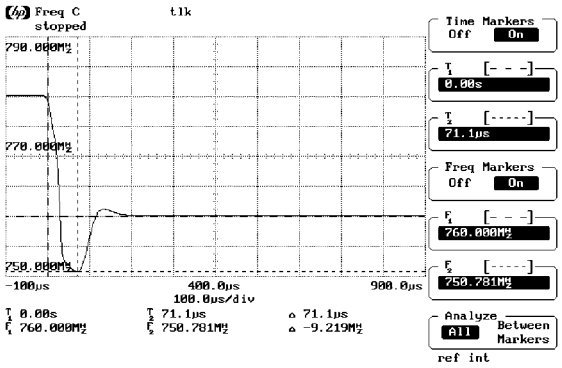
Spurs at 780 MHz are too low to measure.

IF PLL Lock Time

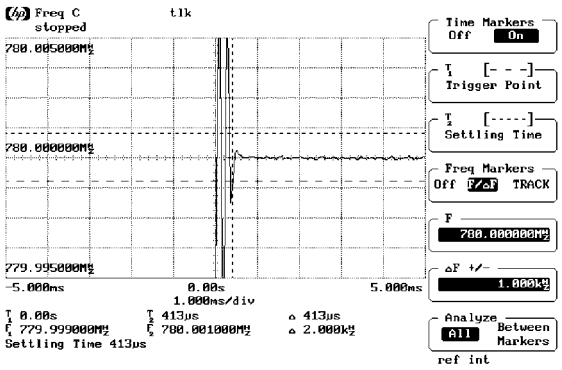
IF_TOC = 500



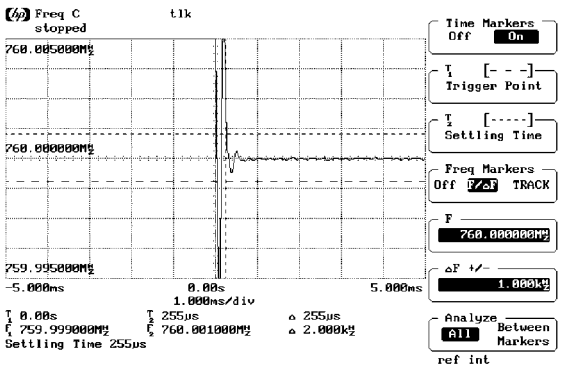
Positive peak time is 100 uS. The frequency overshoot is 6.6 MHz.



Negative peak time is 71 uS. The negative undershoot is –9.2 MHz.

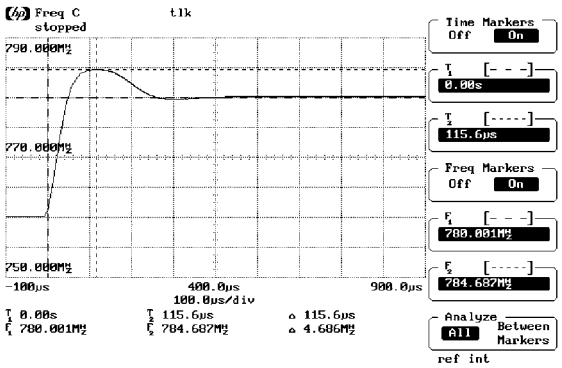
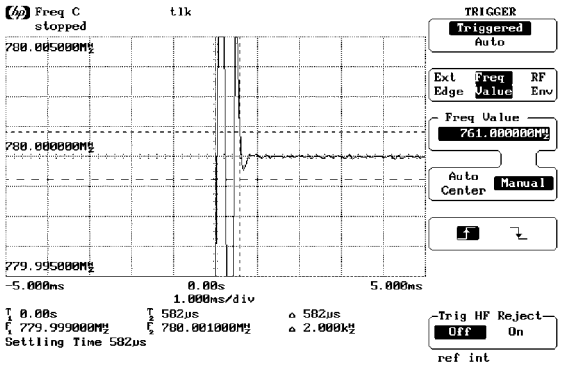
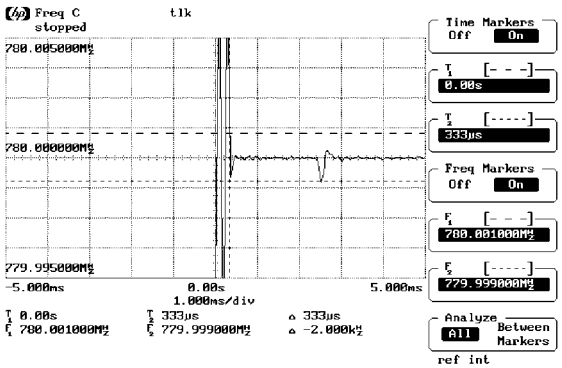
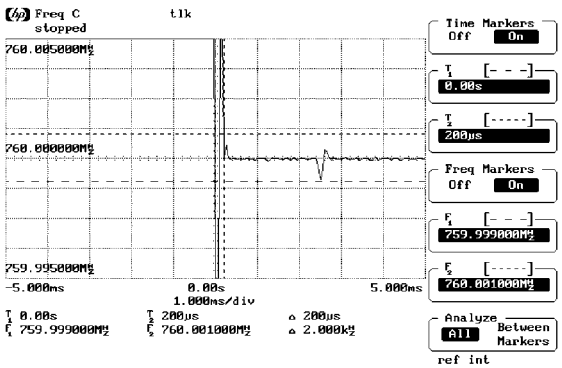


Positive lock time from 760 to 780 MHz to a 1 KHz tolerance is 413 uS.

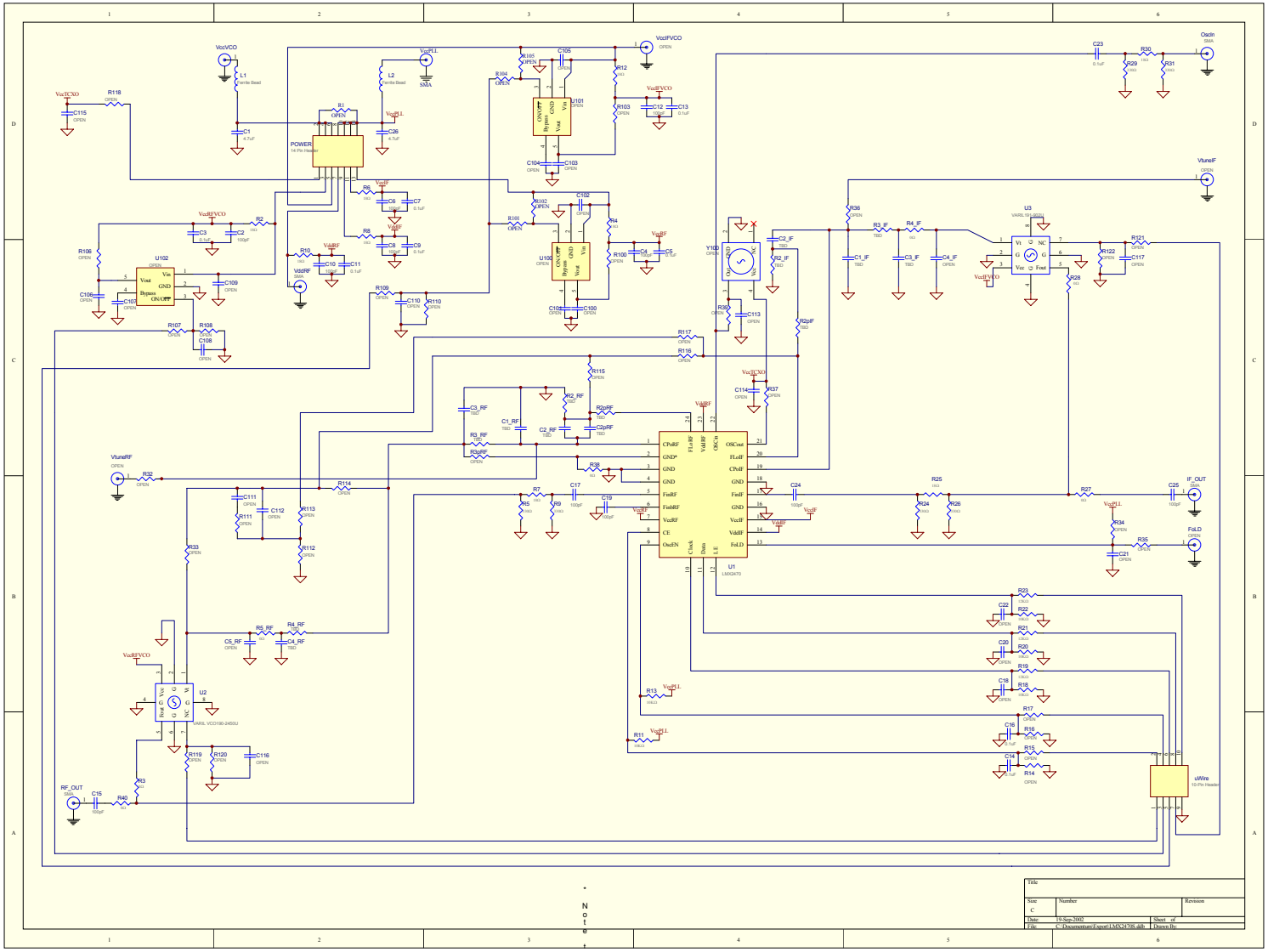


Negative lock time from 780 to 760 MHz to a 1 KHz tolerance is 255 uS.

IF PLL Lock Time Attributes

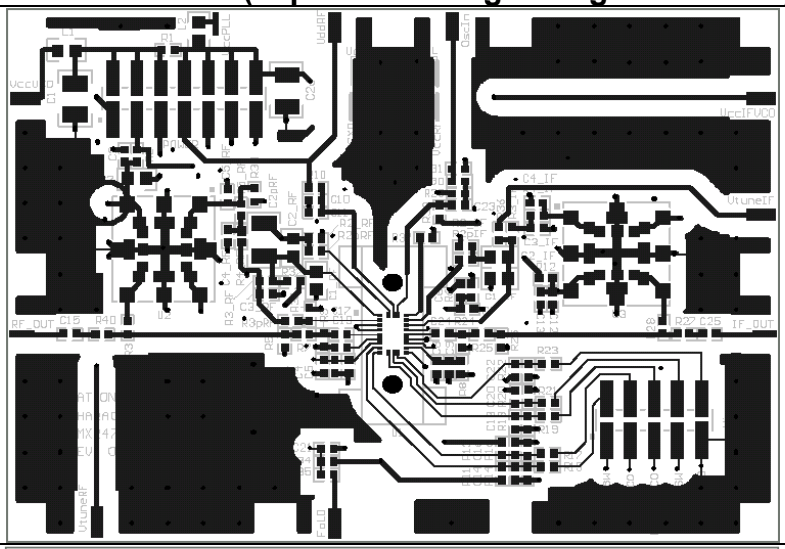
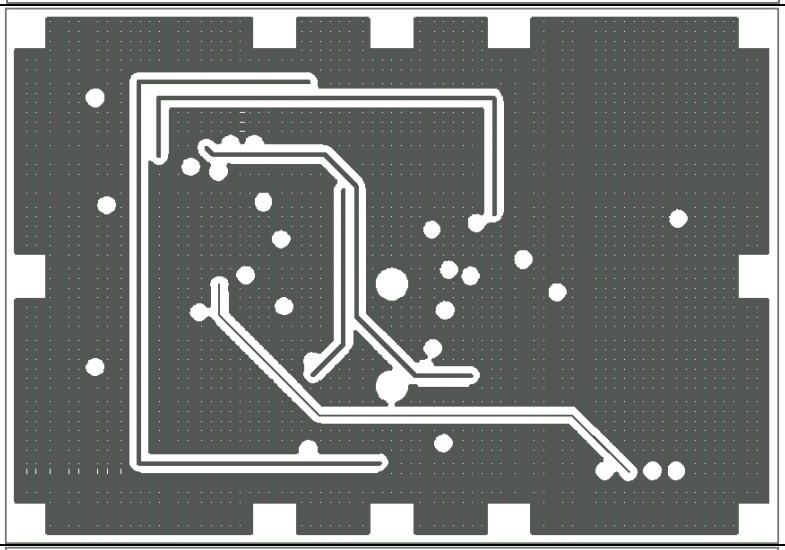
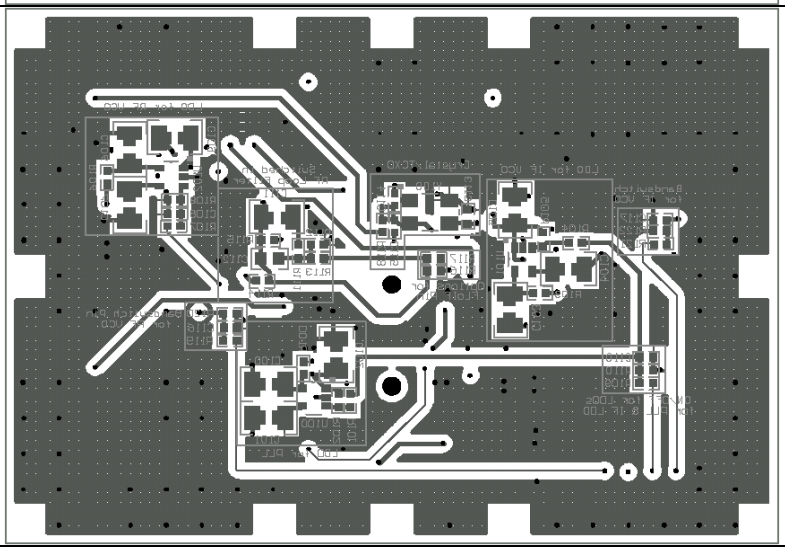
IF_TOC = 0		The peak time without using fastlock is a whopping 116 uS. The overshoot is 4.7 MHz.
		Positive lock time from 760 to 780 MHz to 1 KHz tolerance is 582 uS.
IF_TOC = 500		Lock time from 760 to 780 MHz to 1 KHz tolerance with fastlock engaged all the time is 333 uS. The fastlock disengagement glitch is about 1 KHz.
		Lock time from 780 to 760 MHz to 1 KHz tolerance with fastlock engaged all the time is 200 uS. The fastlock disengagement glitch is about 1 KHz.

Appendix A – LMX2470 Evaluation Board Schematic Diagram



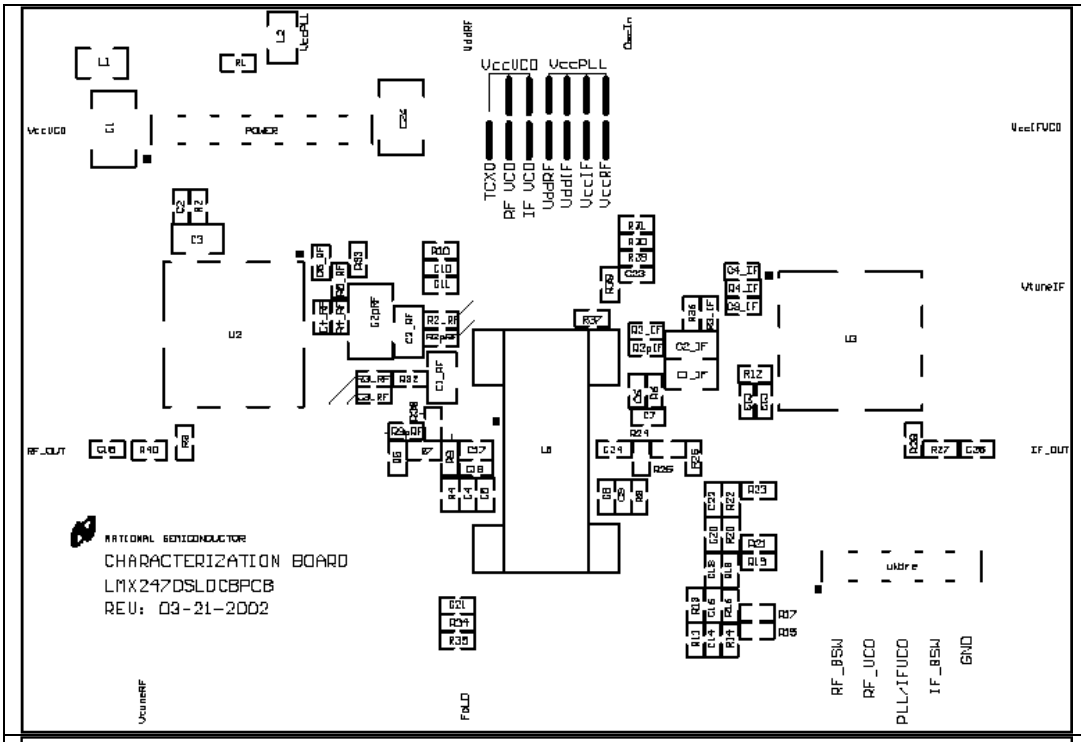
Appendix B – LMX2470 Evaluation Board Layout

(top view looking through the board)

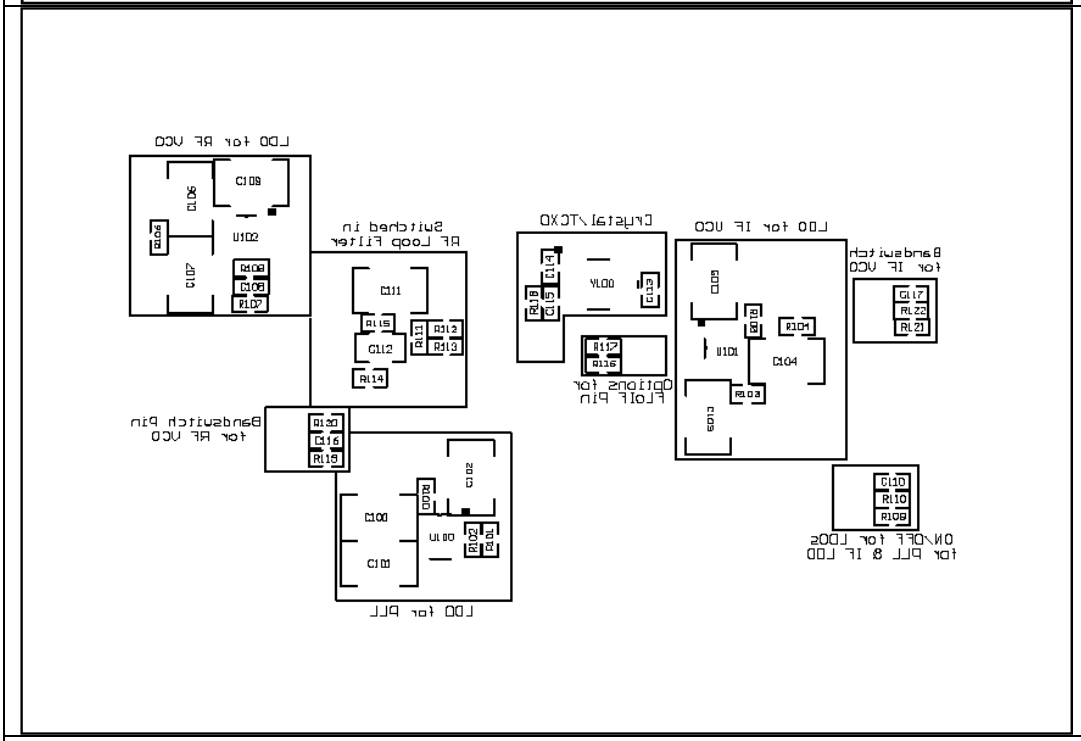
	**TOP LAYER and Silkscreen**
	**MID LAYER 2** (Mid Layer 1 is Ground and is 10 mils below the top layer)
	**BOTTOM LAYER and SILKSCREEN**

Appendix C – LMX2470 Build Diagram

(As seen top view through the board)



TOP LAYER



BOTTOM LAYER

(Note that in the default configuration, no components on the bottom layer should be stuffed. They are included for added features and functionality)

This board is 4 layer board comprised of FR4 material. Mid Layer 1 is not shown, but is a ground plane that is 10 mils below the top layer. The distance between Mid Layer 1 and Mid Layer 2, and Mid Layer 2 and the bottom layer is not critical, but the total thickness off the board should be 31 mils. Note that 1 mil = 1/1000 of an inch.

Additional Information

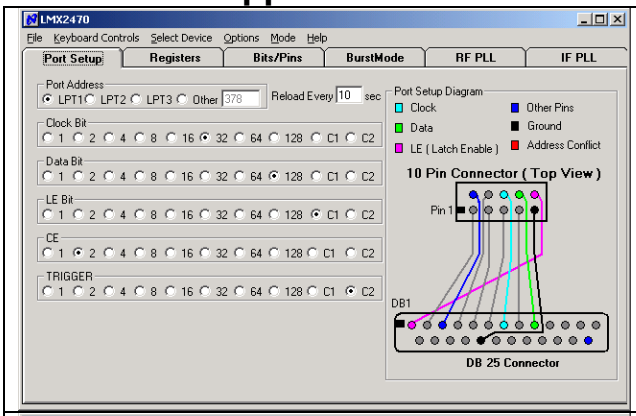
Appendix D –Bill of Materials

Assembly	LMX2470SLDEB
Revision	2.1
Last Updated	10/18/2002

Item	Qty.	Manufacturer	Part#	Part Type	Part Footprint	Material	Designator
0	n/a	OPEN	OPEN	• C18, C20, C21, C22, C2_RF, C3_IF, C4_IF, C5_RF • R1, R2pRF, R14, R15, R16, R17, R32, R33, R34, R35, R36, R37, R39, R3pRF • FoLD, VccIFVCO, VddRF, VtuneIF, VtuneRF, • Any component with designator 100 or higher is open and on the bottom layer.			
1	1	COMM CON CONNECTORS	HTSM3203-10G2	10 Pin Header	HEADER_2X5	PLASTIC	uWire
2	1	COMM CON CONNECTORS	HTSM3203-14G2	14 Pin Header	HEADER_2X7	PLASTIC	POWER
3	7	COMM CON CONNECTORS	CCIJ255G	SHUNT, Single, 0.1", Closed Top	N/A	PLASTIC	Place across the following pins of the POWER (1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14)
4	5	CDI	5762SF	SMA	SMA(30X125MIL)	METAL	IF_OUT, RF_OUT, OscIn, VccPLL, VccVCO
5	1	LUX MANUFACTURING	225325GTSP	LARGE FRAME	LARGE FRAME	METAL	MECHANICAL
6	12	ORLANDER, INC	OF12SHCA	FRAME SCREWS	SCREWS	METAL	MECHANICAL
7	10	ORLANDER, INC	2C18PPMZZ	SMA SCREWS	SCREWS	METAL	MECHANICAL
8	1	NATIONAL SEMICONDUCTOR	LMX2470	LMX2470	CSP24	SILICON	U1 (Match Dot on Part with Dot on Board)
9	1	NATIONAL SEMICONDUCTOR	LMX2470SLDEBPCB	PCB Board	n/a	FR4	n/a
10	1	VARIL	VCO191-773U	VCO	VARIL U	CAN	U3 (Match Dot on VCO with Dot on Board)
11	1	VARIL	VCO191-2450U	VCO	VARIL U	CAN	U2 (Match Dot on VCO with Dot on Board)
12	2	STEWARD	LI0603D301R-00	Ferrite Bead	603	FERRITE	L1, L2
13	11	KEMET	C0603C101J5GAC	100pF	0603	NPO	C2, C4, C6, C8, C10, C12, C15, C17, C19, C24, C25
14	1	KEMET	C0603C561CJ3GAC	560pF	0603	NP0	C4_RF
15	1	KEMET	C0603C821CJ3GAC	820pF	0603	NP0	C3_RF
16	1	KEMET	C0805C182CJ3GAC	1.8nF	0805	NP0	C1_IF
17	1	PANASONIC	ECHU1C103JB5	10nF	0805	FILM	C2_IF
18	1	PANASONIC	ECHU1C153JB5	15nF	0805	FILM	C1_RF
19	9	KEMET	C0603C104K3RAC	100nF	0603	X7R	C3, C5, C7, C9, C11, C13, C14, C16, C23
20	1	PANASONIC	ECHU1C154MA5	150nF	1210	FILM	C2pRF
21	2	KEMET	C1210C475K8RAC	4.7uF	1210	X7R	C1, C26
22	8	VISHAY	CRCW0603000ZRT1	0 Ω	0603	CERAMIC	R3, R3_IF, R4_IF, R5_RF, R27, R28, R38, R40
23	9	VISHAY	CRCW0603180JRT1	18 Ω	0603	CERAMIC	R2, R4, R6, R7, R8, R10, R12, R25, R30
24	1	VISHAY	CRCW0603221JRT1	220 Ω	0603	CERAMIC	R2_RF
25	6	VISHAY	CRCW0603331JRT1	330 Ω	0603	CERAMIC	R5, R9, R24, R26, R29, R31
26	1	VISHAY	CRCW0603152JRT1	1.5 KΩ	0603	CERAMIC	R3_RF
27	1	VISHAY	CRCW0603272JRT1	2.7 KΩ	0603	CERAMIC	R4_RF
28	1	VISHAY	CRCW0603822JRT1	8.2 KΩ	0603	CERAMIC	R2_IF, R2pIF
29	5	VISHAY	CRCW0603103JRT1	10 KΩ	0603	CERAMIC	R11, R13, R18, R20, R22
30	3	VISHAY	CRCW0603123JRT1	12 KΩ	0603	CERAMIC	R19, R21, R23

The loop filter components C1_RF, C2_RF, and C2_IF that were used to take the information had a FILM dielectric. However, X7R capacitors were substituted and no noticeable degradation in performance was observed, so it is acceptable to substitute X7R components for these components.

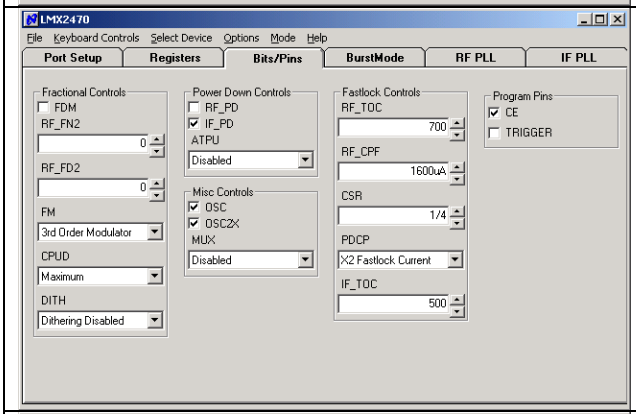
Appendix E – How To Setup CodeLoader Software



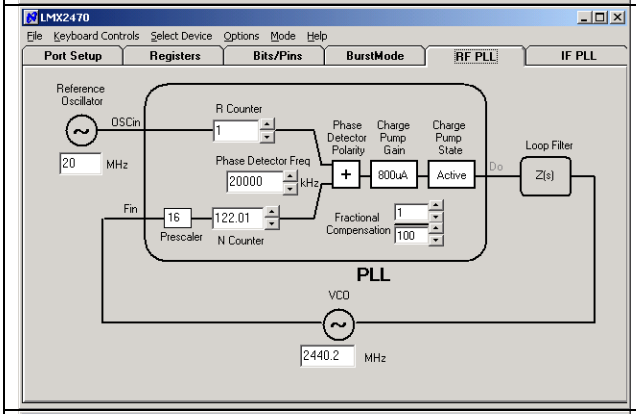
This shows the proper port setup. The port setup is:

Clock: 32
Data: 128
LE: C1
RFEn: 2
IFEn: 4
Trigger: C2

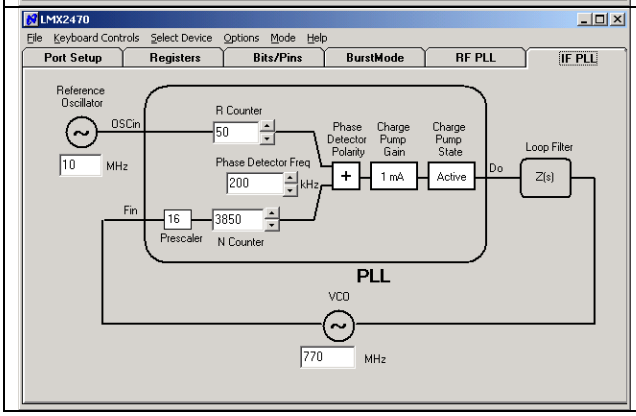
For most desktop computers, the parallel port is LPT1, but LPT3 is common for many laptop computers. CodeLoader does not autodetect the correct port.



This shows the proper bits/pins setup. At this time, not all the best known modes are shown. The CE pin is normally enabled to power up the evaluation board, but this evaluation board has a pull-up resistor, so this pin has no impact.



Note that although a 10 MHz reference source is used, this should be treated as 20 MHz on the RF PLL side because the oscillator doubler is used. Ensure that the 16 prescaler is used for the best performance.



The oscillator doubler only doubles the frequency for the RF PLL, so on the IF PLL, the reference source frequency is 10 MHz.

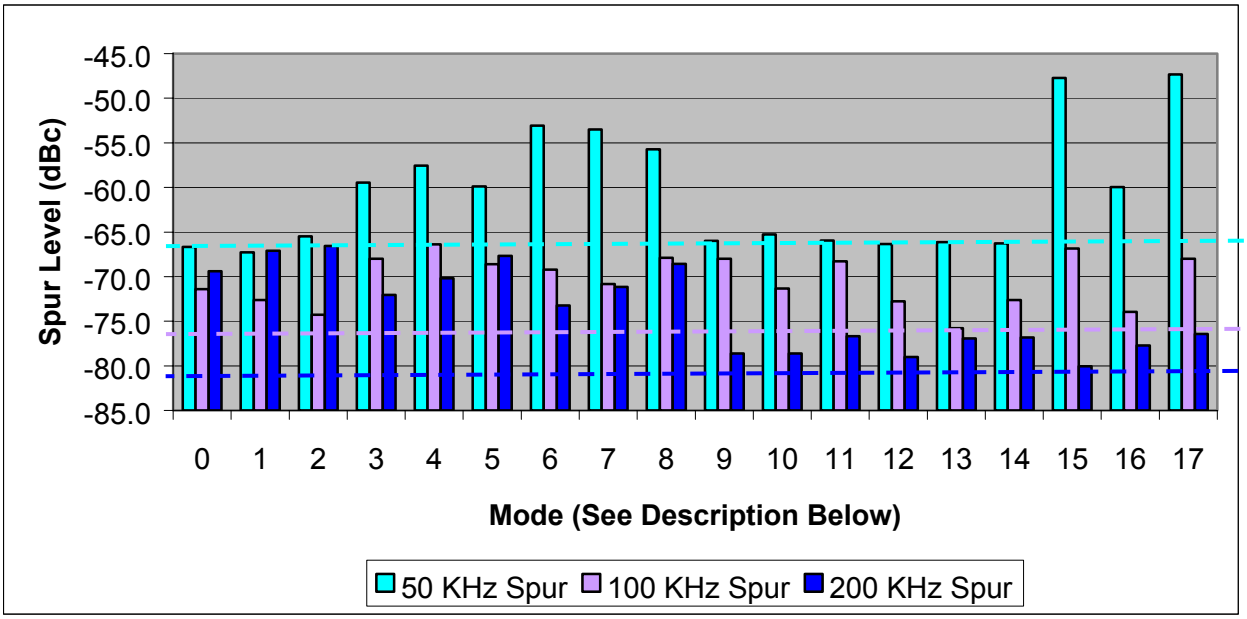
Appendix F – Tinkering with the CPUD and FM Modes

The CPUD and FM bits have a large impact on fractional spurs. They do have some impact on phase noise, but this impact is on the order of 1 dB or less. For this evaluation board, there are three types of fractional spurs. The main fractional spur is at 200 KHz offset. Fractional spurs that occur at frequency offsets that are either one-half or one-fourth of the channel spacing will be referred to as sub-fractional spurs. There may be a sub-fractional spur at 100 KHz, and if the fourth order modulator is used, then there may also be a sub fractional spur at 50 KHz as well. There are trade-offs between the main fractional spur level and main fractional spur level. Also, the sub-fractional spurs are sensitive to the power level of the reference input. In order to best show the impact of these bits, the worst case spurs from 2400.2 MHz, 2440.2 MHz, and 2480.2 MHz were measured. Various bits were changed to make 17 different modes. When the comparison frequency was 10 MHz, the charge pump gain was increased to 1600 uA to maintain the same loop bandwidth.

				50 KHz Spur (dBc)		100 KHz Spur (dBc)		200 KHz Spur (dBc)	
Mode	**OSC2X**	**FM**	**CPUD**	**Avg.**	**Stdev.**	**Avg.**	**Stdev.**	**Avg.**	**Stdev.**
0	0	2nd	Minimum	-66.7	1.3	-71.4	4.2	-69.4	5.4
1	0	2nd	Maximum	-67.3	0.3	-72.6	3.5	-67.1	0.9
2	0	2nd	Nominal	-65.5	0.7	-74.3	5.0	-66.6	4.3
3	0	3rd	Minimum	-59.4	7.7	-68.0	3.6	-72.1	3.1
4	0	3rd	Maximum	-57.6	7.6	-66.4	3.8	-70.2	1.5
5	0	3rd	Nominal	-59.9	7.4	-68.6	3.8	-67.7	3.3
6	0	4th	Minimum	-53.1	5.4	-69.2	1.6	-73.2	1.9
7	0	4th	Maximum	-53.5	3.0	-70.8	2.0	-71.2	1.7
8	0	4th	Nominal	-55.7	7.0	-67.9	3.3	-68.6	2.2
9	1	2nd	Minimum	-66.0	3.6	-68.0	2.7	-78.6	0.9
10	1	2nd	Maximum	-65.3	2.2	-71.3	1.7	-78.6	1.1
11	1	2nd	Nominal	-65.9	0.3	-68.3	2.6	-76.7	2.2
12	**1**	**3rd**	**Minimum**	**-66.3**	**0.4**	**-72.8**	**0.8**	**-79.0**	**2.8**
13	**1**	**3rd**	**Maximum**	**-66.1**	**1.8**	**-75.8**	**2.0**	**-76.9**	**1.9**
14	1	3rd	Nominal	-66.3	2.1	-72.6	2.0	-76.8	5.1
15	**1**	**4th**	**Minimum**	**-47.7**	**2.8**	**-66.8**	**3.3**	**-80.1**	**2.1**
16	1	4th	Maximum	-59.9	3.8	-73.9	0.1	-77.7	1.5
17	1	4th	Nominal	-47.3	1.9	-68.0	4.5	-76.4	3.6

The reference source was the 10 MHz out of the back of a HP8563E spectrum analyzer. This source was about 0 dBm. There is also a 3 dB pad on the board. When the OSC2X bit was one, the comparison frequency was 20 MHz, otherwise it was 10 MHz. The following trends can be seen with these different modes:

- For all modes, the main fractional spur at 200 KHz looks lower with the 20 MHz comparison frequency than with a 10 MHz comparison frequency.
- The 1/4th sub fractional spur at 50 KHz offset is only present when the 4th order modulator was used
- The data in the front of this document was originally taken with mode 13, but the table suggests that using mode 12 reduces the 200 KHz spur at the expense of the 100 KHz spur. Using mode 15 creates large spurs at 50 KHz, but reduces the main fractional spur at 200 KHz. It is impossible to say that one mode is the best for every application and circumstance, but there are certainly modes that are better than others. Modes 12, 13, and 15 seem to be optimal, depending on how optimal spur performance is defined.

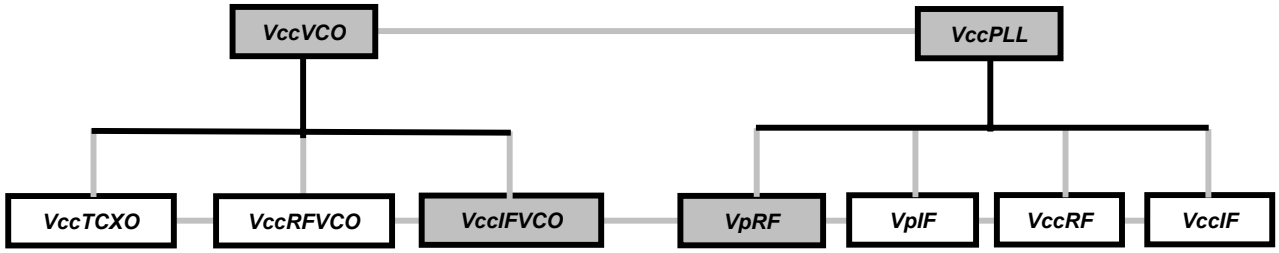


The chart above is just a visual representation of the table on the previous page. The turquoise, purple, and blue dotted lines on the graph indicate the noise floor of the spectrum analyzer at 50 KHz, 100 KHz, and 200 KHz, respectively.

Appendix G – Additional Features of the LMX2470 Evaluation Board

POWER MANAGEMENT

The power management strategy on this board allows one to run the board off any combination of power supplies. The resistor R1 connects VccVCO with VccPLL. The gray lines represent optional connections that can be made. One important thing to understand is that the jumpers may be placed horizontally as well as vertically, allowing more flexibility. The squares that are gray in color have an SMA connector routed to them.



Name	Function
VccVCO	Power Supplies for the TCXO, RF VCO, and IF VCO
VccTCXO	Power supply for the TCXO
VccRFVCO	Power supply for the RF VCO. Note that there is an option to send this through an LDO.
VpRF	Power supply for the VpRF pin of the PLL Note that for normal operation, VpRF = VpIF
VpIF	Power supply for the VpIF pin of the PLL. Note that for normal operation, VpRF = VpIF
VccIFVCO	Power supply for the IF VCO. Note that there is an option to send this through an LDO.
VccRF	Power supply for the VccRF pin of the PLL. Note that for normal operation, VccRF = VccIF
VccIF	Power supply for the VccIF pin of the PLL. Note that for normal operation, VccRF = VccIF

MICROWIRE

In the default setup, the 10K/39K voltage divider divides 5 volts to 4 volts. Now the reason it doesn't go to 3 volts is that if the PC has a 3 volt output as a few do, then it gets 2.4 volts. If the user is at 3.0 volts Vcc for the rest of the board, it is still within specifications. Note also the capacitors. On DC lines, the ESR of the 1uF capacitor is not critical because it is next to 10KΩ resistor. This should significantly reduce any noise coming the microwire on these traces. On CLOCK, DATA, and LE, there is only 10 pF, since these carry AC signals. The pull-up on the RF_EN and IF_EN is to VCCmain, so it does not disrupt current measurements into the VccPLL pin. So it should be clear that if the Pull-up resistor is in the board, and the PLL is powered down, then there will be a voltage across these pull-up resistors which will increase the current consumption of the board. The microwire can also turn off the RF and IF LDOs and be used for bandswitch functions on the VCOs.

PART NUMBERING SCHEME

The part designators are assigned such that all the components on the bottom layer have a designator of 100 or higher, and all the components on the top layer are less than 100. In the default configuration, no components on the bottom layer should be included. All components on the bottom layer are to support additional features.

HYBRID VCO FOOTPRINT

Although the evaluation board is created to support a particular VCO, the footprint is flexible and designed such that other VCOs are easy to put on the board. To mount a smaller VCO on the board, scratch off the soder mask with the flat edge of a screwdriver and then put solder on the pads such that it covers the exposed copper.

MULTI-FASTLOCK SUPPORT

In addition to supporting traditional fastlock, this board supports switching in two resistors. This is more there for testing purposes. For both the RF and IF loop filters, it is possible to switch in up to 3 possible combinations of resistors. For instance, on the RF loop filter, if one makes R40 0 ohm and R2_IF open, then one can switch in R2_RF, R41, or both. The way to use this is to make R2pRF = R2_RF and R41 = R2_RF/2. If the charge pump current or comparison frequency is increased, it is possible to keep the loop filter and phase margin optimized with these resistors. Although this example is for the RF loop filter, the same concept applies to the IF loop filter.

Charge Pump or Comparison Frequency Multiplier	R2pRF	R41	FloutRF	FLoutIF	Equivalent Fastlock Resistor	Loop Bandwidth Multiplier
1X	R2_RF	R2_RF/2	Tri-State	Tri-State	OPEN	1X
4X	R2_RF	R2_RF/2	Low	Tri-State	R2_RF	2X
9X	R2_RF	R2_RF/2	Tri-State	Low	R2_RF/2	3X
16X	R2_RF	R2_RF/2	Low	Low	R2_RF/3	4X

TUNING VOLTAGE ACCESS

The tuning voltage is brought out to an SMA. This is useful for charge pump sweeps and VCO characterization. Note to characterize the VCO on the board with a VCO tester, it is not necessary to remove the PLL. Simply power it down. When this feature is not used, resistors R30 and R36 should be removed. Note that if R30 is removed, so is support for switched filters.

ANALOG LOCK DETECT SUPPORT

R34, R35, and C21 are there so that lock detect filters can be constructed. Note that this is intended for open drain lock detect.

INPUT IMPEDANCE MEASUREMENTS

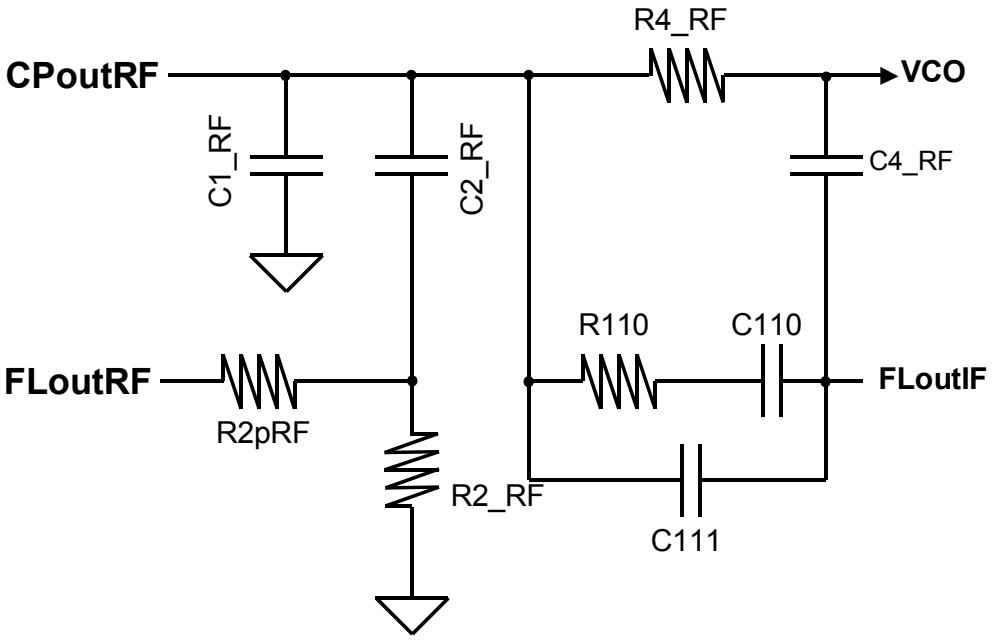
Because the RF traces are straight into the PLL, one can short C15, R38, and R7. Open R3, R5, and R9. Put 100 pF in C17. To calibrate the equipment, use 0 ohm, 50 ohm (2 100 ohms in parallel), and open in R9. This way the trace is calibrated out and it is not necessary to destroy the board in order to put a piece of semi-rigid cable on it. Measurements done in this way turn out to have less “squiggly” lines than by trying to calibrate out the board trace with the port extensions function.

BANDSWITCH VCO SUPPORT

The board is also configured so that CodeLoader can control a bandswitch VCO for either the RF or IF PLL. In order to do this, one can use the trigger pin. Don’t forget to stuff the components on the bottom layer from this.

RF SWITCHED FILTER SUPPORT

Switched loop filters are useful in dual band applications where one standard has a hard lock time requirement and an easier spur requirement than the other. For this mode of operation, FloIF is tri-state and C42, C43, C4_RF ,and R53 add in parallel with R4_RF and reduce the thermal noise, but theoretically do not impact the PLL loop dynamics (they may impact it a little due to non-zero VCO input capacitance). In the other mode, the FloIF pin is pulled to ground and an extra pole is formed with R4_RF and C4_RF. Now C42 adds in parallel with C1_RF and C43 >> C2_RF such that we can neglect C2_RF and R2_RF and replace that with R53 and C43 for theoretical analysis. On the bottom of the board are components that can be switched in addition to the RF loop filter. The intention of this feature is that R3_RF is 0ohm and C3_RF is open. Now R40 and R2pIF need to be open and R41 should be 0 ohms.



SENSITIVITY MEASUREMENTS

In order to measure sensitivity, short C15 and R38, open R3, put 330 ohms in R5 and R9, put 18 ohms in R7, and put 100 pF in C17. Then from the signal generator, but a cable and between the cable and the board, put a 3 dB pad connector. Now reflected waves in the cable should be minimized by this. Also the 3 db pad constructed on the board with R4, R7, and R9 minimizes standing waves on the board trace. To record the sensitivity level, take the signal generator power level, and subtract 7 db. (1 for the cable, 3 dB for the pad connector, and 3 db for the pad on the board).

CRYSTAL/TCXO SUPPORT

To add a TCXO, short R37 and R39. C114 and C115 form the load capacitors. Now the footprint is 4 pins, not two. put the crystal across pins 4 and 3, but be careful to avoid pin 2, which is ground.

LDO SUPPORT

On the bottom of the board, both of the VCOs and the PLL may be run of a power regulator. The board in mind was the LP2985. Note that the LDOs can be controlled via CodeLoader. In order to do this, one can use the Trigger pin. Don't forget to stuff the appropriate components on the bottom layer.

Appendix H – Evaluation Board Test Limits

The test limits used to test the LMX2470 evaluation board are shown below. Note that test limits are always worse than typical conditions because they account for board to board variation. In addition to this, they also may be worse in order to simplify and speed up the measurement process. This evaluation board is typically tested with an automated test program.

PLL	Parameter	Offset	Test Limit	Comments
RF	Phase Noise	3 KHz	-83	CPUD=2. Marker Noise Function ON.
RF	Phase Noise	5 KHz	-80	CPUD=2. Marker Noise Function ON.
RF	Lock Time	1 KHz	550	TOC=700
RF	Fractional Spur	200 KHz	-68	CPUD=3
IF	Phase Noise	5 KHz	-82	Marker Noise Function ON.
IF	Spur	200 KHz	-69	Note that the spur is typically far below this, but this measurement can be limited by the noise floor of the spectrum analyzer.

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