LMH0303,LMH0344,LMH0356

Literature Number: SNLA173

3G-SDI:
32 Loop Cascade Analysis

National Semiconductor
Lab Report
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Abstract

A distribution amplifier (DA) is often used as a repeater in broadcast video applications to extend the reach of a link, most commonly 75Ω coaxial cable. The data path in a DA consists of an SDI adaptive cable equalizer, SDI reclocker and SDI cable driver. In an operational system a video signal may be transmitted through multiple DAs or similar equipment, such as a video router, before reaching its final destination. The DA's primary function is to reconstruct signal integrity of the incoming attenuated signal back to its original state by opening the waveform eye (equalizer), cleaning high-frequency jitter (reclocker) and setting appropriate slew rate and signal amplitude (cable driver). Low frequency jitter, below the loop bandwidth of the reclocker's PLL, will be passed through. Adding several DAs in cascade will eventually result in accumulated low - frequency jitter commonly referred to as jitter peaking. Some SDI reclockers and equalizers are more susceptible to jitter peaking than others. This report focuses on an experiment to determine the effects of cascading multiple DAs using National Semiconductor's LMH0344 SDI adaptive cable equalizer, LMH0356 SDI reclocker, and LMH0303 SDI cable driver.

In the experiment, eye patterns were collected, jitter tolerance graphs acquired using a PRBS10 and matrix pathological data patterns, and bit error rate testing (BERT) was conducted. This report examines in detail the experiments performed and results obtained.

Table of Contents

Test Setup……..……2

Jitter Definitions…….3

SMPTE Jitter Requirements ……..…….4

Waveform Eye Diagrams……..……..5

Jitter Tolerance Measurements ……..……8

Bit Error Testing ……..10

Conclusion ……...11

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Test Setup

Test Equipment List:

- Agilent N4903A J-BERT Bit Error Rate Tester
- Agilent DCA-J Scope
- HP 6023A DC Power Supply

Hardware List:

- Octal DA Evaluation Board (4)
- Pasternack 50Ω to 75Ω Adaptor PE7006
- Belden 1694A coaxial cable (100m lengths)
- Belden 1694A coaxial Cable (1m and 2m lengths)

Conditions:

- Room temperature
- 3.3V supply voltage

Figure 1 shows the experimental setup. After going through a 50Ω to 75Ω adaptor, the signal from the 50Ω data output of the Agilent J-BERT goes through 120m of Belden 1694A cable. In between each stage, 1m lengths of Belden 1694A cable connect consecutive DA ports. For the jitter tolerance test, the last stage data and the recovered clock are fed to the test data input of the Agilent J-BERT. A second 50Ω to 75Ω matching attenuator was used on the data output of the DA cascade. An automated test program developed at National Semiconductor was run to first align the clock and data and then record the jitter tolerance using a PRBS-10 data pattern.

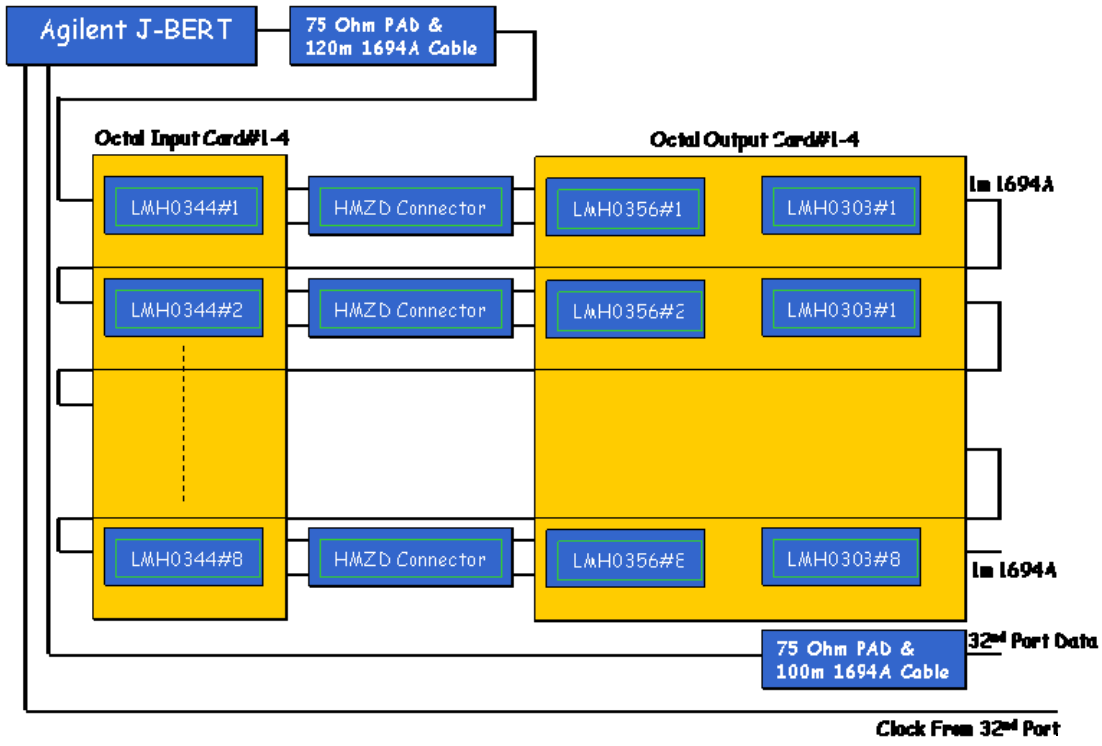

FIGURE 1. Experimental Setup

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Jitter Definitions

In digital communication, jitter is defined as time deviation from the ideal timing of the signal transition [1]. Any jitter that describes how much in time a clock edge varies can be given as a peak-to-peak number. Peak-to-peak jitter specifications are convenient when the jitter is deterministically characterizable. But as random jitter is probabilistic, it is difficult to say what the maximum jitter can possibly be [2]. In general jitter is divided into two categories: Random Jitter and Deterministic Jitter [2]:

Random jitter (RJ) is characterized by a Gaussian distribution and comes from physical sources such as thermal noise, shot noise, and wave scattering in fiber (i.e. mainly from Multimode Fiber). RJ is modeled as a Gaussian distribution and is used to predict peak-to-peak jitter as a function of bit error [2].

Deterministic jitter (DJ) is generally bounded and non-Gaussian. Duty Cycle Distortion (DCD), Periodic Jitter and Bounded Uncorrelated jitter all are components of Deterministic Jitter [3].

In Video applications, there is a potential for a long chain of regenerative repeaters. Signal regeneration is beneficial in extending the reach of the transmission media, preventing the accumulation of noise and distortion through the transmission media. However, the regenerative repeater itself contributes an accumulation of jitter which can become a critical problem if it is not properly controlled through the careful design of the timing recovery circuit. This accumulation of jitter will typically result in a limit on the number of repeaters of a given design which can be installed in the transmission path before the accumulated jitter becomes intolerable.

When considering the accumulation of jitter it is imperative to distinguish between the two basic types of jitter. In a long chain of repeaters deterministic jitter greatly dominates random jitter [2]. This is because the DJ component is the same in each repeater and therefore adds coherently. Effects of the jitter introduced by one repeater on the jitter introduced upstream will be slight as long as the total introduced jitter remains low and thus we can assume that the jitter in each repeater is additive [2].

Let's assume each repeater has an equivalent jitter transfer function. We should consider the following three cases [2]:

At frequencies where the jitter transfer function has gain, as the number of repeaters in cascade increases, the overall jitter gain could approach infinity. As such, the jitter peaking of the PLL will eventually limit the number of repeaters that can be placed in cascade.

For frequencies where the jitter transfer function has a magnitude much less than unity, meaning the input jitter is attenuated through the repeater, we can say there is not much jitter accumulation and the only significant jitter is that introduced in the last stage.

The third critical case is where the jitter transfer function is equal to unity (i.e. the input jitter is passed through). This will occur within the pass band of the jitter transfer function. As such N repeaters would result into N times the jitter amplitude and jitter increases in proportion to number of loops or cascade. In this case, the only way to limit the accumulated jitter is to reduce loop bandwidth.

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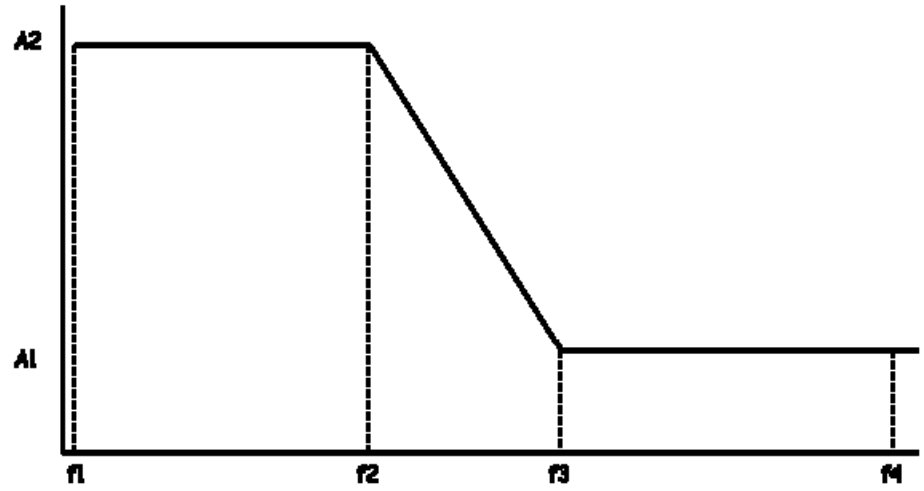
SMPTE Jitter Requirements

Random jitter is specified in the way it describes clock edge fluctuations. Accordingly, jitter is typically listed as an amount of one clock period, or an amount of one unit interval (UI). Should the edge of a clock jitter around over time 10 picoseconds (ps) within a 100ps clock period, then the jitter is 0.1 UI.

SMPTE Jitter Tolerance Specifications



SMPTE259	f1	f2	f3	f4	A1	A2
SMPTE259	10Hz	200Hz	1KHz	*	0.2UI	6UI
SMPTE292	10Hz	20KHz	100KHz	*	0.2UI	1UI
SMPTE424	10Hz	15KHz	100KHz	*	0.3UI	2UI

* > 1/10 Clock Rate

FIGURE 2 – Jitter Tolerance Specifications from SMPTE serial data transmission standards

The eye diagrams from the first twelve cascaded loops are shown next. The output clock from the BERT was used as the trigger or clock source for the DCA-J scope. A PRBS10 data pattern was used.

Figure Number	Number of DAs	Data Pattern
3	1	PRBS10
4	2	PRBS10
5	3	PRBS10
6	6	PRBS10
7	12	PRBS10

Table 1 – Eye Diagram Tests

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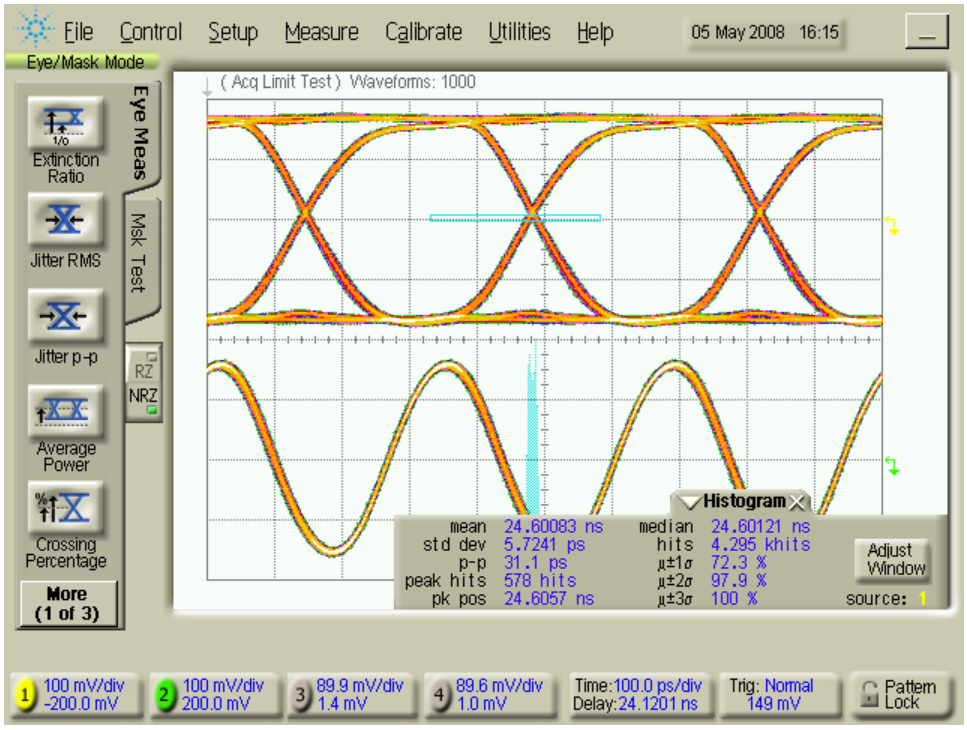

FIGURE 3. Eye Diagram after the first stage using a PRBS10 data pattern

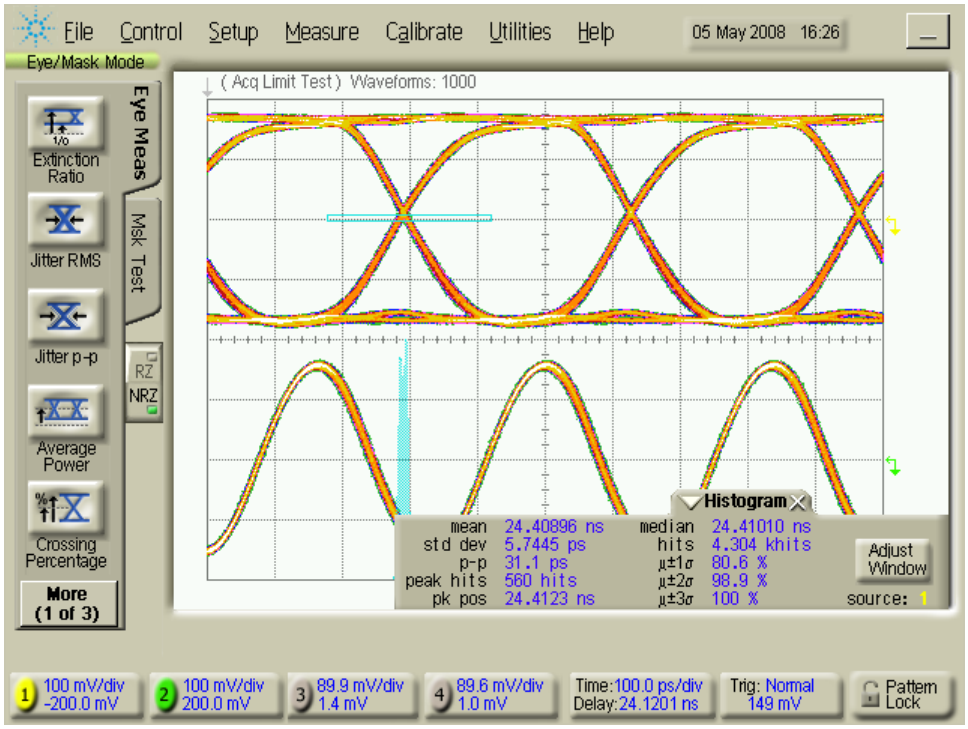

FIGURE 4. Eye Diagram after the second stage using a PRBS10 data pattern

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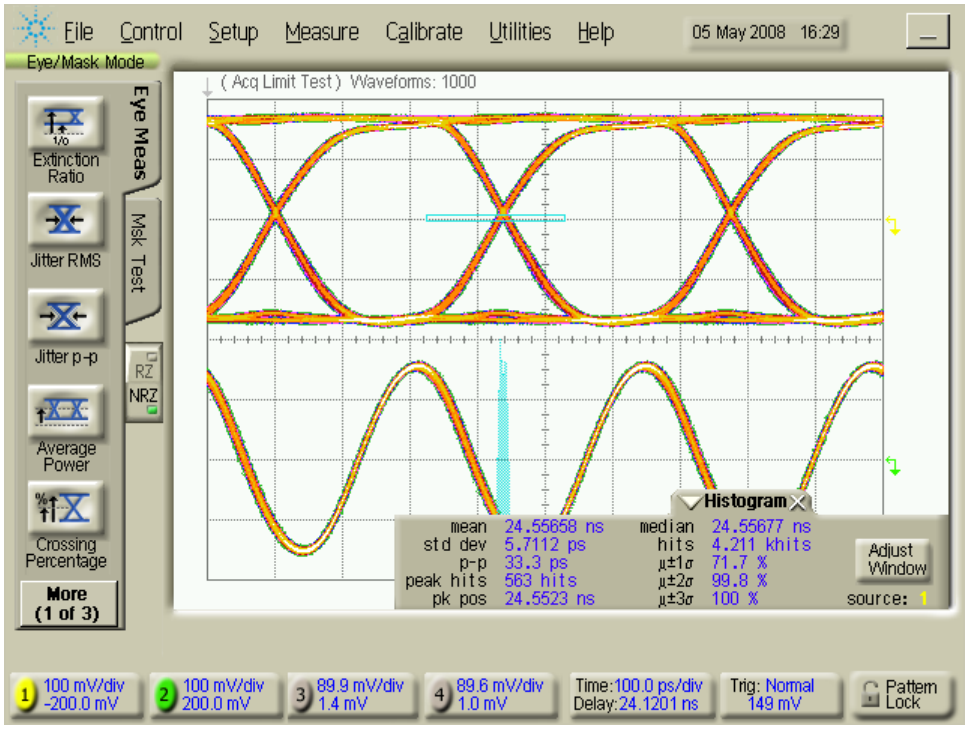

FIGURE 5. Eye Diagram after the third stage using a PRBS10 data pattern

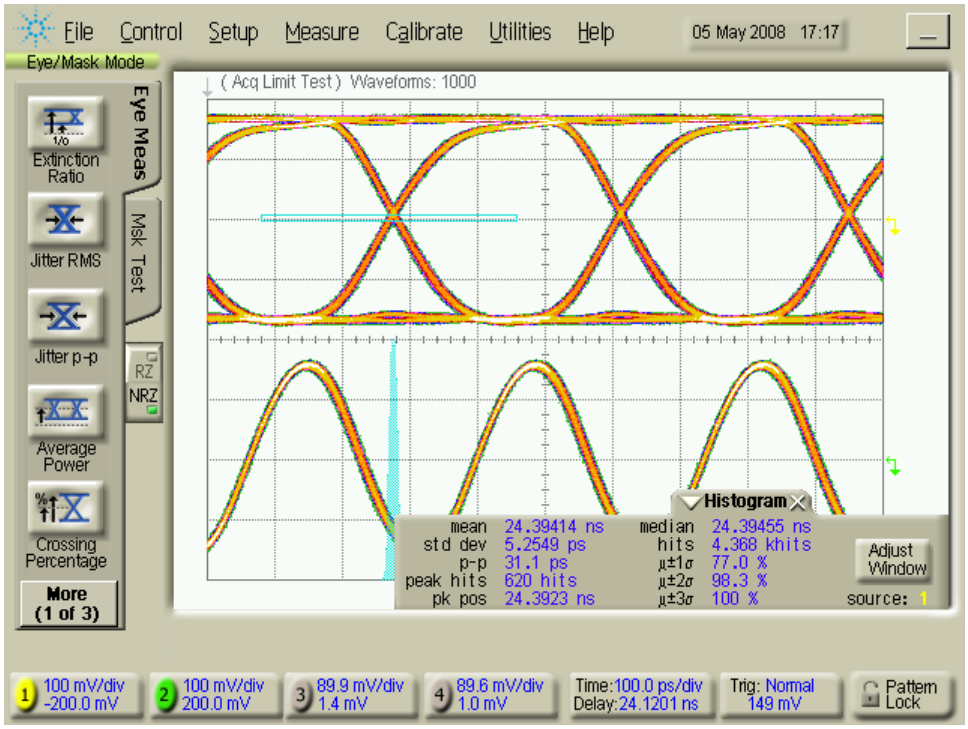

FIGURE 6. Eye Diagram after the sixth stage using a PRBS10 data pattern

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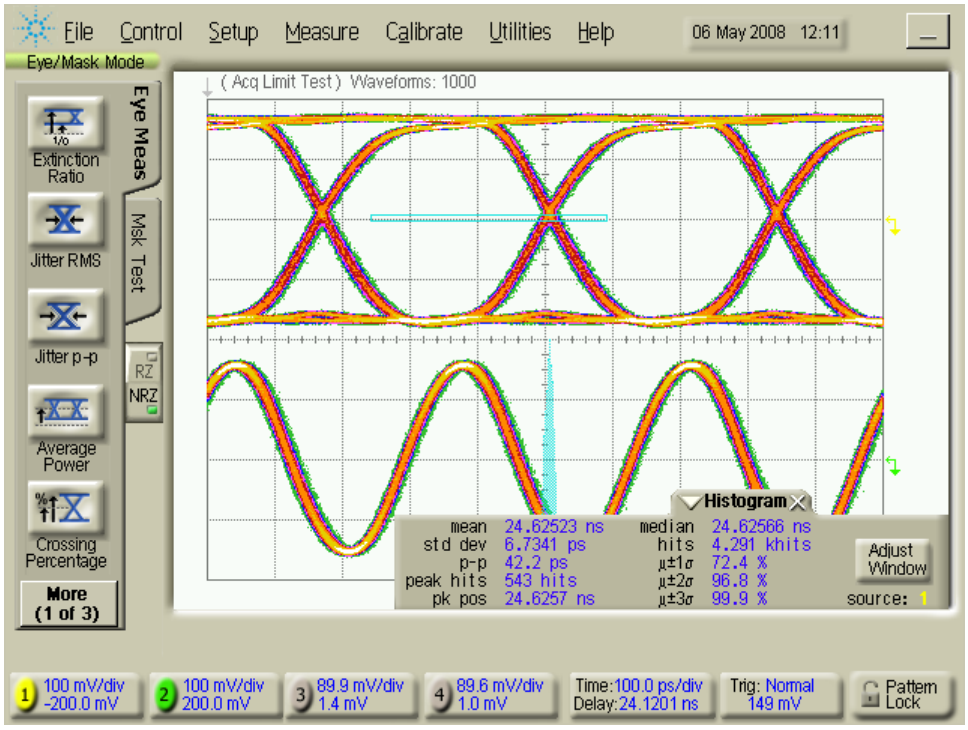

FIGURE 7. Eye Diagram after the twelfth stage using a PRBS10 data pattern

Based on these eye diagrams, the PRBS10 data pattern which, from a spectral standpoint, is very much like a color bar pattern, exhibits essentially the same jitter at every point in the cascade. Thus it is conceivable that using the PRBS10 or color bar pattern we could potentially have a much larger number of cascaded ports even than 32.

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Jitter Tolerance Measurements

The number of loops used in the experiment was increased from 1 to 8, 16, to 24, and then to 32. For each cascade setup, the jitter tolerance was measured. Figures 8 and 9 show the jitter tolerance for a PRBS10 data pattern and the matrix pathological data pattern, respectively.

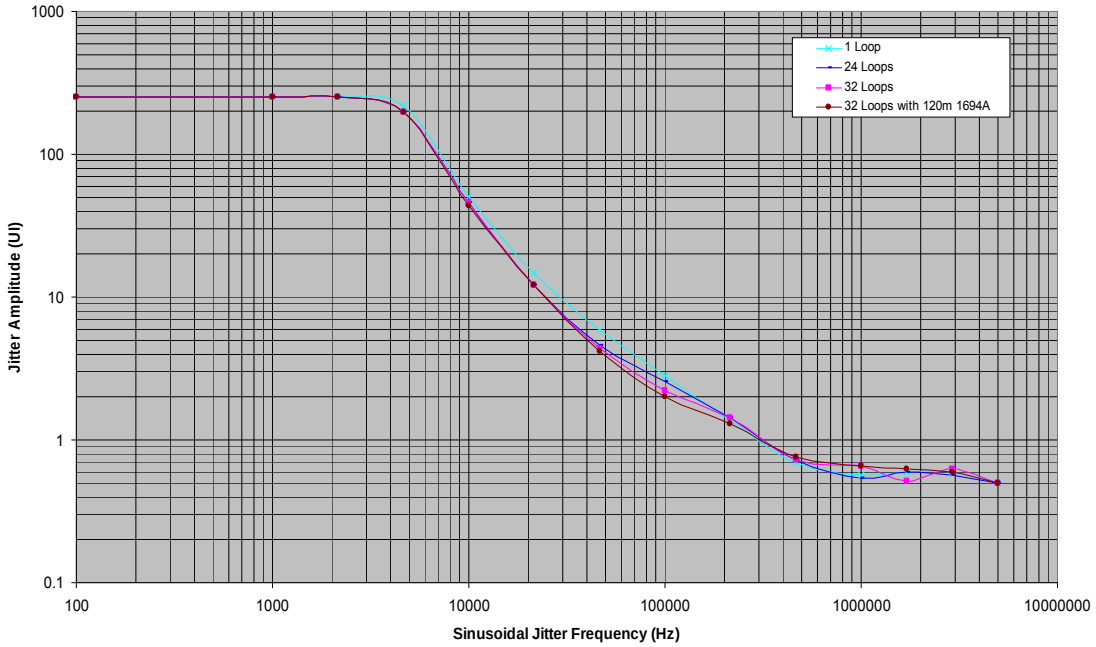

Figure 8. Jitter Transfer using PRBS10 data pattern

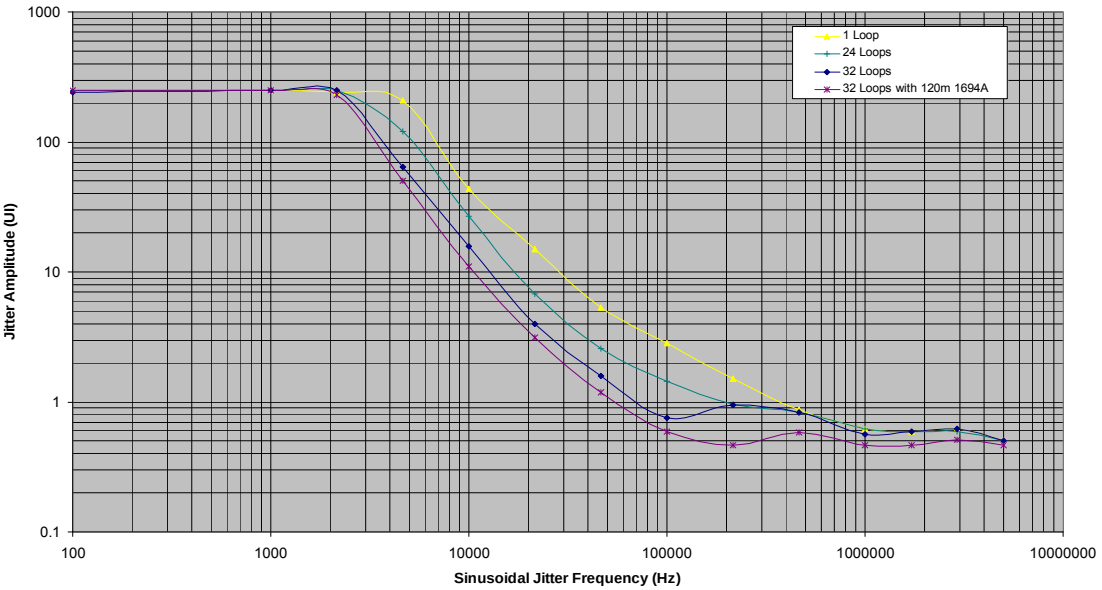

Figure 9. Jitter Transfer using Matrix Pathological data pattern

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Inspection of jitter tolerance graphs shows that as the number of loops increase, the overall loop bandwidth is reduced. Even with a cascade of 32 DAs, a jitter tolerance at high jitter frequencies of 0.4 to 0.5UI is maintained. Further, the low frequency jitter tolerance is maintained at 250UI (the limit of the instrumentation). This suggests that a cascade of more than 32 loops may be achievable with reasonable performance.

Using the 32-port cascade setup and an Agilent J-BERT, we ran data with 0.5 UI of injected sinusoidal jitter at 5 MHz through the cascade error-free for 3 consecutive days[1]. Note Figures 10, 11, and 12.

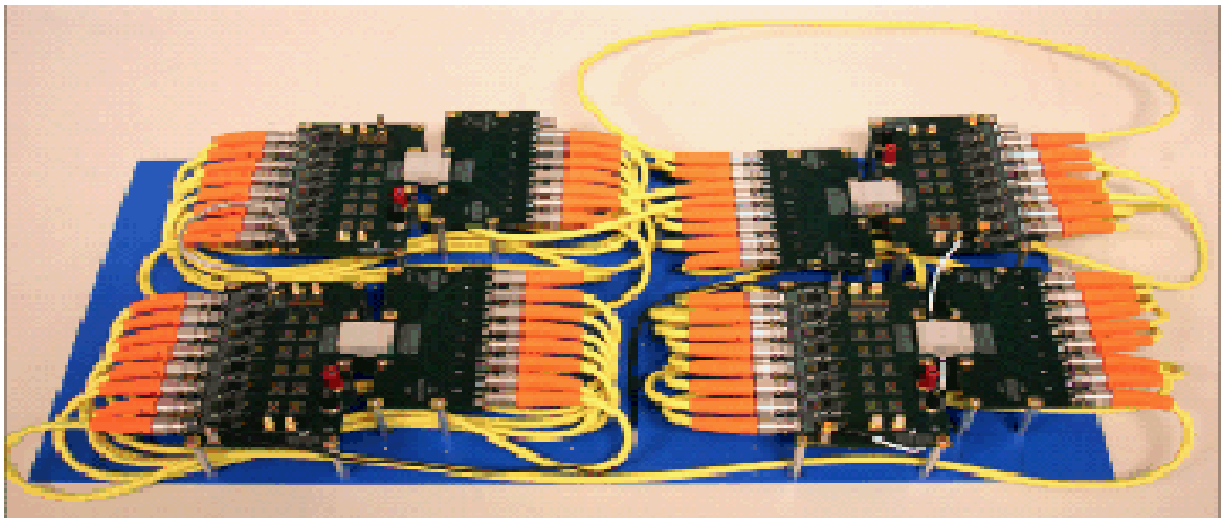

Figure 10. 32 Port Cascade Hardware Setup

[1] BERT experiment was limited to three days due to equipment availability, no error was detected.

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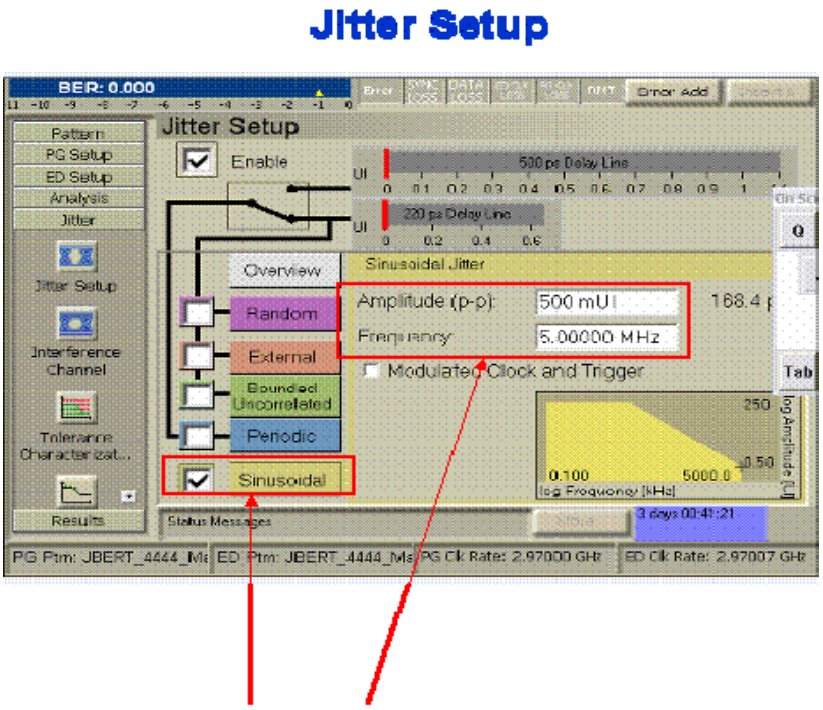

Figure 11. J-BERT Jitter Setup for 32 port reference clock cascade application

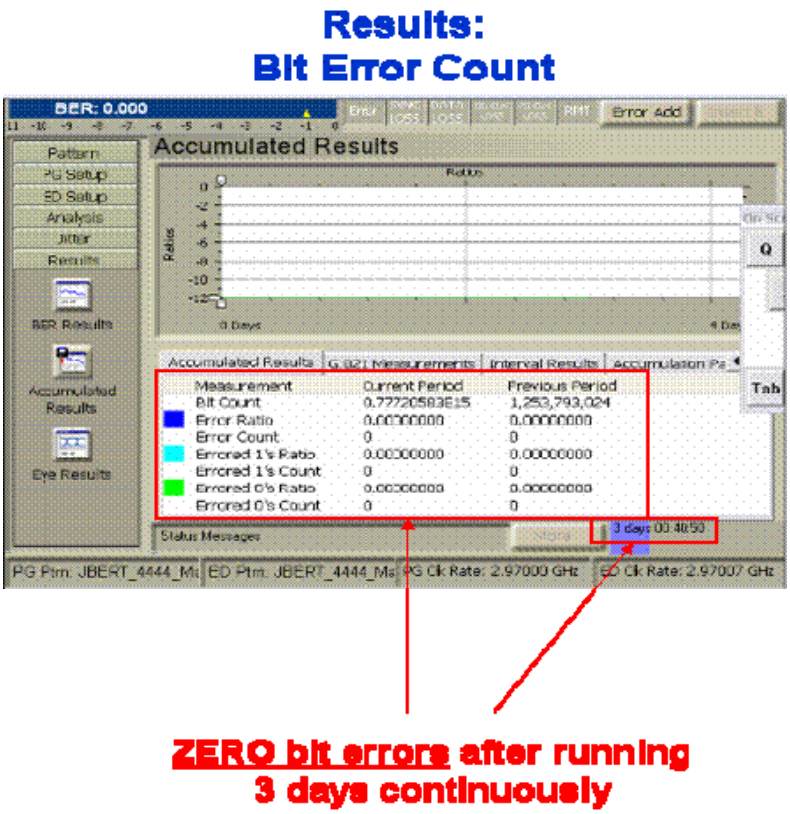

Figure 12. J-BERT Result for 32 port reference clock cascade application

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Conclusion

Using the setup described in this report, we were able to successfully pass stressful signals through 32 cascaded distribution amplifiers with zero bit errors demonstrating the robustness of National Semiconductor's SDI data path. We have conducted further experiments with a higher number of cascaded stages and have not yet found the fundamental limit of the system. Through the experiment, we demonstrate the low intrinsic output jitter of National's LMH0344 SDI cable equalizer and LMH0303 SDI cable driver. The LMH0356 reclocker shows very robust low-frequency jitter tolerance while at high-frequencies the low-pass jitter transfer function attenuates the input high-frequency jitter. Therefore, the system is able to pass matrix pathological and PRBS10 (similar to color bars) data patterns while exceeding SMPTE jitter tolerance/transfer requirements with significant margin. The Agilent J-BERT jitter measurements confirmed that the system can run error free with at least 32 DAs in cascade for extended periods of time.

A single 27 MHz crystal as a reference clock for all 32 reclockers in this experiment. Please refer to the Reference Clock Cascade Lab Report.

References

SMPTE Recommendation "Specification of Jitter in Bit-Serial Digital Systems" RP-184-2004 Revision of RP184-1996

Edward A. Lee & David G. Messerschmitt "Digital Communication" – Second Edition

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