DS92LV0411,DS92LV0412,DS92LV0421, DS92LV0422,DS92LV2411,DS92LV2412, DS92LV2421,DS92LV2422,DS92LV3221, DS92LV3222,DS92LV3241,DS92LV3242, DS99R103,DS99R104

Literature Number: SNLA200

Channel Link II Design Guide

2011 national.com/serdes

Best Practices for Serializing High-Speed Data Links

National Semiconductor

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1.1 Why Serialize?

The main benefit of serialization is a significant reduction of signal lines and connector pins. Thus, serialization enables smaller, more economical boards that are easier to lay out, smaller IC packages, and also allows for more wide bus pins that can be used for additional device functionality. Cost savings also extend into the interconnects with fewer, lighter, and mechanically smaller cables and connectors. Generally, these system savings significantly offset the cost of implementing serialization/deserialization, yielding a smaller, lower-cost system overall.

Depending on the application, serialization benefits may extend to lower power consumption, reduced system noise (electromagnetic interference), increased noise tolerance, or even longer interconnects.

1.2 The Parallel Bus

In general, the simplest bus configuration is a point-to-point link. If more data per time interval is required, there are two general options—drive the signal faster or add additional signal lines. Both solutions are shown in ***Figure 1-1***.

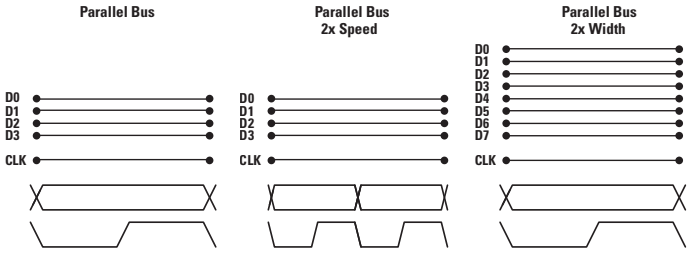

Figure 1-1. Increasing Bandwidth on a Parallel Point-to-Point Bus

Increasing the signaling rate may be viable for small improvements, but what about 10x, 50x, or even 100x improvements? Many factors affect the feasibility of this type of scaling, but normally it becomes limited quickly by the I/O cell, power, or signal integrity constraints. Therefore, simply increasing the signaling rate is not an ideal solution.

A more common solution is to simply increase the bus width. This solution quickly adds cost as additional I/O cells, pins, and interconnects are needed. Power consumption and noise generation also increase. As edge rates, speeds, and lengths increase, additional ground signals typically are required, up to a ratio of one ground connection per signal line. Adding lines quickly becomes an unattractive solution.

Serializer (Ser) and Deserializer (Des) devices solve this interconnect challenge by **reducing** the number of pins required. The serializer collects many lower-speed signals and transmits them over fewer, higher-speed signals. The deserializer recovers the high-speed signals and converts them back into their original form as shown in ***Figure 1-2***.

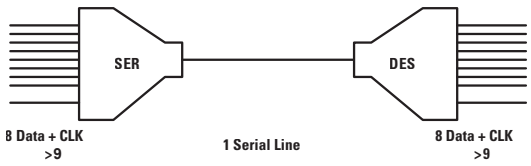

Figure 1-2. Ser/Des Devices reduce Wire Count

1.3 Ser/Des

National Semiconductor first introduced Ser/Des devices in the early 1990s, covering a wide variety of applications. The original family of "Channel Link" Ser/Des devices collected a wide single-ended data bus (originally 5V CMOS) and a synchronous clock, reducing the data bus to fewer Low Voltage Differential Signaling (LVDS) serialized signals. The LVDS signals could operate much faster, and at lower power, than single-ended CMOS. Additionally, they generated less Electromagnetic Interference (EMI) and offered high noise tolerance. The chipset evolved over time to interface to 3.3V LVCMOS, along with several speed upgrades, including support for parallel bus widths of 21, 28, and 48 bits at clock rates up to 133 MHz.

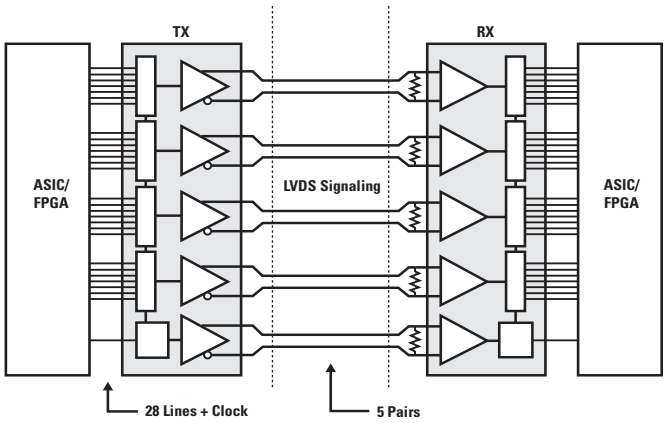

Figure 1-3. Channel Link (I) – DS90C285/86 with 29-to-10 Wire Compression

Introduction

The 28-bit chipset has been widely adopted in many applications, including a de-facto frame grabber standard called “Camera Link”. This version of Channel Link (I) supported 24-bit RGB (8 bpp), three video control signals, and one general-purpose signal for 28 data bits total, serializing them down to four LVDS data pairs and one LVDS clock pair (five pairs, 10 pins total). This gave rise to its nickname: “many-to-few” and is shown in ***Figure 1-3***.

Channel Link II is the 2nd generation of Channel Link Ser/Des devices and offers new features along with additional reduction in signal pairs. Instead of multiple pairs, Channel Link II Ser/Des serializes data and the clock onto a single signal pair. It uses a scheme called embedded clocking to reduce data and the clock onto a single pair. This lowers the cable cost and eliminates the need to specify and control the skew between pairs (Receiver Skew Margin (RSKM)). As such, Channel Link II is nicknamed “many-to-one” and is shown in ***Figure 1-4***.

Channel Link III, nicknamed “do more,” is the 3rd generation of the family and it focuses on the utilization of the same single twisted pair to do more work. In addition to a high-speed forward link, it also implements a lower-speed, bidirectional, full duplex, real-time control channel.

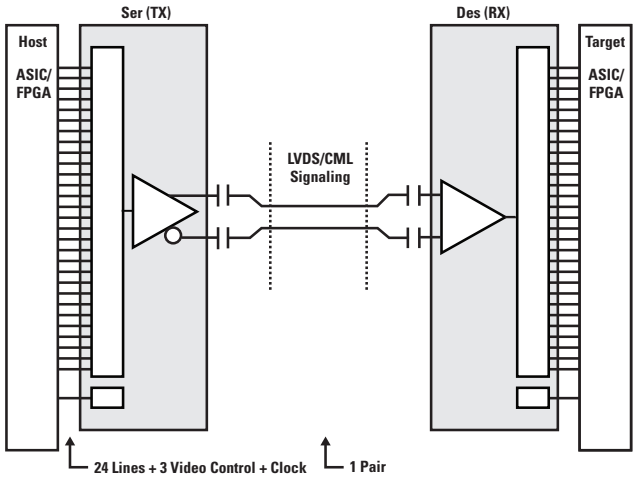

Figure 1-4. DS92LV2421/22 Ser/Des Applications

National’s three generations of Channel Link devices have greatly influenced the industry, setting the standard in bandwidth, reach, and advanced features. Additional versions are available, covering notebook and desktop monitors (FPD-Link) as well as automotive-grade parts for display and imaging (FPD-Link II and III) in vehicle applications. The three generations of Channel Link products are depicted graphically in ***Figure 1-5***.

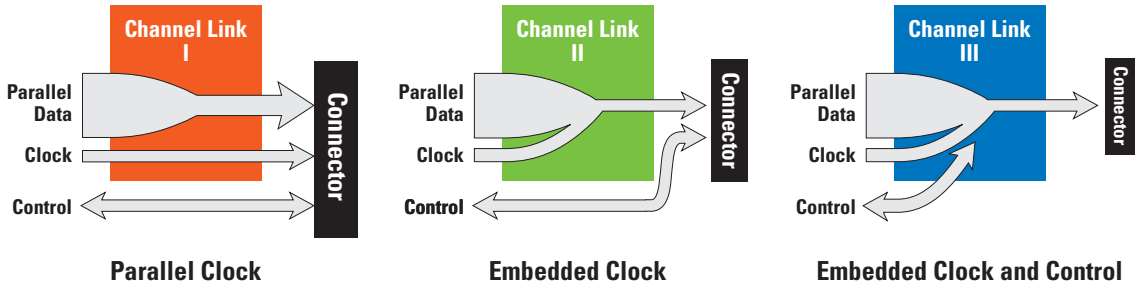

Figure 1-5. Channel Link Generations

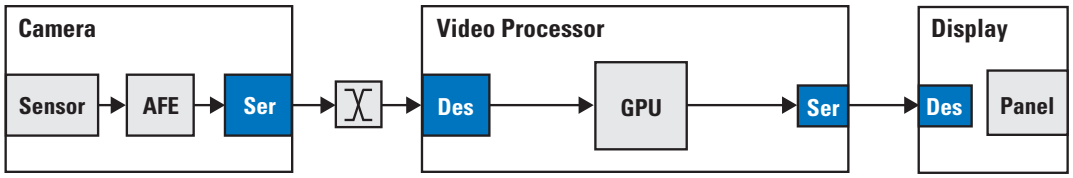

Figure 2-1. Industrial Video Application

Figure 2-1 shows the typical block diagram of an industrial video application. Video images are captured by a camera, distributed through an industrial cabling network to a processing device. The video can be processed to extract data (factory automation applications), displayed on a screen (security and medical applications), or stored for later use.

Industrial imaging systems now require higher-resolution and bit-depth images to provide the detail required for complex analysis. This is critical for uses such as electronics inspection equipment where shrinking geometries necessitate more detailed examination. Applications such as security and surveillance are moving to HD resolution and beyond due to the need for high resolution in video analytics.

On the display side, LCD displays have become thinner and brighter and can produce much higher resolution images with deeper color. The cost of LCD monitors has decreased, leading to a proliferation of LCD display applications. Advanced features such as 3D displays and touch screens have also helped boost the number of industrial imaging applications.

As displays become larger and support deeper color, the amount of video data that needs to be transported increases. Shown in ***Table 2-1***, National's Channel Link II family of devices supports a wide variety of display applications, from small QVGA displays to HD displays. These devices also support a wide variety of bus widths to support different color depths such as 18-bit or 24-bit color.

2.1 Key Features

- Support for a wide variety of video applications—display, images, and data
- Support for up to 32-bit bus widths
- Automatic receiver lock without training patterns or characters, "plug-and-go" operation
- No external coding or framing required
- Very low power consumption
- Wide operating frequency range
- Deserializer requires no external clock source
- Long reach over cables and FR-4 backplanes
- Industrial temperature range support
- Support for spread spectrum clocking

Product ID	Function	Ratio	Clock (MHz)	Parallel Bus	Total Bandwidth (Gbps)	Lanes	Unique Feature
DS92LV3241	Serializer	32:4	20 to 85	LVCMOS	2.7	4	No RSKM
DS92LV3242	Deserializer	4:32	20 to 85	LVCMOS	2.7	4	No RSKM
DS92LV3221	Serializer	32:2	20 to 50	LVCMOS	1.6	2	No RSKM
DS92LV3222	Deserializer	2:32	20 to 50	LVCMOS	1.6	2	No RSKM
DS99R103	Serializer	24:1	3 to 40	LVCMOS	1	1	Low frequency support
DS99R104	Deserializer	1:24	3 to 40	LVCMOS	1	1	Low frequency support
DS92LV2411	Serializer	24+:1	5 to 50	LVCMOS	1.2	1	Plus video control
DS92LV2412	Deserializer	1:24+*	5 to 50	LVCMOS	1.2	1	Plus video control
DS92LV0411	Serializer	4:1	5 to 50	LVDS	1.2	1	4D+C (Channel Link) input
DS92LV0412	Deserializer	1:4	5 to 50	LVDS	1.2	1	4D+C (Channel Link) output
DS92LV2421	Serializer	24+:1	10 to 75	LVCMOS	1.8	1	Plus video control
DS92LV2422	Deserializer	1:24+	10 to 75	LVCMOS	1.8	1	Plus video control
DS92LV0421	Serializer	4:1	10 to 75	LVDS	1.8	1	4D+C (Channel Link) input
DS92LV0422	Deserializer	1:4	10 to 75	LVDS	1.8	1	4D+C (Channel Link) output

* 24+ = 24 video data + (HYSNC + VSYNC + DATA ENABLE) 3 control

Table 2-1. Channel Link II Devices

Target Applications

This section introduces several targeted applications for Channel Link II serializers and deserializers. These include general-purpose data applications ***(shown in Figure 3-1)*** as well as advanced designs in consumer and industrial products.

Depending on the exact design requirements, the Channel Link II family of products offers Ser/Des options in varying speeds, input configurations, as well as single-, dual-, or quad-lane LVDS. All feature an embedded data clock.

3.1 General-Purpose Data Communication

Channel Link II products are well suited for transport of large parallel data buses over long distances. This includes situations where a large parallel bus originating from a CPU, ASIC, Field-Programmable Gate Array (FPGA), or other data source requires transport over long distances, including cable and FR-4 backplane traces. A Ser/Des scheme helps to alleviate skew and routing complexity problems inherent in wide, high-speed parallel data buses.

3.2 Display Signage

Large, active display signs often require distribution of video frames over a series of large display panel sub-sections that work as part of the overall screen. This requires a high-speed data link capable of distributing uncompressed video data over multiple-meter distances across the distributed display electronics of the larger system. Furthermore, cabling and routing constraints may require daisy chaining multiple panels to save on cabling weight and cost. An example is shown in ***Figure 3-2***.

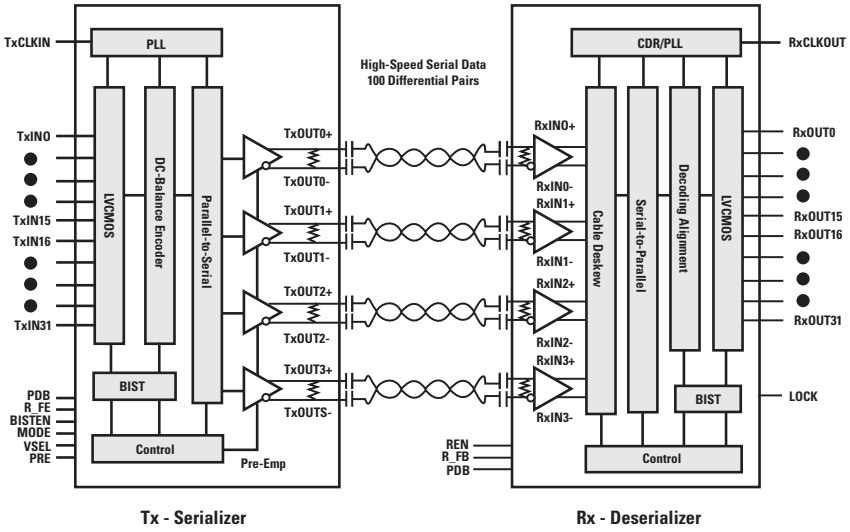

Figure 3-1. Example of a General-Purpose Channel Link II Ser/Des Application

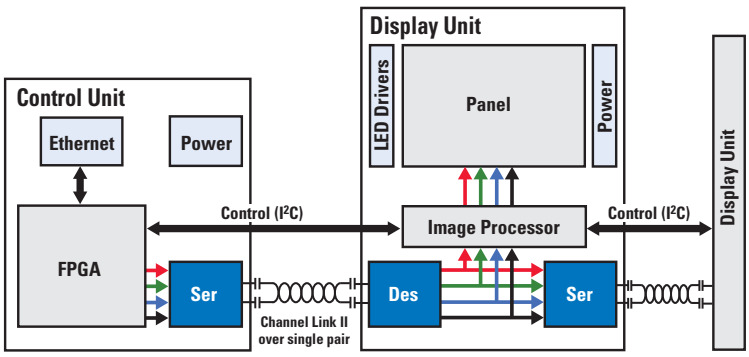

Figure 3-2. Example of a Display Signage Block Diagram using Channel Link II Ser/Des

3.3 Security and Machine Vision

Channel Link II data links are ideal for the transmission of high-speed, uncompressed video data from cameras used in surveillance and machine vision applications. These applications are especially sensitive to the size and complexity of remote data and control units. Other physical link options may be prohibitively bulky (larger cables or parallel buses) or limited in maximum cable length and signal integrity tolerance within diverse environments. Security cameras can be especially constrained due to the diversity of physical locations and conditions required for this application. ***Figure 3-3*** shows an example implementation.

Machine vision systems are often sensitive to any latency, signal degradation, or compression loss introduced by other video link solutions. Channel Link II Ser/Des overcome this by allowing the transmission of raw, high-speed and high-resolution video data in real time.

3.4 Medical Imaging

Medical imaging applications require the transmission of high-bandwidth, real-time data from instruments and image acquisition to image processing and display units (shown in ***Figure 3-4***). The push to miniaturize and simplify such systems benefits from the use of high-speed data links in the form of Ser/Des devices, including the Channel Link II family of products.

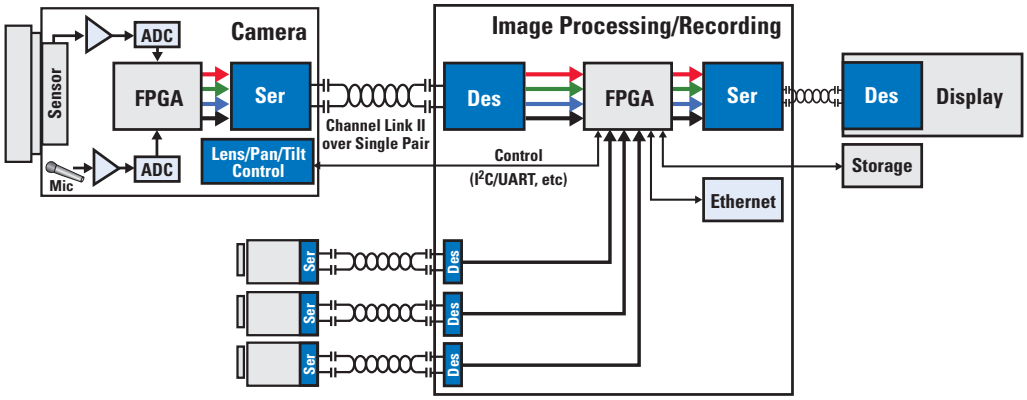

Figure 3-3. Example of a Security Camera System Block Diagram using Channel Link II Ser/Des

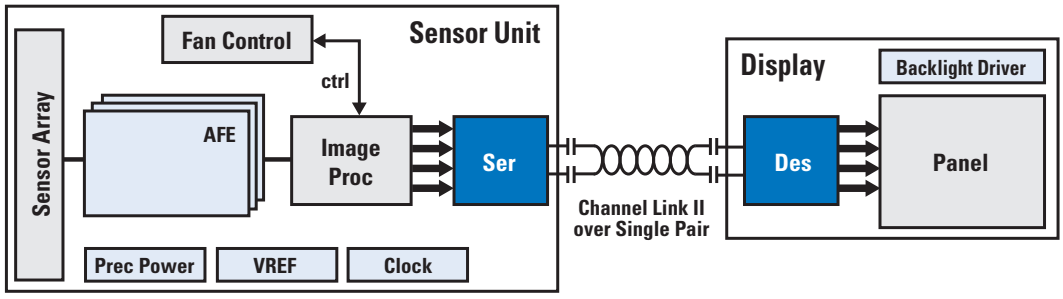

Figure 3-4. Example of a Medical Imaging System Block Diagram using Channel Link II Ser/Des

Target Applications

3.5 Multifunction Printers and Office Automation

Printers, copiers, fax machines, and other office automation systems use multiple internal imaging and data paths for the transport of digital imaging data. This includes the image processing subsystems themselves as well as video displays present on the unit to assist with user control and interaction (shown in ***Figure 3-5***). In addition to being data- and speed-intensive, these applications also benefit from space and weight savings from smaller cables and connectors. The advantages of Channel Link II Ser/Des are therefore very desirable in this space.

3.6 Factory Automation

Automation and control applications for the industrial environment require high-speed video links for remote control and monitoring of processes and equipment. These systems may be deployed in situations where environmental and space constraints may require compact, remote transmission of data between control units and control systems. This includes intelligent sensor and imaging applications for process acquisition and control. An example is illustrated in ***Figure 3-6***.

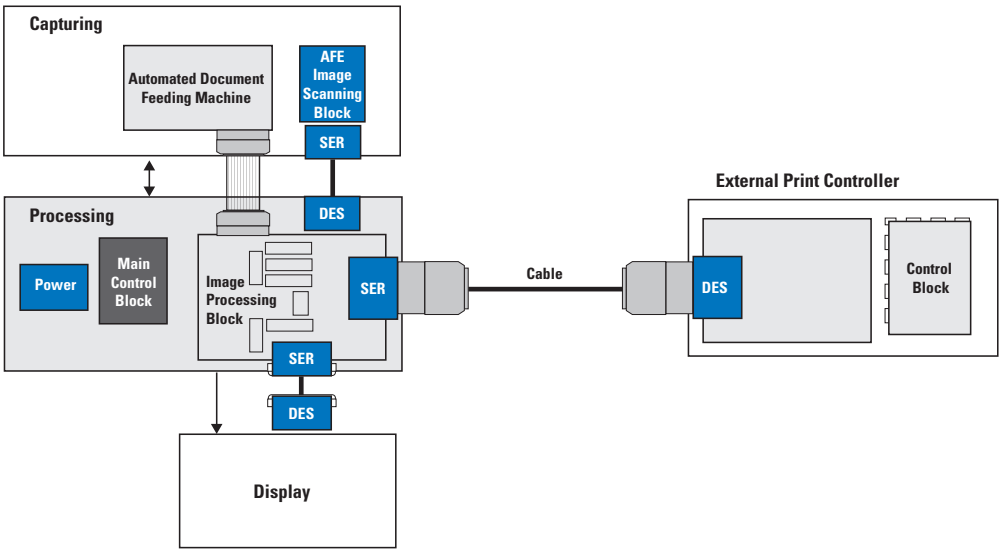

Figure 3-5. Example of a Multifunction Printer Block Diagram utilizing Channel Link II Ser/Des

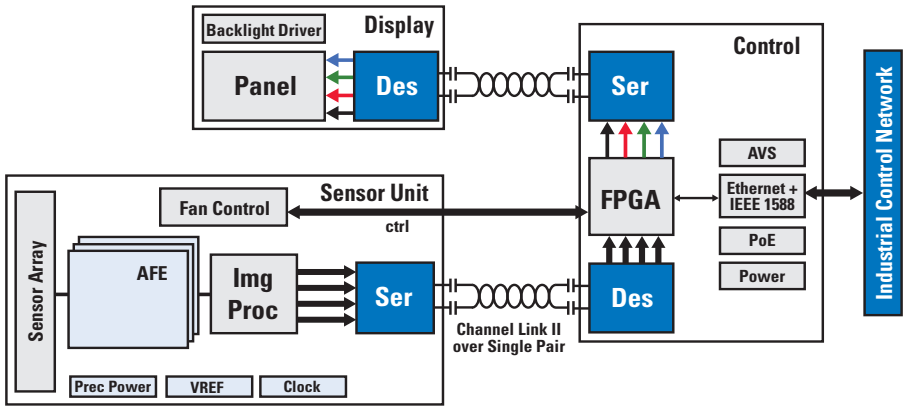

Figure 3-6. Example of a Factory Automation System Block Diagram with Channel Link II Ser/Des

3.7 Video Applications: Typical Resolutions

National offers a wide selection of Channel Link II products suitable to video designs with diverse picture requirements, including various resolutions, pixel clocks, and color depths, covering multiple standard video resolutions (XGA, VGA, QVGA, etc.). The Channel Link II family supports LVCMOS or LVDS I/O to enable interfacing to a variety of panel data input interfaces.

Table 3-1 summarizes a sampling of standard display resolutions and electrical interfaces, including an example display panel and the recommended Channel Link II Ser/Des pair appropriate for that application. ***Table 3-2*** summarizes a sample list of imagers and the appropriate Channel Link II Ser/Des chipset.

Resolution	Typical Size (in)	Color Depth (bits)	Pixel Clock (MHz)	Interface	Example Display Panel	Recommended Ser/Des Chipset
QVGA (320 x 240)	3 to 6	18	6.2 to 6.8	LVCMOS	Sharp LQ035Q7DB05	DS92LV2411/12
VGA (640 x 480)	5 to 12	18	23 to 26	LVCMOS	Sharp LQ057V3DG01 NEC NL6448BC18-01F	DS92LV2411/12
SVGA (800 x 600)	5 to 15	18	33 to 40	LVCMOS	NEC NL8060BC31-20	DS92LV2421/22
		24		LVDS	Sharp LQ070Y3LG4A	DS92LV0411/12
XGA (1024 x 768)	8 to 19	18	60 to 75	LVDS	NEC NL10276BC16-01	DS92LV0421/22
		24			Sharp LQ150X1LGB1	
WXGA (1280 x 768)	14 to 20	24	70 to 80	LVCMOS	NEC NL12876BC26-28	DS92LV3241/42

Table 3-1. Typical Display Resolutions

Resolution	Typical Size (in)	Color Depth (bits)	Pixel Clock (MHz)	Interface	Example Sensor	Recommended Ser/Des Chipset
VGA	—	10	13.5	CMOS	Aptina MT9V011	DS92LV2411/12
WVGA	1/3	10	27	CMOS	Aptina MT9V032	DS92LV2411/12
Megapixel (1.2 Mp)	1/3	12/14	74.25	CMOS	Aptina MT9M033	DS92LV2421/22

Table 3-2. Typical Imaging Sensors

Key Features

The Channel Link II family of serializers and deserializers share a number of key features. Since the family continues to grow and evolve, it is recommended that the respective device datasheets be consulted for full descriptions of device-specific and optional features.

4.1 Extending the Reach with Signal Conditioning

Signal conditioning is a generic term used to describe features that help extend the length of interconnects and provide error-free recovery of transmitted data. Signal conditioning features and techniques may be employed at the link endpoints as well as within the Ser/Des devices themselves.

The serializer usually supports three different features to extend the length of the link. First is encoding. Instead of simply serializing the data and sending it out at a higher speed (employed by earlier devices; namely, the DS90CR285), Channel Link II serializers perform four different operations to optimize the serial stream. First the data is randomized using a Pseudo-Random Bit Sequence (PRBS) pattern to remove static patterns and ensure some transitions. The stream is further enhanced by scrambling bit positions. Next, the data is sent in either true or inverted form to maintain DC balance of the signal. The clock is then embedded by wrapping a fixed low and fixed high around the payload. This maintains DC balance and also ensures another transition. The coding supports the AC coupling of the link to provide isolation between the ends of the link. The randomization, scrambling, and balancing help to open up the eye pattern by reducing the DC wander of the signal. The PRBS pattern is also very useful for reducing EMI generation by removing static beats and spreading out the spectral content of the transmitted data.

Signal conditioning is also addressed at the line driving block. The output driver translates the signal into a low-voltage differential signal based on Current Mode Logic (CML) or LVDS circuit implementations. In either case the output is a differential signal which supports the high-speed transmission of the signal over great lengths. The devices also offer an output voltage select control. This allows for a larger starting signal to be used when the noise environment is high, interconnect lengths are very long, a larger signal is optimal for extending and enhancing the de-emphasis feature, or for other various termination scenarios.

The serializers also support a “transmit emphasis” feature. This is another signal conditioning feature that pre-distorts the signal for the expected losses over the interconnect to yield the best possible eye opening at the receive end. There are two techniques: pre-emphasis and de-emphasis, but in general, they perform the same eye-opening task. LVDS solutions tend to use pre-emphasis, meaning high-frequency components of the signal are driven with additional drive current or signal level, with the low-frequency components driven at a normal level. The media tends to roll off (attenuate) the high-frequency components more, thus one is left with a better mix of high- and low-frequency content at the end of the cable for an improved eye opening. CML-based line drivers tend to use a de-emphasis feature. The signal is driven at normal levels, and if it remains at the same logic state, the signal is reduced (or de-emphasized). The net effect is the same at the load end, as the interconnect rolls off higher-frequency components of the signal, leaving the right amount of high- and low-frequency signal for data recovery. Both techniques are proven to extend the reach of the line driver and the choice of one over the other is more related to the technology implemented (CML or LVDS). An 1100 data pattern with de-emphasis is shown in ***Figure 4-1***.

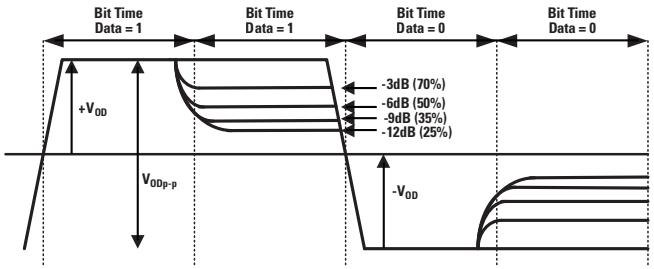

Figure 4-1. Serializer De-Emphasis Waveform (1100 Data Pattern)

Select deserializers also perform signal conditioning functions. Noting the low-pass filtering characteristic of most interconnect media, the receiver input can recover the signal by applying an inverse response or high-pass effect to flatten out the overall link response curve. The equalizer block yields an enhanced eye with less jitter and a greater eye opening for clock and data recovery. Several of the Channel Link II deserializers feature test access points that re-drive the recovered signal to enable the observation of the post equalizer signal. Likewise, the chipset Bit Error Rate Test (BERT) feature can also be used to verify that the link is operating error free.

4.2 Channel Link II Ser/Des Helps to Reduce EMI in Many Ways

Channel Link II chipsets are packed with strong features to help manage EMI on as many fronts as possible. EMI mitigation falls into several categories:

- Differential serial data transmission
- Randomized, Balanced, and Scrambled (RBS) serial coding
- Spread Spectrum Clocking (SSC) TX compatibility
- Spread Spectrum Clock Generation (SSCG) RX (output data and clock) feature
- Output slew rate control (LVCMOS out)
- LVDS parallel inputs/outputs
- Common-mode filter pin

The high-speed signals are sent using a differential data transmission scheme using either an LVDS- or CML-based line driver. In either case, two lines are used per signal with a small signal swing and controlled edge rates to help reduce EMI. This allows for high-speed transmission without generating a large amount of noise. The equal and opposite current flow in the pair also helps to tie up and cancel out certain types of emissions. Great lengths are also taken to maintain balance and symmetry of the signal. These attributes work together to help lower the EMI generated.

As discussed earlier, the RBS encoding also helps to address EMI concerns with its randomization and scrambling features. If the data has a large repeating pattern component or a "beat" to it, this "R&S" feature helps to break it down with a spreading effect that lowers peak emissions.

The serializers are designed to accept slow spread spectrum clocks to aid in reduced system emissions. SSC is usually done in the low kHz range and the serializer Phase-Locked Loop (PLL) will simply track and pass the majority of the spreading (some attenuation will occur along the chain). The net effect is that the serializer is compatible with most SSC clocking schemes. Caution areas include the peak deviation and an excessively fast spreading rate. These should be limited in order to take advantage of the EMI benefits without impacting data recovery.

In many applications, a major point of EMI concern is the wide deserializer output data bus and clock. If this is high speed, a large swing (e.g. 3.3V LVCMOS) over many signals on a wide parallel bus can produce substantial EMI. Channel Link II devices help to mitigate this effect by employing SSCG to spread data and clock transitions over a specified range. Additional options to lower EMI are available, including support for lower I/O supply voltages, down to 1.8V. The output slew rate can also be adjusted to control noise. Certain Channel Link products also support input/output onto an LVDS interface instead of a wide LVCMOS bus. Multiple deserializer devices feature the 4D+C (four data channels plus parallel clock) LVDS interface. This format is known in the industry as Channel Link (I) or also FPD-Link (I) for flat panel display applications.

One last mitigation feature to note is the common-mode filter. This pin provides access to the center point of the 100Ω termination resistor in the serial domain at the deserializer input. This allows placement of a capacitive filter to help shunt off any undesired common-mode noise or for the use of alternate termination schemes. A common-mode voltage or custom impedance to ground can also be applied for additional flexibility.

4.3 Built-In Self Test (BIST) enables Fast and Easy Performance Checks

BIST provides a useful and easy method to determine chipset performance over interconnects without heavy overhead from the system or expensive test equipment. The serializer is configured for a BIST via procedures described in the datasheet. In this mode, it outputs a basic test pattern using a standard PRBS code. The deserializer is also set into this mode, checking the incoming pattern versus a reference and flagging error-free reception. This can be useful in the prototype stage to determine system margin in terms of different interconnect media, interconnect lengths, and/or maximum data rate (within the limits of the chipset). For example, the cable length can be extended until errors are first detected to determine the amount of system margin. Additional external noise sources can be introduced to determine their impact to the link. The BIST may also be invoked by the system to perform a startup test or diagnostics on demand. Reporting modes and operation vary between chipsets. The datasheet should be consulted for additional information.

Key Features

4.4 I/O Options offer Great Flexibility

The Channel Link II Ser/Des family is significantly expanded over the prior generation of Channel Link (I) Ser/Des. The original family supported 5V CMOS and 3.3V LVCMOS interfaces in 21-, 28-, or 48-bit wide parallel buses. A comparison of I/O signaling options is shown in ***Figure 4-2***.

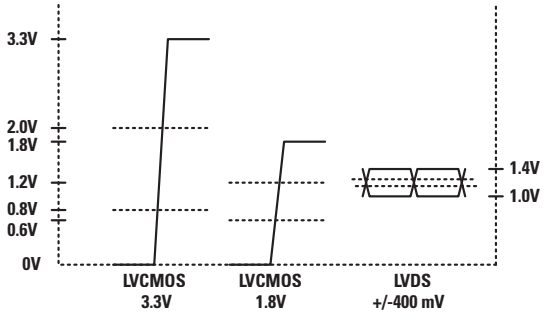

Figure 4-2. Low-Speed Interface Options: 3.3V LVCMOS, 1.8V LVCMOS, and LVDS

4.5 Multi-Link De-Skew

The high-bandwidth, 32-bit versions deploy multiple serial links to scale up bandwidth. Unlike the first generation of Channel Link devices, skew matching between pairs in the picosecond range is no longer required. Each serial link has its own embedded clock signal for data recovery and a wide de-skew capability to re-align the 32-bit data.

This de-skew is performed automatically so no system overhead or intervention is required. ***Figure 4-3*** shows the methodology to measure coarse skew between the serial streams with embedded clocks which is in the nano-second range—see datasheet.

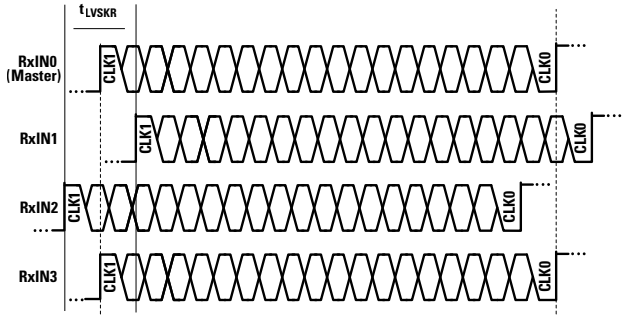

Figure 4-3. Multi-Link De-Skew

4.6 Additional Device-Specific Features

Channel Link II devices also support a variety of other features that offer unique and special capability to systems. Some devices support an auto power-down feature that senses the presence of a clock. If no clock is active, the link will automatically power down and await the return of a clock signal. In the sleep state or power-down mode, certain deserializer devices offer additional options, including holding a certain state or TRI-STATE® at the output pins. The individual datasheets should be consulted for device-specific features.

Cables, Connectors, and Boards

The key aspects of any physical Ser/Des implementation can be broken down into these areas: cables (serial interconnects), connectors, and board layout. This chapter addresses common design criteria for selecting cables and connectors and addresses board-level guidelines for a robust implementation.

5.1 Issues: Skew and Loss

When selecting a serial interconnect, previous generations of Ser/Des required system designers to focus on loss, implement additional control signal lines to transmit SYNC patterns according to the lock status, or perform complex calculations of cable skew margin which included strobe positions, pulse positions, jitter, and cable manufacturer tolerances. Channel Link II Ser/Des simplifies the design process of choosing and implementing high-speed serial interconnects by allowing system designers to focus on two interconnect characteristics—loss, and in some cases, skew.

Most Channel Link II devices serialize a wide parallel bus down to a single serial lane, allowing system designers to focus on intra-pair skew and loss for a differential interconnect solution or only loss for a coaxial solution. The DS92LV3241, DS92LV3242, DS92LV3221, and DS92LV3222 are the current devices in the Channel Link II family that feature two or more serial lanes. However, the DS92LV32xx devices have been improved over the previous generation of Ser/Des in that cable de-skew is performed automatically without any special instruction sequence or command. The de-skew circuit has also been improved such that system designers only need to compare a cable's inter-pair (pair-pair) skew specification to 0.4x the input parallel clock rate to determine if they have sufficient skew margin in their system. This new deskew circuit enables nanoseconds of receiver skew margin, where previous generations of Channel Link devices were limited to picoseconds of skew margin. This topic is discussed in greater detail in application note AN-2007. See the **Tools and References** section for further details.

Channel Link II Ser/Des are equipped with integrated signal conditioning features to assist system designers in addressing cable loss. Some of these signal conditioning features include: Output Differential Voltage (V_{OD}) select, pre-emphasis, de-emphasis, and receive equalization. The device datasheet includes more detailed information on the signal conditioning features of the various devices.

5.2 Reach versus Loss

One of the most common questions asked about Ser/Des devices is, "How far can they transmit data?" The answer to this question depends on many factors. To determine the maximum cable length a Ser/Des can drive, a few variables must first be considered. The most important parameters to consider are the cable type and operating frequency or speed of the serial link.

The cable type will help to determine the loss in dB per unit length. In more complex systems, the cable type can be used to determine the noise margin by investigating the cable crosstalk parameters. The loss per unit length can be found in the cable manufacturer's specifications or measured in a lab. In a lab setting, the easiest way to measure loss per unit length for copper cables is to use a network analyzer. Most network analyzers are easily configured or pre-programmed to measure loss, which can also be designated as insertion loss—S21 for single-ended cables, or SDD21 for differential cables. Once the loss characteristics of the cable are known, they must be compared against the serial line rate.

To determine the serial line rate of a Ser/Des chipset, one must refer to the relevant datasheet. All of the serial line rates for Channel Link II Ser/Des are simple multiples of the input parallel clock rate. Some common parallel clock/serial line rate ratios include:

- 28 x pclk for devices such as the DS92LV2421, DS92LV2422, DS92LV0421, and DS92LV0422
- 16 x pclk for devices such as the DS92LV3241, DS92LV3242, DS92LV3221, and DS92LV3222

Typically, the loss characteristics of cables are specified in terms of a graph illustrating loss in dB versus frequency in Hz. Before comparing the serial line rate to these "loss versus frequency" plots, the serial line rate will need to be converted from Mbps or Gbps to MHz or GHz. Channel Link II Ser/Des use Non-Return to Zero (NRZ) signaling on their serial links. This means that to convert from the serial line rate in bits per second to hertz, the serial line rate is simply divided by two. Consider that the fastest possible rate that the serial lane could toggle, its Nyquist Rate, would be alternating bits of 1's and 0's. Since it takes two bits to create a transition, from either 1 to 0 or from 0 to 1, the rate at which the serial line could toggle will be the serial line rate divided by two.

5.3 PCB Guidelines

When designing a high-speed PCB, the designer should keep the following recommendations in mind:

- Use at least a four-layer board with dedicated power and ground planes
- Use surface-mount components to minimize parasitics
- Separate a single-ended signal from a differential signal by at least three times the differential spacing
- Separate adjacent differential pairs by three times the intra-pair trace spacing
- If vias are required for high-speed data lines, be sure to place vias to ground next to the signal via for a constant return path for the signal
- Route all differential traces as 100Ω differential impedance transmission lines
- Route all single-ended signals as 50Ω impedance lines
- Route all power signals as wide as reasonably possible to minimize inductance
- Use connectors and cables that are designed for high-speed differential data
- Follow the typical connection diagrams found in the datasheet for power-supply filtering recommendations

Please see the **Tools and References** section for additional details.

5.4 Recommended Cable Media

The following cables should serve as a starting point when selecting the appropriate cabling solution for a given system. Other impedance-controlled cables and connectors can be used to achieve various lengths depending on their loss characteristics:

- RJ-45 cable connector with CAT-5/-6/-7
- 50Ω BNC connector with RG-58/U coax
- USB connectors and cables
- IEEE 1394 connectors and cables
- DVI, HDMI, and display port connectors and cables

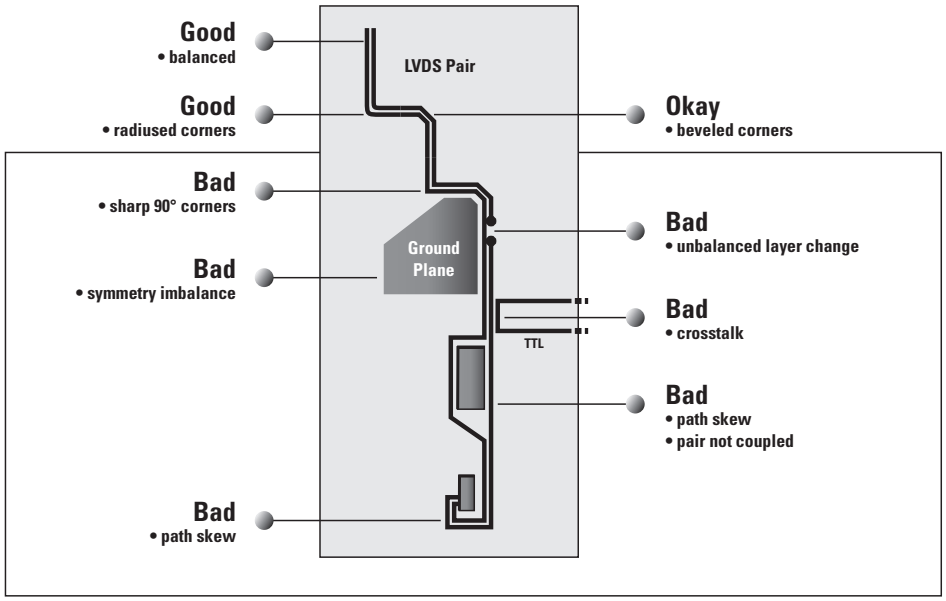

Figure 5-1. PCB Trace Layout Guidelines

6.1 Power

Providing constant, low-noise power to Channel Link II Ser/Des is a key component of the system design. Typical power supply filtering consists of individual 0.1 µF capacitors placed on each power pin, with additional bulk capacitors placed on the PLL power pins and where power is supplied to the board. Ferrite beads are recommended in some cases to help isolate potentially noisy power supply rails. Bypass capacitors and other power-supply filtering recommendations can be found in the device datasheets.

Aside from implementing proper power-supply filtering, system designers should take care to choose the most appropriate regulator for their Ser/Des. Historically, switching power regulators have not been ideal for communication circuits because they can generate noisier output voltage than their Low Drop Out (LDO) regulator counterparts. Usually this noisy or large ripple on the output of the switching regulators is due to a marginal layout.

To simplify the complexities of a switching regulator circuit design and layout, National has introduced the LMZ family of power modules which fully integrates the regulator and critical components such as the shielded inductor within the device package. By consolidating the critical parts of the regulator circuit into a single package, the LMZ family is able to offer peak efficiencies of up to 96%. Since the majority of the components are integrated within a single package, the module can be inserted quickly into a design. Time normally spent on regulator design and layout implementation can now be utilized to focus more on the power distribution network to ensure that output voltage ripple is kept to a minimum. See the **Tools and References** section for details.

The most commonly recommended power solution for high-speed communication systems such as the Channel Link II Ser/Des is the use of LDO regulators. In addition to a wide portfolio of LDOs, National has a line of low-noise LDO regulators that are ideal for Ser/Des systems.

National's low-noise LDO regulators offer wide input voltage range, pre-set or adjustable output voltage levels, and a variety of current sourcing strengths and high Power Supply Rejection Ratios (PSRR). These regulators are simple to design in and require minimal external components. However, the reason that these low-noise LDO regulators are often found in high-speed systems is their excellent PSRR, which can be >74 dB. For additional information on low-noise LDOs, see the **Tools and References** section of this guide.

Finding the right power device that suits a particular system's needs can sometimes be a bit overwhelming. There are a wide variety of power regulators available, each of which has its own strengths and unique circuit implementation. National has developed WEBENCH®, a free, easy-to-use, web-based application, to simplify the power network design process. This tool is particularly handy for regulator circuit design, board-level implementation, and can even be used to help design the power architecture of a complex system. The WEBENCH design tool goes beyond a mere product selection guide; it provides users with schematics, complete order information for a full bill of materials, thermal simulations, efficiency calculation, and board footprints.

For more information on WEBENCH design tools, please refer to the **Tools and References** section of this guide.

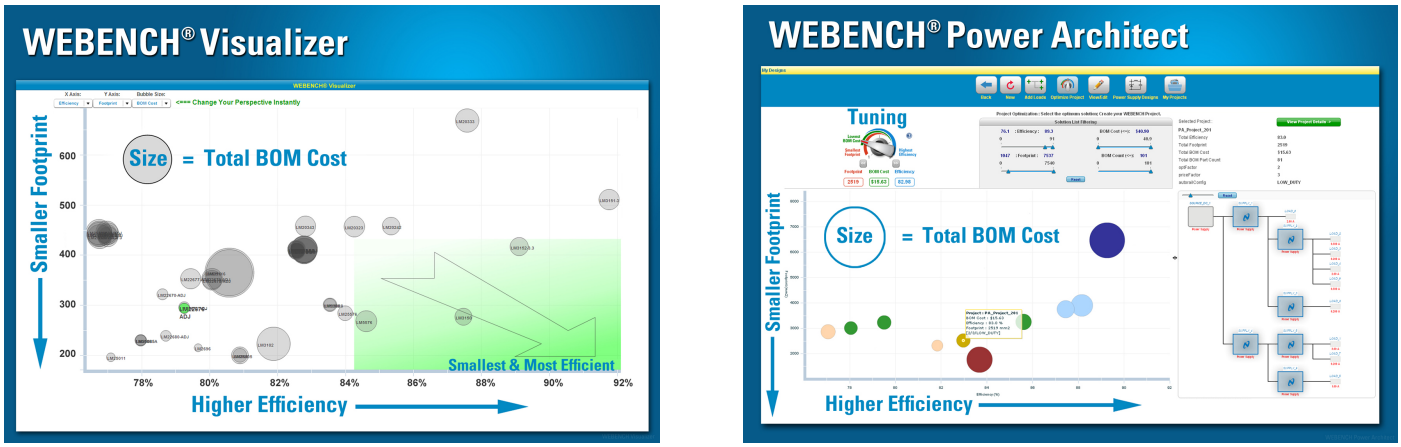

Figure 6-1. WEBENCH Design Tools

Design Tips

7.1 Clocking

Providing a good quality clock is the most important task in developing high-speed Ser/Des systems. For systems that need to communicate over tens of meters of cable, supplying a quality clock is even more important. But what makes a clock good or bad? Most often the quality of a clock is measured by jitter, edge rate, and voltage levels. For exact input clocking requirements, the datasheet should be consulted. However, there are some general guidelines that apply to all Ser/Des systems that should be kept in mind when designing or debugging a high-speed system:

1. **Keep clock jitter to a minimum**

   High-speed serial links often include one or more PLLs and sometimes Clock Data Recovery (CDR) circuit PLLs that can help to mitigate some of the input clock jitter, but will pass through any jitter that is less than the PLL's bandwidth. This jitter travels from the input of the serializer directly to the high-speed serial link and can impair the cable reach and performance of the system. The jitter transferred to the serial transmission line is worsened as the high-speed signal incurs loss across the serial interconnect. If enough jitter accumulates across the serial link, the deserializer will have a difficult time extracting the proper clock information out of the serial data, resulting in bit errors or loss of lock.

2. **Minimize glitches**

   Glitches or spikes can cause problems in a wide range of areas, but they are especially problematic in clock signals. Whether this occurs on the input clock to a serializer or on the SCL line of an I^2C compliant bus, glitches will cause data corruption. Glitches that occur on clock edges are especially problematic because they can cause data to be sampled incorrectly if they occur near the input threshold levels. Often these glitches occur as a result of an improperly configured host device or impedance problems with the signal line.

   Glitches or spikes that occur on the rails of a clock signal are most often attributed to excessive noise in the power supply or within the host clock's generation circuit. To reduce these spikes, a simple first-order R-L or R-C filter can be used. When implementing a filter, it is recommended that the component selection does not overly degrade the edges of the clock signal or input setup and hold violations may be encountered.

3. **Make sure the clock edge rates are appropriate for the data rate**

   Edge rates are an important aspect of any clock signal. The levels of the clock edges define setup and hold times. It is important to make sure that the clocking device is able to adequately drive the clock signal from its output across the board trace and to the input of the serializer. By traveling across the PCB and interfacing with other components before the serializer, the clock signal may degrade. If the edges of the clock become too smooth or rounded, the setup and hold time requirements of the serializer may be violated resulting in improperly sampled data.

   However, the clock device should not be too strong in driving the input clock to the serializer. An over-driven signal can result in under- or over-shoot of the signal, more appropriately named "excursion". This problem can be identified easily by comparing the voltage levels of the clock signal to the input specifications of the serializer. As a general guideline, an input signal should never drop below ground.

7.2 I/O Interfacing

The parallel input and output signals of a high-speed serial link can suffer from a few common signal integrity problems. With LVCMOS parallel I/O, the most common problems that users encounter are:

1. **Setup and hold time violations**

   For the exact timing relationship required between the input clock and data, the datasheet of the Channel Link II device should be consulted. Also, the diagram which defines the setup and hold time should be referenced as it can differ from vendor to vendor or from product to product.

2. **Excessive over-/under-shoot**

   An input signal should never exceed the datasheet minimum or maximum values. If multiple device input pins are driven beyond the datasheet limits for V_{IH} and V_{IL}, the ESD protection circuitry may activate. If this occurs, the input signals will not be sampled correctly and bit errors will occur. To avoid excessive over-/under-shoot, the drive strength of the host device should be reduced, or a series termination resistor near the beginning of

the transmission line should be implemented. I/O Buffer Information Specification (IBIS) models are available for all Channel Link II devices and can help a designer simulate a given board to determine the appropriate resistor value.

With LVDS parallel interfaces, the most common problems that users encounter are:

1. **Poor signal integrity – LVDS termination**

   All Channel Link II devices with an LVDS parallel interface require external 100Ω differential termination resistors on the receive end of the LVDS trace. This means that a differential termination resistor must be placed at the differential inputs to the clock and data inputs for serializers with the parallel LVDS interface, while the deserializer LVDS outputs must have a differential termination placed as close to the receiving device's differential inputs as possible.

2. **Poor signal integrity – differential trace**

   The signal traces routed to and from the LVDS I/O ports of Channel Link II devices must be routed as 100Ω differential traces.

3. **Serializer LVDS receiver skew margin**

   RSKM is budgeted for the amount of inter-pair skew that can be allowed between the clock and any given data pair. RSKM factors in the pulse positions of the LVDS transmitter, jitter, and strobe positions of the LVDS receiver to determine the allowable skew of the traces. Violating the receiver skew margin is similar to violating the setup and hold times of an LVCMOS data input and will result in bit errors. To avoid problems with RSKM, the propagation velocity of the LVDS signal across the PCB trace and any other interconnect in the signal path must first be understood. Next the RSKM value and the propagation velocity is used to calculate the physical inter-pair skew in mils (or mm). With this maximum skew length, margin can be added safely to the system by routing the LVDS pairs to a tighter skew specification.

7.3 Alternate Device Implementations

Most Channel Link II applications utilize the Ser/Des chipset in a point-to-point configuration. However, sometimes there is a need to string multiple receiver links together in a daisy chain or to fan out from a source to multiple destinations. These types of configurations can be performed with Channel Link II devices, as long as a few additional design concerns are addressed.

7.3.1 Daisy Chaining

There are two basic ways to daisy chain links of Channel Link II Ser/Des devices together. The best daisy chain configuration utilizes the loop-through driver of the DS92LV2422 or DS92LV2412 device. The loop-through driver of these Channel Link II deserializers allows the serial stream to be equalized and sent out across the next serial link through the integrated cable driver. It is important to note that the loop-through driver in these Channel Link II deserializers allows the incoming signal to be equalized only and not re-timed or conditioned with de-emphasis. However, the loop-through implementation in these Channel Link II deserializers is sufficient to provide two links of 10m CAT-6 cable at 75 MHz input parallel clock or more links at a reduced parallel clock rate or reduced cable length.

Another method of daisy chaining links together requires the use of an additional chipset for every link after the primary link. There are, however, two primary disadvantages with this system configuration: 1) jitter accumulation and 2) signal integrity issues caused by driving multiple loads from the parallel outputs. Since this implementation requires an additional chipset for each additional daisy chain hop, any jitter that lies within the PLL and CDR bandwidth will pass through to the next chipset where it will be amplified by the jitter transfer characteristics of the serializer and grow larger due to the loss characteristics of the next serial interconnect. If the user needs to send parallel data to an additional device, such as an FPGA or display as well as the serializer for the next daisy chain hop, signal integrity issues may arise. The LVCMOS and LVDS outputs of the Channel Link II deserializer are designed to drive a single point-to-point load. This means that the edge rates and drive strengths of these output drivers were not designed to handle the impedance discontinuities, lower impedance loads, or transmission line stubs for the LVDS drivers. Or in the case of the LVCMOS drivers, this includes the drive strength required to drive high-capacitive loads. For this type of system configuration, buffers must be used.

If achieving multiple daisy chain hops is a critical part of a given system, the DS32ELX0421/DS32ELX0124 FPGA-Link Ser/Des should be considered. The DS32ELX0124 FPGA-Link deserializer has an integrated re-timed loop-through driver with input equalization and output de-emphasis. The re-timer in the loop-through cable driver circuit mitigates the jitter between each daisy chain hop, allowing for large numbers of daisy chain hops.

7.3.2 Fan Out

Fan out can lead to reduced system costs by minimizing PCB board trace and space, decreasing serial interconnects, and saving power. The fan out can occur from a single host to multiple serializers, from a single serializer to multiple deserializers, or from a single deserializer to multiple loads.

If a fan-out configuration involves the parallel LVCMOS or parallel LVDS I/O found in the Channel Link II Ser/Des, then an additional buffer repeater device should be used. If a buffer repeater device is not used, signal integrity problems may arise from lack of drive strength and impedance discontinuities. Any lack of drive strength will result in the softening or rounding of signal edges, interfering with the setup and hold timing of the data. Clock and data signals are worsened by the changes in impedance caused by driving multiple transmission lines and loads. The changing impedance will result in reflections that can further interfere with the signal integrity and timing.

For applications where the receiving systems are in different locations, a fan out of the serial transmission line can be implemented. If only two endpoints are required, the serial outputs of the serializer can be routed and connected as 50Ω, single-ended coaxial lines that run to two different deserializers. In this case, the serial terminal of the serializer will need to be connected to the matching serial input terminal of the deserializer. The unused terminal of the deserializer should be connected to a 0.1 µF capacitor and terminated to ground with a 50Ω resistor. If more than two endpoints are required for a system, then a buffer repeater or crosspoint device can be inserted into the serial data path.

High-speed Ser/Des applications may require flexibility and performance beyond the basic specifications and capabilities of the serializer and deserializer ICs alone. This includes design situations where increased link length or advanced routing topologies are required. These applications necessitate devices capable of enhancing and guaranteeing the integrity of the transmitted signal over longer distances and in diverse environments.

National provides several devices designed with these design requirements in mind, including:

- Cable extenders and buffers
- Crosspoint switches and multiplexers

The purpose of this section is to introduce these solutions and provide suggestions appropriate to individual Channel Link II products.

8.1 Cable Extenders and Buffers

Link lengths beyond several meters can degrade data signal characteristics beyond the point at which they can be reliably recovered at the receiver end. This is due to non-idealities in the source, channel, and receiver. Each introduces noise and signal losses that limit the overall performance characteristics of LVDS systems. Performance is primarily limited by jitter or attenuation and distortion introduced by the transmission media.

Cable extenders, buffers, and equalizers correct for the jitter and attenuation created by the channel. They work to compensate for these undesired effects and restore the signal to a form that can be recovered readily by the receiver (the deserializer).

8.2 Application to Channel Link II Ser/Des

Designs will often require that one or many of the previously mentioned effects be addressed or compensated for in the system. This includes loss and jitter introduced over long links. Use of devices that correct for these undesirable effects is recommended in these situations. A typical example is shown in ***Figure 8-1***.

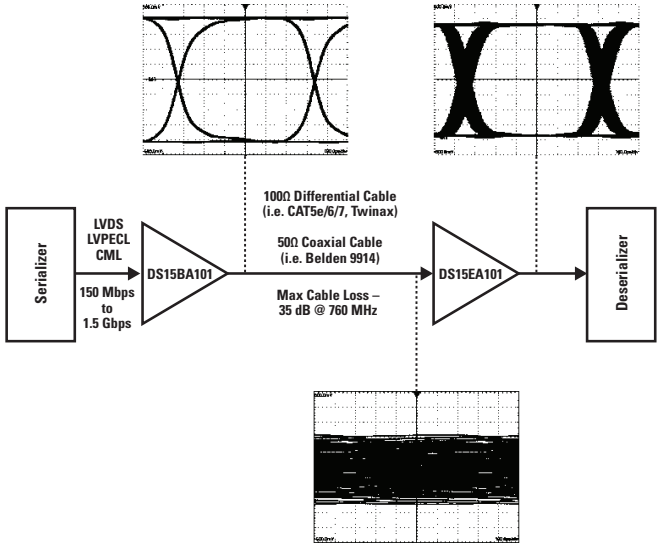

Figure 8-1. Example of a Cable Buffering/Extension Application

National offers several options for Channel Link II cable extension, buffering, and equalization appropriate to the characteristics and throughput of different serializer and deserializer chipsets. A small collection of these products is summarized in ***Table 8-1***.

Product ID	Description	Links	Throughput (Mbps)	Channel Link II Ser/Des Chipset	Notes
DS15EA101	0.15 to 1.5 Gbps adaptive cable equalizer	1	1500	DS92LV0411/DS92LV0412/DS92LV2411/ DS92LV2412	Pair with DS15BA101
DS15BA101	1.5 Gbps differential buffer	1	1500	DS92LV0411/DS92LV0412/DS92LV2411/ DS92LV2412	Pair with DS15EA101
DS25BR100	3.125 Gbps LVDS buffer	1	3125	DS92LV0421/DS92LV0422/DS92LV2421/ DS92LV2422	Pre-emphasis and receive equalization
DS25BR110	3.125 Gbps LVDS buffer	1	3125	DS92LV0421/DS92LV0422/DS92LV2421/ DS92LV2422	Receive equalization
DS25BR120	3.125 Gbps LVDS buffer	1	3125	DS92LV0421/DS92LV0422/DS92LV2421/ DS92LV2422	Pre-emphasis
DS25BR150	3.125 Gbps LVDS buffer	1	3125	DS92LV0421/DS92LV0422/DS92LV2421/ DS92LV2422	Small footprint
DS25BR440	3.125 Gbps quad LVDS buffer	4	3125	DS92LV3221/DS92LV3222/DS92LV3241/ DS92LV3242	Pre-emphasis and receive equalization

Table 8-1. Example of Cable Extension Options for Channel Link II Ser/Des

Complementary Products

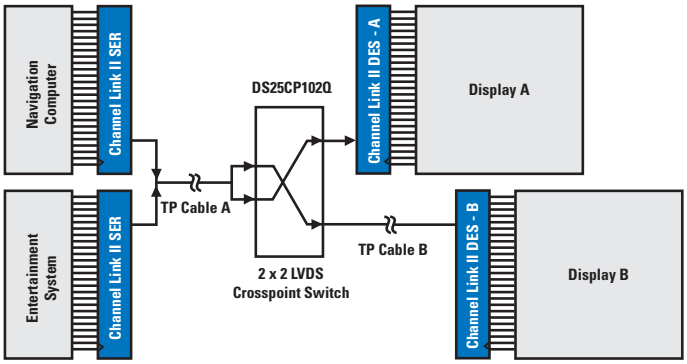

Figure 8-2. Example of a Video Application with Channel Link II and Crosspoint Switching

8.3 Switching and Multiplexing

Certain designs may require routing of signals to and from multiple data sources and sinks. This includes selecting between different data sinks, such as displays or storage devices, or selectively connecting or blocking data streams to enable sharing of a common media. These routing schemes allow efficient use of physical transmission media as well as on-the-fly reorganization of routes and data connections.

For instance, a video display system may require selection between multiple sources of video or the sharing of a video source with another display. This can be accomplished using a device that routes or switches the desired video source to the selected video sink(s) shown in ***Figure 8-2***. Alternatively, one or more of the video sinks can be a storage device such as a hard drive.

Applications requiring routing, switching, or multiplexing of LVDS signals can take advantage of National's portfolio of crosspoint switches and multiplexers. Many incorporate signal conditioning and equalization, offering many of the same advantages seen in other standalone buffer, extender, and equalizer products.

National offers 1x2/2x1 multiplexers or 2x2 and 4x4 crosspoint switches appropriate to the Channel Link II family of Ser/Des products. These devices are summarized in ***Table 8-2***.

Product ID	Description	Links	Throughput (Mbps)	Channel Link II Ser/Des Chipset	Notes
DS25CP114	3.125 Gbps 4x4 LVDS crosspoint switch	4	3125	DS92LV0421/DS92LV0422/ DS92LV2421/DS92LV2422	Pin or SMBus control
DS25CP102	3.125 Gbps 2x2 LVDS crosspoint switch	2	3125	DS92LV0421/DS92LV0422/ DS92LV2421/DS92LV2422	Pin selectable
DS10CP154A	1.5 Gbps 4x4 LVDS crosspoint switch	4	1500	DS92LV0411/DS92LV0412/ DS92LV2411/DS92LV2412	Pin or SMBus control
DS10CP152	1.5 Gbps 2x2 LVDS crosspoint switch	2	1500	DS92LV0411/DS92LV0412/ DS92LV2411/DS92LV2412	Pin selectable

Table 8-2. Examples of Crosspoint Switch Options for Channel Link II Ser/Des

National offers a variety of tools, application notes, and websites to aid in device understanding and design-in support of the Channel Link II Ser/Des family.

Application Note Number	Family	Description	Primary Devices (if applicable)
AN-1807	FPD-Link II	FPD-Link II Display Ser/Des Overview (introduction, typical application, and key feature discussion)	DS90C241/DS90C124, DS90UR241/DS90UR124, DS90UR905/DS90UR906, DS90UR907/DS90UR908
AN-1826	FPD-Link II	Extending the Reach of a FPD-Link II Interface with Cable Drivers and Equalizers	DS90UR241/DS90UR124, DS15BA101/DS15EA101
AN-1898	FPD-Link II	LVDS Repeaters and Crosspoints Extend the Reach of FPD-Link II Interfaces	DS90UR241/DS90UR124, DS25BR1xx/DS25CP10x
AN-1909	Channel Link II, FPD-Link II	DS15BA101 and DS15EA101 Enable Long Reach Applications for Embedded Clock Ser/Des	DS15BA101/DS15EA101
AN-1957	Channel Link II, FPD-Link II	LVDS Signal Conditioners Reduce Data-Dependent Jitter	
AN-2007	Channel Link II	Improving the Robustness of Channel Link Designs with Channel Link II Ser/Des (compares the 32-bit Channel Link II to the prior generation)	DS92LV3241/DS92LV3242, DS92LV3221/DS92LV3222

Table 9-1. Application Notes

9.1 Models

Select devices have IBIS models available to simulate the low-speed side of the Ser/Des devices. IBIS modeling does not support most signal conditioning features of the high-speed side of the devices and thus is not currently modeled. At this time, additional modeling capability is being researched for support of the signal conditioning features. Up-to-date information on signal conditioning high-speed serial-side support can be found on National's website. A complete listing of available IBIS models and other modeling information can be found at:

www.national.com/analog/interface/ibis_home

9.2 Evaluation Platforms

Evaluation boards are available for most Channel Link II chip-sets. Current availability, pricing, and ordering information can be found on National's website. Also within the product folder for each device, a tab is available called "BOARD" for those devices that have evaluation boards. The boards offer easy evaluation and general pin-outs to signals, headers, or connectors for easy access and control of the various device features. Some devices also offer multiple options for power sources.

9.3 Application Notes

Application notes are routinely published and are posted on National's website. ***Table 9-1*** lists application notes that are currently available on Channel Link II or related families.

9.4 Additional Design Guides

In addition to this design guide on National's Channel Link II products, the following design guides are available on National's website:

LVDS Owner's Manual

www.national.com/analog/interface/lvds_owners_manual

Generic information on LVDS interfaces.

Channel Link Design Guide

www.national.com/appinfo/lvds/files/channellink_design_guide.pdf

Design Guide for Channel Link (I) and 21-, 28-, and 48-bit Ser/Des.

Tools and References

9.5 Websites

Please see National's website for the most current information. In addition to product folders, several "feature" sites are also available that are of direct interest to Channel Link Ser/Des.

Ser/Des Feature Site

national.com/serdes

Family information, videos, white papers, and much more….

LVDS/CML Feature Site

national.com/lvds

Selection information, design tools, videos, and much more….

LMZ Power Modules

www.national.com/analog/power/simple_switcher_power_modules#overview

Low-Noise LDOs

www.national.com/analog/power/ldo#low_noise

WEBENCH® Design Tools

national.com/webench

Design, layout, simulation, and more…

Buffers and Crosspoint Switches

national.com/lvds

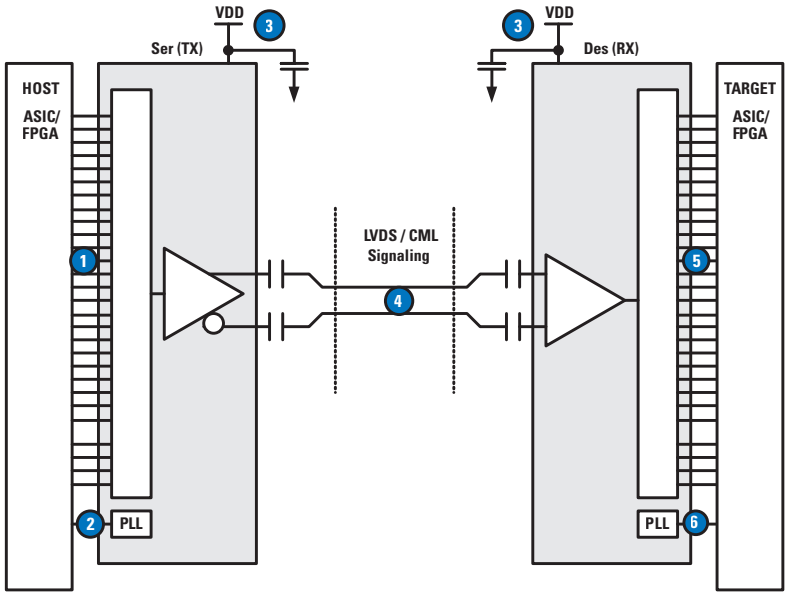

Figure 10-1. Design Review Points

Listed below are some handy tips to check designs for high-performance operation as referenced in ***Figure 10-1.***

1. Data-In Signal Quality

Ensure that the data signal quality presented to the input of the serializer meets datasheet specifications in terms of levels, and also meets the setup and hold times. Excessive overshoot, undershoot, and ring should also be avoided as these tend to add noise. If the source has programmable drive strength, setting data inputs to low drive is usually recommended since they are strobed by the input clock signal.

2. Clock-In Quality

Ensure that the clock signal quality presented to the input of the serializer meets datasheet specifications in terms of levels and jitter specifications. Excessive overshoot, undershoot, and ring should also be avoided as these tend to add noise also. If the source has programmable drive strength, setting the clock input to high drive is usually recommended since the clock signal is edge information and desired to be sharp. Consider termination if the net is long and the driving device supports it.

3. Power Supply Considerations

Excessive supply noise, especially on the PLL supply, can add undesired jitter to the system. Keep supply noise to less than 100 mVp-p especially in the PLL bandwidth range.

4. High-Speed Layout

Where possible, maintain balance and symmetry in the differential pair layout to reduce common-mode conversion.

5. Data-Out Signal Quality

Avoid long traces on the data output lines to avoid transmission line effects. If high fan out is required, consider a fan-out device.

6. Clock-Out Signal Quality

Avoid long traces on the clock output line to avoid transmission line effects. If high fan out is required, consider a fan-out device.

Worldwide Design Centers and Manufacturing Facilities

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ASIA:
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Manufacturing Facilities

Wafer (Die) Fabrication:
Greenock, Scotland
South Portland, Maine

Chip Test and Assembly:
Melaka, Malaysia

World Headquarters
2900 Semiconductor Drive
Santa Clara, CA 95051
USA
+1 408 721 5000
www.national.com

Mailing Address:
PO Box 58090
Santa Clara, CA 95052
support@nsc.com

European Headquarters
Livry-Gargan-Str. 10
82256 Fürstenfeldbruck
Germany
+49 8141 35 0
europe.support@nsc.com

Asia Pacific Headquarters
2501 Miramar Tower
1 Kimberley Road
Tsimshatsui, Kowloon
Hong Kong
+852 2737 1800
ap.support@nsc.com

Japan Headquarters
Beside KIBA
2-17-16
Kiba, Koto-ku
Tokyo, 135-0042, Japan
+81 3 5639 7300
jpn.feedback@nsc.com

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