Application Report
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Receiver Skew Margin for Channel Link I and FPD Link I Devices

Michael Lu

ABSTRACT

One of the most critical parameters for Channel Link I and FPD Link I SerDes performance is Receiver Skew Margin (RSKM). Since data and clock are sent on separate pairs, large pair-to-pair skew can ultimately result in a reduced data throughput during transmission. In this application note, the importance of RSKM is discussed as well as how to calculate and improve overall RSKM in a system application. By optimizing the RSKM between LVDS transmitter and receiver, system designs become less susceptible to bit errors while allowing more margin for cable skew, source clock jitter, and ISI effects.

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1 Introduction

In industrial video applications, FPGAs and ASICs often transfer parallel 18-bit or 24-bit LVCMOS video data across several meters of cable or several inches of PCB trace in order to reach an endpoint display panel or screen. To reduce cable or trace density, improve EMI performance, and resist the effects of a noisy environment, the parallel data is often serialized at the transmitter (Tx) output and then deserialized at the receiver (Rx) input. A typical example of this is shown Figure 1. In this example, a video feed from a security camera interfaces through a cable to a video processor, which is then cabled again to a display panel.

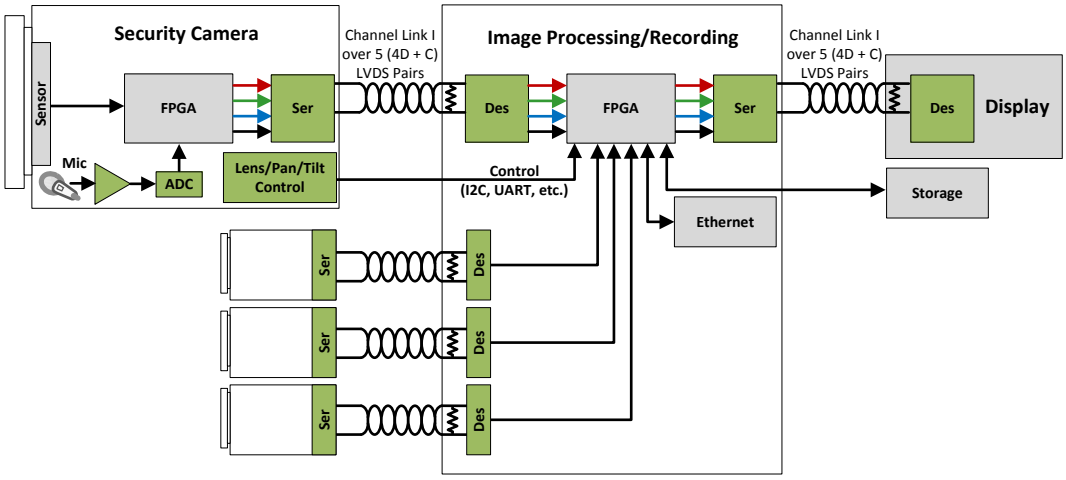

Figure 1. Typical Security Camera Application with Channel Link I Devices

A popular method of serialization is with high speed Low Voltage Differential Signaling (LVDS), where seven LVCMOS bits are serialized per LVDS pair. With this method, four LVDS pairs (3 data, 1 clock) can be used to serialize up to 21 bits of video data (for example, RGB565 or RGB666), while five LVDS pairs (4 data, 1 clock) can be used to serialize up to 28 bits of video data (for example, RGB888).

Traditionally, FPGAs, ASICs, and displays have relied on discrete solutions to perform serialization and deserialization. This type of serialization-deserialization (SerDes) process is addressed by TI's Channel Link I and FPD Link I portfolio, as shown in Figure 2.

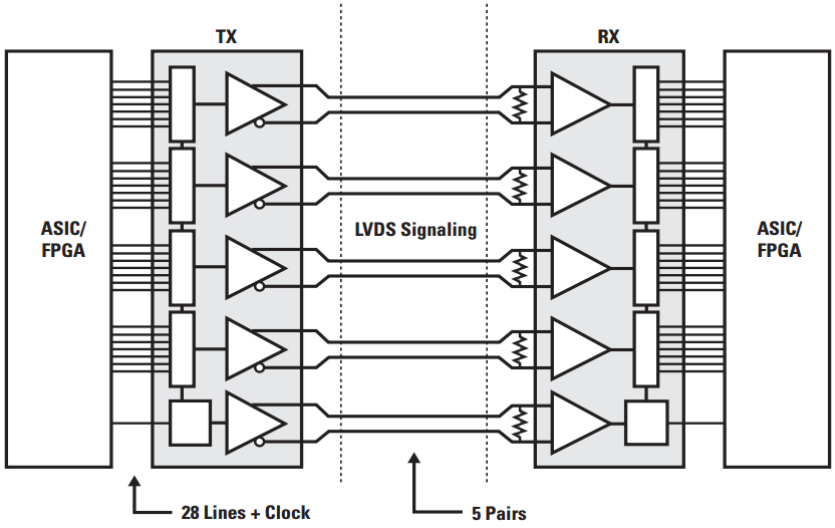

Figure 2. Typical Discrete LVDS SerDes Application with Channel Link I or FPD Link I Tx and Rx Chipset

However, to save board space, FPGAs, ASICs, and displays may integrate the serialization function, deserialization function, or both, on-chip. When designing a high-speed video system, it is possible that two devices with different topologies must interface with one another. If a device that transmits serialized LVDS is required to interface with a device that receives parallel LVCMOS, or vice versa, an OpenLDI-to-RGB (or RGB-to-OpenLDI) bridge converter is required. In this case, a single Channel Link I or FPD Link I Tx or Rx chip can be used as a bridge converter. An example of this application is shown in Figure 3.

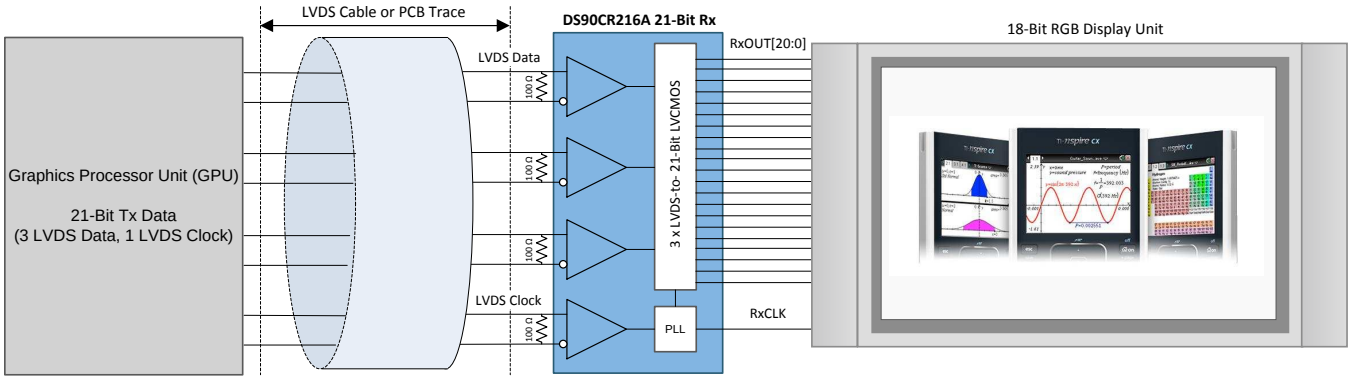

Figure 3. Channel Link I Rx Device Used as a Serial-to-Parallel Bridge

When interfacing an LVDS TxOUT with an LVDS RxIN, a critical parameter for Channel Link I and FPD Link I SerDes performance is Receiver Skew Margin (RSKM). Since data and clock are sent on separate pairs, large pair-to-pair skew can ultimately result in a reduced data throughput during transmission. This application note addresses how to calculate RSKM and how to improve RSKM in system applications by minimizing pair-to-pair skew.

2 How Does the LVDS Rx Strobe Incoming Data?

In order to strobe seven bits within one LVDS clock cycle, an internal PLL within the Rx device locks to the incoming clock with a VCO that operates at f_{CLK} × 7. The internal f_{CLK} × 7 VCO then determines the strobe positions for each of the seven bits following the RxCLKIN rising edge. These strobed inputs are then latched out as parallel data. The internal PLL resynchronizes with the rising clock edge on each new clock cycle. This concept is illustrated with ideal Tx pulse positions and Rx strobe positions in Figure 4.

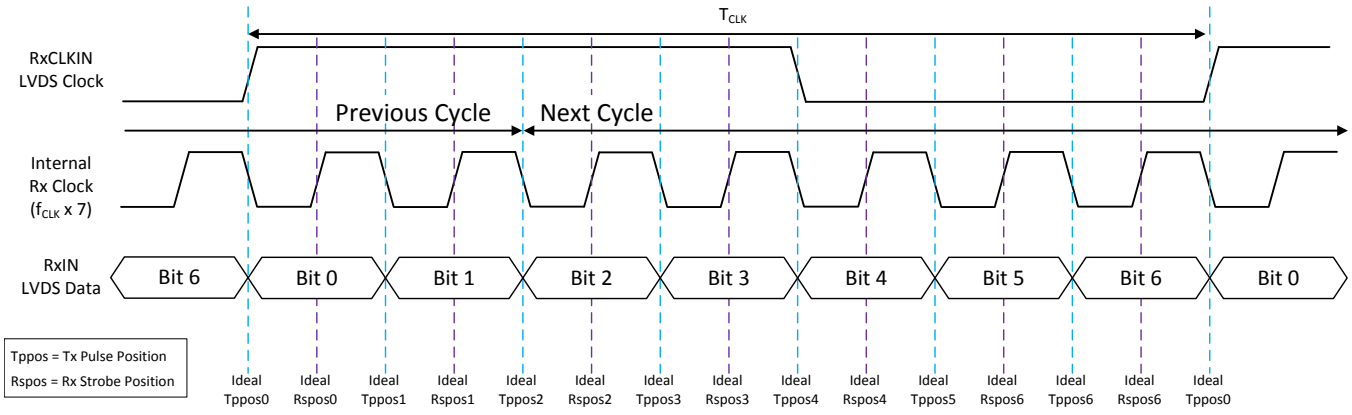

Figure 4. Internal PLL Determines Strobe Positions for the Serialized LVDS Bits

Ideally, each strobe would occur at the center of each data bit. However, the strobe position will be affected by realistic non-ideal effects, such as jitter, temperature drift, and manufacturing variations. Therefore, the Rx strobe position has a window in time for sampling each receive bit, corresponding to a minimum and maximum strobe position.

3 What is RSKM?

Receiver Skew Margin (RSKM) is the maximum amount of skew and jitter that the LVDS receiver can tolerate when sampling input LVDS serialized data. Due to variations in manufacturing process, supply voltage, and operating temperature, LVDS transmitters have minimum and maximum pulse positions for each bit, and LVDS receivers have minimum and maximum strobe positions for sampling each bit. The LVDS receiver samples seven bits per clock cycle, so the skew between the clock and data pairs is critical to ensure that the correct bit value is strobed into the Rx.

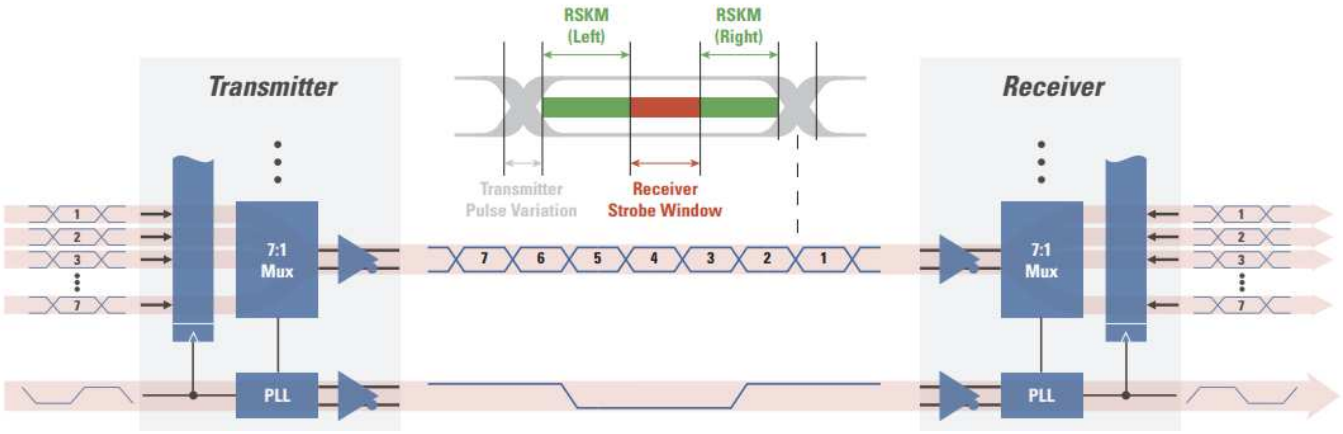

Figure 5. Receiver Skew Margin Illustration

Many SerDes chipset manufacturers define the RSKM value in their datasheets at various operating frequencies. However, the RSKM value can only be defined as a datasheet parameter if both the LVDS transmitter and receiver are produced by the same manufacturer. If the Channel Link I or FPD Link I device is used as a bridge converter and interfaces with a SerDes Tx or Rx from another vendor, it is important to verify that the RSKM between the two interfaces is acceptable. In this case, the RSKM value must be calculated from the datasheet values for Tx pulse position and Rx strobe position.

4 Calculating RSKM

The RSKM is determined by the margin between the Rx bit strobe position and adjacent Tx bit pulse positions, as shown in Figure 6.

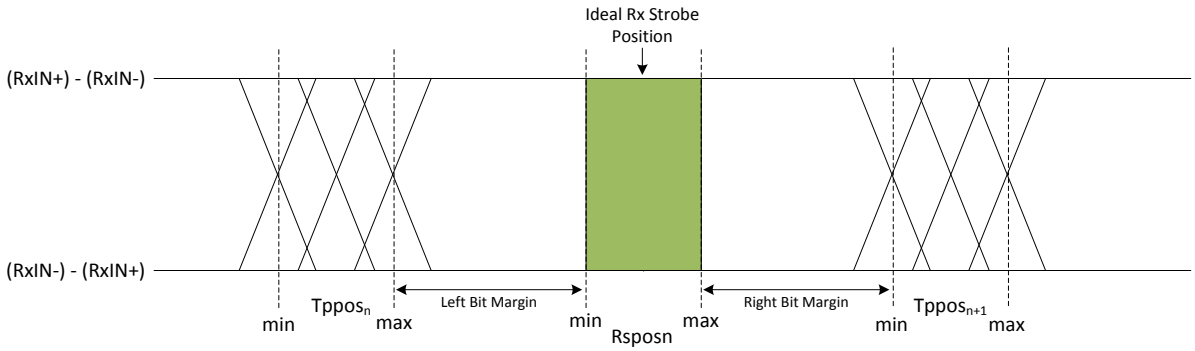

Figure 6. Receiver Skew Margin (RSKM) Defined by Left and Right Bit Margins

Note the following details about this figure:

- Rspos = Rx Input Strobe Position (min and max)
- Tppos = Tx Output Pulse Position (min and max)
- There is a left and right bit margin value associated with each Rx bit strobe position.

The following equations detail how to calculate RSKM based on the datasheet minimum and maximum Tx pulse positions and Rx strobe positions:

$$\text{Left Bit Margin} = Rspos_{n\_min} - Tppos_{n\_max}$$

where

- n = Bit 0..6 (1)

$$\text{Right Bit Margin} = Tppos_{n+1\_min} - Rspos_{n\_max}$$

where

- n = Bit 0..6 (2)

$$RSKM = \min \{\text{All Left Bit Margins, All Right Bit Margins}\} \quad (3)$$

To summarize the RSKM equation, the calculated RSKM is the minimum of all the left and right bit margin values for each of the seven serialized LVDS bits.

5 RSKM Calculation Example

Two RSKM calculation examples are provided in this section. To calculate the overall RSKM, use the equations defined in Equation 1 and Equation 2, then determine the overall RSKM with Equation 3.

5.1 Example 1: DS90CR287 (Tx) and DS90CR288A (Rx)

In the first example, the RSKM is calculated between a DS90CR287 and DS90CR288A chipset. A typical connection diagram is shown in Figure 7.

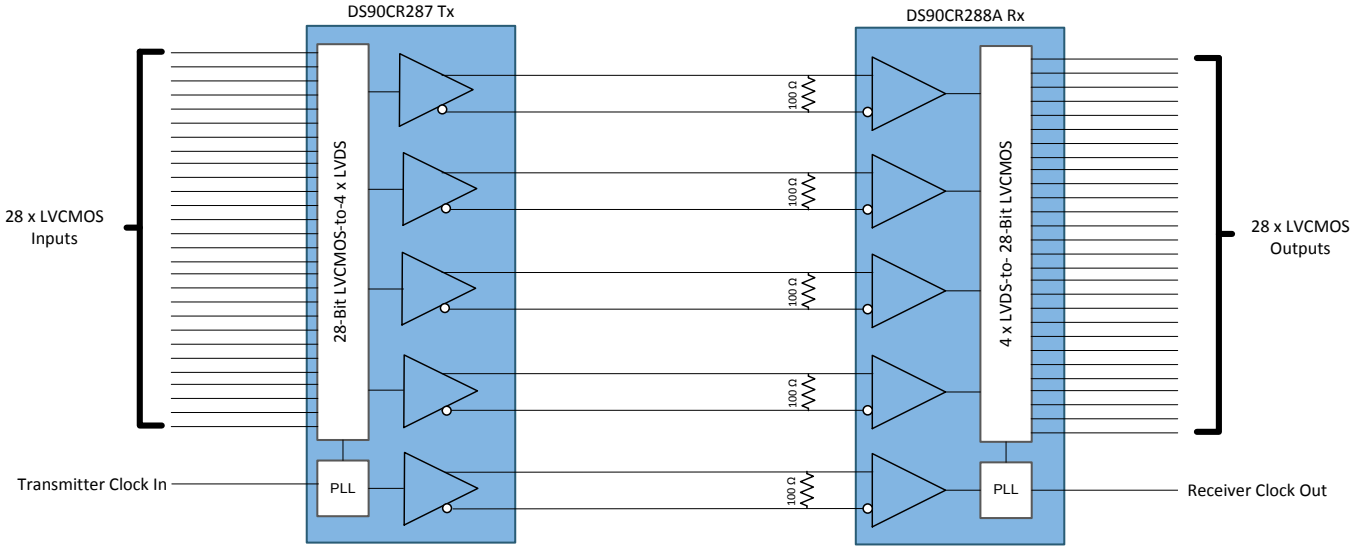

Figure 7. Connection Diagram for DS90CR287 to DS90CR288A

To determine the minimum RSKM value, the Tx pulse positions and Rx strobe positions for the maximum operating frequency should be used. The DS90CR287 Tx pulse positions and DS90CR288A Rx strobe positions for each bit at 85 MHz is provided in Table 1 and Table 2 from the respective datasheets.

Table 1. DS90CR287 Transmitter Pulse Position at f = 85 MHz

PARAMETER		MIN	MAX	UNIT
Tppos0	Transmitter Output Pulse Position for Bit 0	–0.20	0.20	ns
Tppos1	Transmitter Output Pulse Position for Bit 1	1.48	1.88	ns
Tppos2	Transmitter Output Pulse Position for Bit 2	3.16	3.56	ns
Tppos3	Transmitter Output Pulse Position for Bit 3	4.84	5.24	ns
Tppos4	Transmitter Output Pulse Position for Bit 4	6.52	6.92	ns

Table 1. DS90CR287 Transmitter Pulse Position at f = 85 MHz (continued)

PARAMETER		MIN	MAX	UNIT
Tppos5	Transmitter Output Pulse Position for Bit 5	8.20	8.60	ns
Tppos6	Transmitter Output Pulse Position for Bit 6	9.88	10.28	ns

Table 2. DS90CR288A Receiver Strobe Position at f = 85 MHz

PARAMETER		MIN	MAX	UNIT
Rspos0	Receiver Input Strobe Position for Bit 0	0.49	1.19	ns
Rspos1	Receiver Input Strobe Position for Bit 1	2.17	2.87	ns
Rspos2	Receiver Input Strobe Position for Bit 2	3.85	4.55	ns
Rspos3	Receiver Input Strobe Position for Bit 3	5.53	6.23	ns
Rspos4	Receiver Input Strobe Position for Bit 4	7.21	7.91	ns
Rspos5	Receiver Input Strobe Position for Bit 5	8.89	9.59	ns
Rspos6	Receiver Input Strobe Position for Bit 6	10.57	11.27	ns

Note that to calculate the right bit margin for Rspos6, the operating period T must be added to the Tppos0 minimum value. In this example, frequency f = 85 MHz, so period T = 11.76 ns.

Table 3. RSKM Calculation for DS90CR287 and DS90CR288A Pair at f = 85 MHz

PARAMETER		LEFT	RIGHT	UNIT
Rspos0_m	Receiver Strobe Position Margin for Bit 0	0.29	0.29	ns
Rspos1_m	Receiver Strobe Position Margin for Bit 1	0.29	0.29	ns
Rspos2_m	Receiver Strobe Position Margin for Bit 2	0.29	0.29	ns
Rspos3_m	Receiver Strobe Position Margin for Bit 3	0.29	0.29	ns
Rspos4_m	Receiver Strobe Position Margin for Bit 4	0.29	0.29	ns
Rspos5_m	Receiver Strobe Position Margin for Bit 5	0.29	0.29	ns
Rspos6_m	Receiver Strobe Position Margin for Bit 6	0.29	0.29	ns

The RSKM is the minimum of the left and right bit margins across all seven bits. After calculating all bit margins at 85 MHz in Table 3, RSKM = 290 ps. This RSKM value matches the RSKM shown in the datasheet. Therefore, to design a sub-system with the DS90CR287 Tx and DS90CR288 Rx, users must ensure that any remaining jitter sources associated with cable interconnect, clock jitter, or pair-to-pair skew are less than 290 ps in order not to violate the available RSKM.

5.2 Example 2: GPU (Tx) and DS90CR286AT-Q1 (Rx)

In the second example, the DS90CR286AT-Q1 is used as an OpenLDI-to-RGB bridge converter to interface a generic GPU's serialized LVDS outputs to an end display that takes in only parallel RGB. The DS90CR286AT-Q1 is placed on the same board as the GPU, and the DS90CR286AT-Q1 RGB output interfaces via ribbon cable to the display unit. A typical connection diagram is shown in Figure 8.

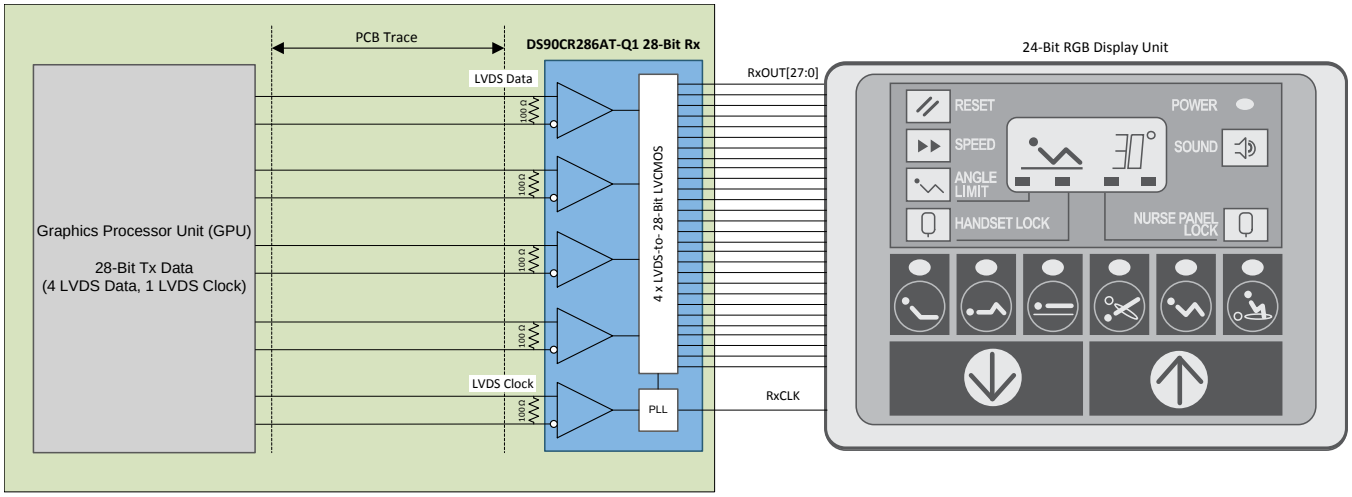

Figure 8. GPU Connection Diagram to DS90CR286AT-Q1 Receiver

To calculate RSKM, the Tx pulse positions and Rx strobe positions are referenced at the desired operating frequency. In this application, the GPU operates at 65 MHz (T = 15.38 ns). The GPU Tx pulse positions and DS90CR286AT-Q1 Rx strobe positions for each bit are provided in Table 4 and Table 5.

Table 4. Example GPU Transmitter Pulse Position at f = 65 MHz

PARAMETER		MIN	MAX	UNIT
Tppos0	Transmitter Output Pulse Position for Bit 0	-0.10	0.10	ns
Tppos1	Transmitter Output Pulse Position for Bit 1	2.10	2.30	ns
Tppos2	Transmitter Output Pulse Position for Bit 2	4.30	4.50	ns
Tppos3	Transmitter Output Pulse Position for Bit 3	6.50	6.70	ns
Tppos4	Transmitter Output Pulse Position for Bit 4	8.60	8.80	ns
Tppos5	Transmitter Output Pulse Position for Bit 5	10.90	11.10	ns
Tppos6	Transmitter Output Pulse Position for Bit 6	13.10	13.30	ns

Table 5. DS90CR286AT-Q1 Receiver Strobe Position at f = 65 MHz(1)

PARAMETER		MIN	MAX	UNIT
Rspos0	Receiver Input Strobe Position for Bit 0	0.58	1.84	ns
Rspos1	Receiver Input Strobe Position for Bit 1	2.81	4.12	ns
Rspos2	Receiver Input Strobe Position for Bit 2	5.08	6.18	ns
Rspos3	Receiver Input Strobe Position for Bit 3	7.21	8.38	ns
Rspos4	Receiver Input Strobe Position for Bit 4	9.37	10.58	ns
Rspos5	Receiver Input Strobe Position for Bit 5	11.61	12.77	ns
Rspos6	Receiver Input Strobe Position for Bit 6	13.82	14.97	ns

(1) Characterization Rx strobe positions are only available at 66 MHz. To determine strobe positions at 65 MHz, calculate the left and right bit margins at 66 MHz assuming an ideal Tx pulse position for each bit. Then, use the same bit margins to estimate the Rx strobe positions with respect to an ideal Tx pulse position for each bit at 65 MHz.

Table 6. RSKM Calculation for GPU and DS90CR286AT-Q1 Application at f = 65 MHz

PARAMETER		LEFT	RIGHT	UNIT
Rspos0_m	Receiver Strobe Position Margin for Bit 0	0.48	0.26	ns
Rspos1_m	Receiver Strobe Position Margin for Bit 1	0.51	0.18	ns
Rspos2_m	Receiver Strobe Position Margin for Bit 2	0.58	0.32	ns

Table 6. RSKM Calculation for GPU and DS90CR286AT-Q1 Application at f = 65 MHz (continued)

PARAMETER		LEFT	RIGHT	UNIT
Rspos3_m	Receiver Strobe Position Margin for Bit 3	0.51	0.22	ns
Rspos4_m	Receiver Strobe Position Margin for Bit 4	0.57	0.32	ns
Rspos5_m	Receiver Strobe Position Margin for Bit 5	0.51	0.33	ns
Rspos6_m	Receiver Strobe Position Margin for Bit 6	0.52	0.32	ns

The RSKM is the minimum of the left and right bit margins across all seven bits. After calculating all bit margins at 65 MHz in Table 6, RSKM = 180 ps, with the minimum value coming from Rspos1_m (Bit 1 right margin).

6 Method to Improve System RSKM

To improve the relationship between Tx pulse position and Rx strobe position, board designers can increase overall RSKM by purposely introducing clock or data skew to shift the Rx strobe position either to the right or left. The timing relationship between the RxCLKIN and Rx strobe position is fixed. Therefore, if RxCLKIN is adjusted so that the input rising edge is delayed, the minimum and maximum Rx strobe positions for each bit will be delayed by the same amount of time. Likewise, if RxCLKIN is advanced, the minimum and maximum Rx strobe positions for each bit will advance by the same amount of time. This timing characteristic becomes useful when there is a desire to *shift* the Rx strobe position in order to center the minimum and maximum strobe position between adjacent Tx pulse positions. By delaying or advancing the LVDS clock pair in time compared to the LVDS data pairs, the Rx strobe positions for each received serialized bit can be shifted in time.

Figure 9 and Figure 10 show, from a timing perspective, how the left and right skew margin can be improved, either by delaying or advancing the LVDS clock in relation to the incoming LVDS data.

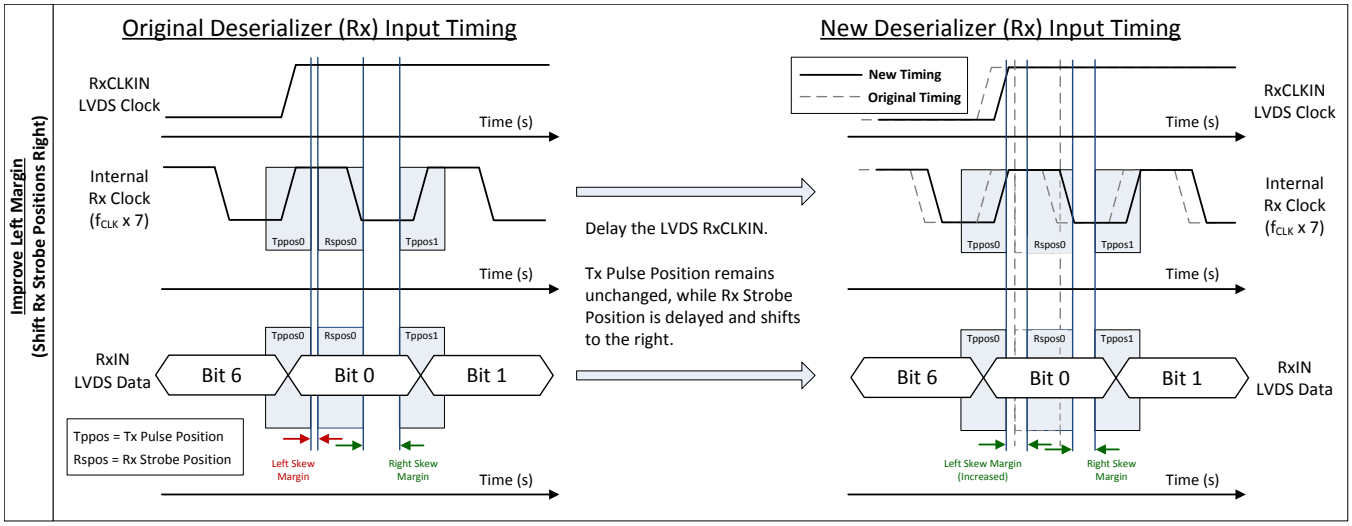

Figure 9. Improving RSKM with Small Left Margin at Receiver Input

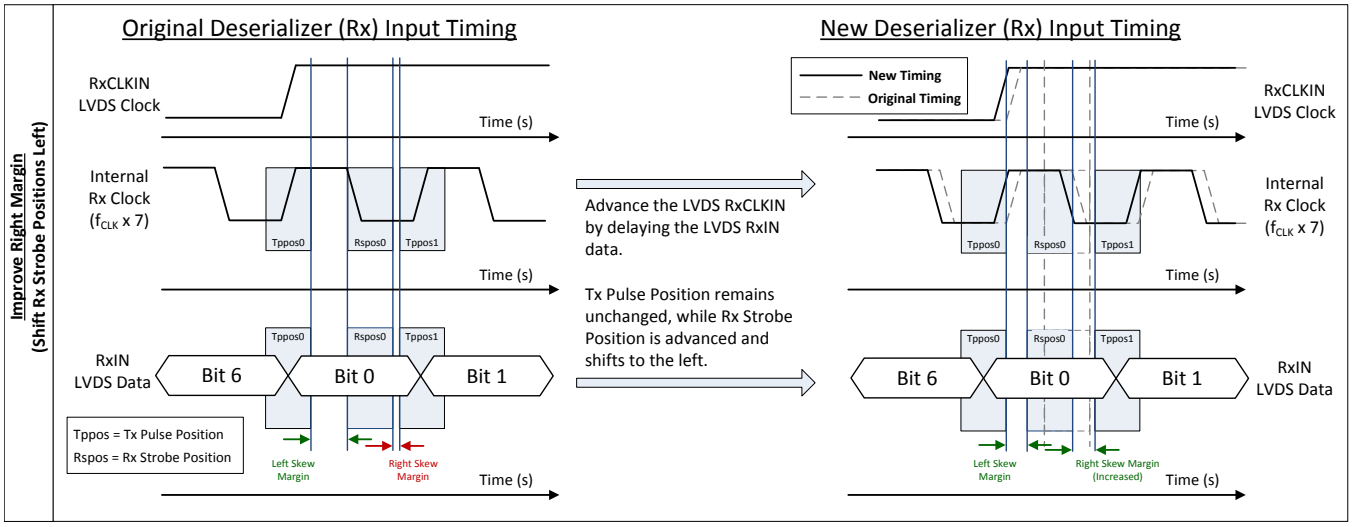

Figure 10. Improving RSKM with Small Right Margin at Receiver Input

In reality, signals can only be delayed. Therefore, to advance the clock, the LVDS data pairs must be delayed uniformly to provide the appearance that the LVDS clock has advanced. A popular method to implement signal delays is by adding PCB trace length between the desired LVDS Tx and Rx pair.

Consider the 180-ps RSKM calculated from Example 2. The margin is weighted unevenly, with the receiver having more left skew margin than right skew margin in Table 6. By advancing the clock compared to the data (in other words, by adding delay to the data), the Rx strobe positions will appear to advance in time. Ultimately, this adjustment will reduce the left skew margin and increase the right skew margin, thereby improving overall RSKM. In Example 2, if the RxIN LVDS data is delayed 150 ps by adding one inch of board trace (typical FR4 board trace delay is approximately 150 ps/in.), RxCLKIN will appear to advance, and the Rx strobe position will shift to the left. The overall effect of this implementation subtracts 150 ps from the left skew margin and adds 150 ps to the right skew margin.

Table 7. RSKM Calculation for Example 2 with RxCLKIN Advanced 150 ps

PARAMETER		LEFT	RIGHT	UNIT
Rspos0_m	Receiver Strobe Position Margin for Bit 0	0.33	0.41	ns
Rspos1_m	Receiver Strobe Position Margin for Bit 1	0.36	0.33	ns
Rspos2_m	Receiver Strobe Position Margin for Bit 2	0.43	0.47	ns
Rspos3_m	Receiver Strobe Position Margin for Bit 3	0.36	0.37	ns
Rspos4_m	Receiver Strobe Position Margin for Bit 4	0.42	0.47	ns
Rspos5_m	Receiver Strobe Position Margin for Bit 5	0.36	0.48	ns
Rspos6_m	Receiver Strobe Position Margin for Bit 6	0.37	0.47	ns

As shown in Table 7, the RSKM improves significantly by advancing RxCLKIN by 150 ps, going from 180 ps to 330 ps of overall RSKM, with the minimum value now coming from Rspos0_m (Bit 0 left margin) and Rspos1_m (Bit 1 right margin).

7 Other Factors that Affect Link Margin

While RSKM accounts for the effects of non-ideal LVDS Tx output pulse positions and Rx input strobe positions, cable skew and clock jitter are not included in the RSKM specification and should be subtracted from the RSKM value to determine the final available link margin. To improve the final available link margin, LVDS buffers and repeaters such as the DS90LV001, DS90LV804, DS10BR150, and DS25BR150 can be used to address non-ideal interconnect media attenuation and jitter between LVDS transmitters and receivers.

For error-free transmission, ensure that RSKM ≥ Cable Skew + Source Clock Jitter + ISI (Inter-Symbol Interference). Optimization of RSKM directly improves the allowable margin for cable skew, source clock jitter, and ISI related to the device interconnect. For additional background details about RSKM and ways to mitigate other sources of margin reduction, refer to Application Note SNLA050.

8 Summary

In this application note, the importance of RSKM was discussed as well as how to calculate and improve overall RSKM in a system application involving two different LVDS SerDes vendors. While RSKM can be guaranteed by datasheet specification when both the transmitter and receiver are released as a chipset by the same manufacturer, RSKM must be calculated when two different vendors interface with one another to ensure timing compatibility. By optimizing the RSKM between LVDS transmitters and receivers, systems become significantly less susceptible to bit errors while allowing more margin for cable skew, source clock jitter, and ISI effects.

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