Functional Safety FIT Rate, FMD and Pin FMA TLV7041-Q1

1 Overview

This document contains information for TLV7041-Q1 (SC70 (5) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards

Figure 1 shows the device functional block diagram for reference.

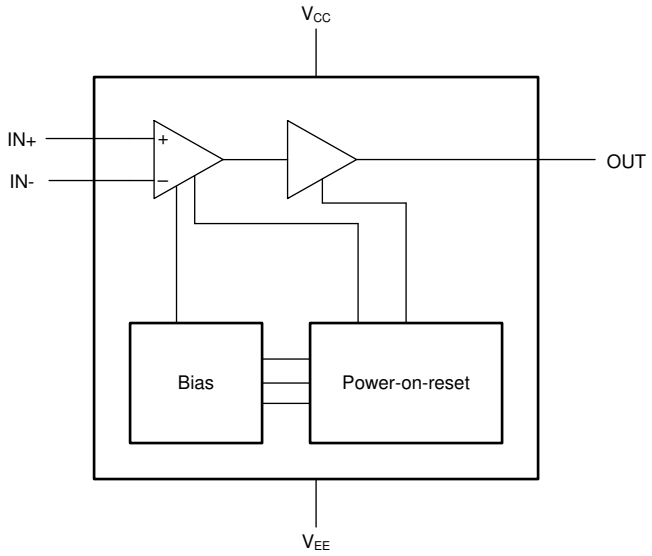

Figure 1. Functional Block Diagram

TLV7041-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLV7041-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 0.1 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS Operational Amp, Comparators and Voltage Monitors	4 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLV7041-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (HIZ)	15%
OUT saturate high	25%
OUT saturate low	25%
OUT functional not in specification	30%
Short circuit any two pins	5%

The FMD in Table 3 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLV7041-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to supply (see Table 7)
- Pin short-circuited to an adjacent pin (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

shows the TLV7041-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLV7041-Q1 datasheet.

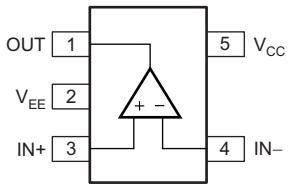

Figure 2. Pin Diagram

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin No.	Pin Name	Damage	Functionality	Description of Potential Failure Effect(s)	Failure Effect Class
1	OUT	No	Yes	No change if GND pin is GND node	B
2	VEE	No	Yes	No change if same node as GND	D
3	IN+	No	Yes	Output goes low, if other input is positive	C
4	IN-	No	Yes	Output goes high, if other input is positive	C
5	VCC	No	No	Main supply shorted out (no power to device)	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin No.	Pin Name	Damage	Functionality	Description of Potential Failure Effect(s)	Failure Effect Class
1	OUT	No	Yes	Output can't drive application load	B
2	VEE	Possible	Affected	Lowest voltage pin will drive GND pin internally (via diode)	B
3	IN+	No	Yes	Output may be low or high	C
4	IN-	No	Yes	Output may be low or high	C
5	VCC	No	No	Main supply open (no power to device)	B

Table 7. Pin FMA for Device Pins Short-Circuited to VCC

Pin No.	Pin Name	Damage	Functionality	Description of Potential Failure Effect(s)	Failure Effect Class
1	OUT	Possible	Yes	Thermal stress due to high power dissipation	B
2	VEE	No	No	Main supply shorted out (no power to device)	B
3	IN+	No	Yes	Output goes high, if other input is less positive	C
4	IN-	No	Yes	Output goes low, if other input is less positive	C
5	VCC	No	Yes	No change if same node as VCC	D

Table 8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin No.	Pin Name	Damage	Functionality	Description of Potential Failure Effect(s)	Failure Effect Class
1 to 2	OUT to VEE	Possible	Yes	No change if GND pin is GND node	B
2 to 3	VEE to IN+	No	Yes	Output goes low, if other input is positive	C
3 to 4	IN+ to IN-	No	Yes	Output may be low or high	C
4 to 5	IN- to VCC	No	Yes	Output goes low, if other input is less positive	C
5 to 1	VCC to OUT	Possible	Yes	Thermal stress due to high power dissipation	B

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