Application Brief

Space-Grade, 100-krad, Isolated Serial Peripheral Interface (SPI) LVDS Circuit

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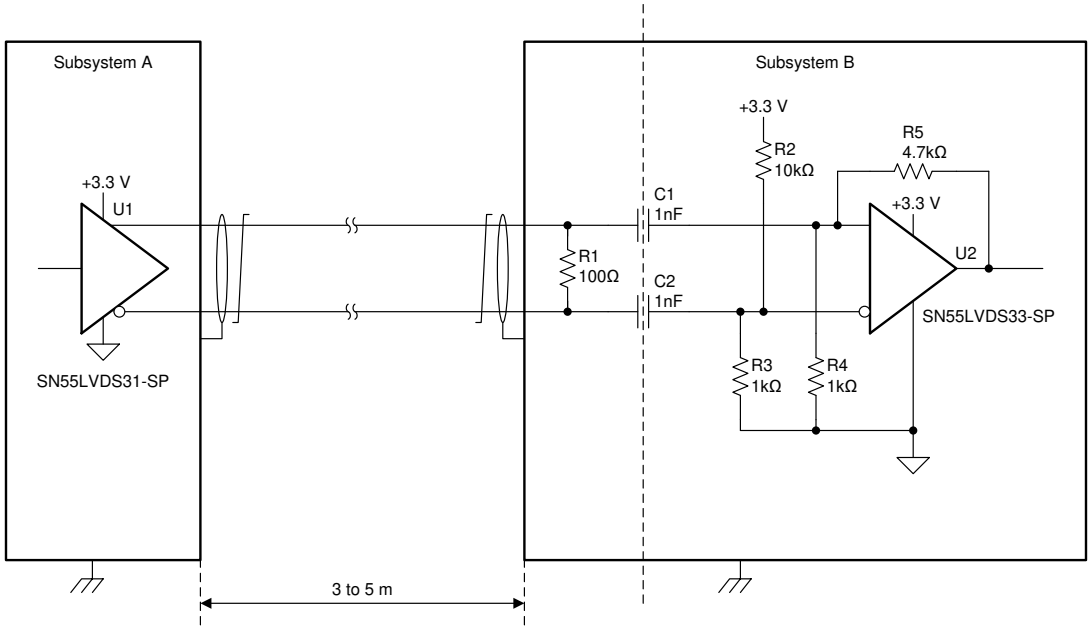
Design Goals

Parameter	Design Requirement
Maximum Bit Rate	≥ 100 kbit/s
Isolation Voltage	≥ ±100 V
Maximum Cable Length	≥ 5 m
Maximum Total Ionizing Dose	≥ 100krad (Si)
Maximum SEL	≥ 75MeV-cm^2/mg

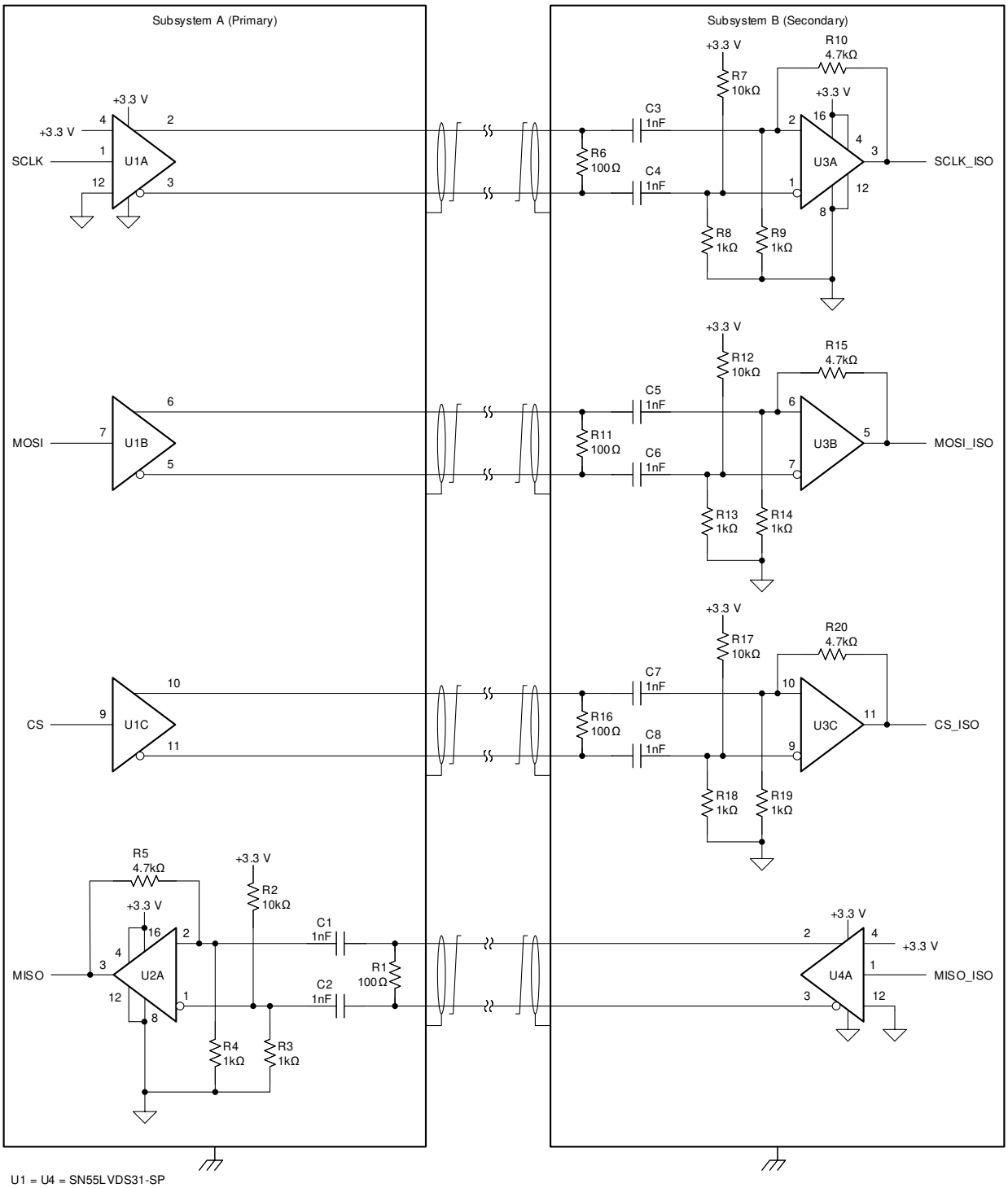
Design Description

The Serial Peripheral Interface (SPI) is commonly used in embedded systems to connect microcontrollers to peripheral devices such as ADCs and DACs. It is often used in spacecraft applications, and sometimes an isolated SPI implementation is necessary to preserve the spacecraft grounding principles or to support DC offsets. The following circuit uses the SN55LVDS31-SP and SN55LVDS33-SP RS-422 driver and receiver devices to implement one channel of an isolated SPI. Isolation is provided by the AC-coupling capacitors, whose voltage rating determines the level of isolation supported.



Complete SPI Implementation

The following image is a typical four-signal SPI implementation. The circuit shown uses the SN55LVDS31-SP and SN55LVDS33-SP devices and a 3.3-V supply voltage.



U1 = U4 = SN55LVDS31-SP
U2 = U3 = SN55LVDS33-SP
Decoupling capacitors and unused gates not shown.

Design Notes

The circuit biases the negative input of each receiver channel slightly above ground. Positive feedback changes the bias point of the positive input depending on the output state of the receiver. When the output is high, the positive input is biased higher than the negative input; when the output is low, the positive input is biased lower than the negative input. In this way, the receiver always remains in the last state that it was actively driven to. The time constant of the AC-coupling circuit is irrelevant, and there is no minimum operating frequency.

Receiver Function Table

SN55LVDS33-SP Function Table

Differential Inputs	Enables		Outputs
$V_{ID} = V_{(A)} - V_{(B)}$	G	$\overline{G}$	Y
$V_{ID} \geq 50$ mV	H	X	H
	X	L	H
$V_{ID} \leq -50$ mV	H	X	L
	X	L	L
X	L	H	Z

Isolation

Isolation is provided by the AC-coupling capacitors. These should be chosen with a voltage rating greater than the isolation voltage required. For improved failure tolerance, two capacitors in series can be used; however, *each capacitor must be rated for the full isolation voltage*.

Design Steps

In the following description the component reference designators referred to are those used in the circuit diagram on the first page of this document.

- Choose R1 to match the characteristic impedance of the cable used. In this case, with 24 AWG twisted pair cable, R1 = 100 Ω.
- Choose R2 and R3 so that when the output is low the differential input voltage is ≤ –50 mV. When the output is low the voltage on the positive input is 0 V and the voltage on the negative input is given by the following equation:

$$V_{I(-IN\ A)} = \left(\frac{R_3}{R_2 + R_3}\right)3.3\,V = \left(\frac{1\,k\Omega}{10\,k\Omega + 1\,k\Omega}\right)3.3\ V = 300\ mV$$

  This yields the following equation for the differential input voltage:

$$V_{ID-} = V_{(+IN\ A)} - V_{(-IN\ A)} = 0\ mV - 300\ mV = -300\ mV$$

- Choose R4 and R5 so that when the output voltage is high, the differential input voltage is ≥ 50 mV. When the output is high the voltage on the positive input is given with the following equation:

$$V_{I(+IN\ A)} = \left(\frac{R_4}{R_4 + R_5}\right)3.3\,V = \left(\frac{1\,k\Omega}{1\,k\Omega + 4.7\,k\Omega}\right) = 579\ mV$$

  Therefore, the following equation shows the differential input voltage:

$$V_{ID+} = V_{(+IN\ A)} - V_{(-IN\ A)} = 579\ mV - 300\ mV = 279\ mV$$

- C1 and C2 set the time constant of the AC-coupling network. If this time constant is long enough to cause the receiver to change state, the absolute value of the AC-coupling time constant is unimportant. The positive feedback network formed by R5 ensures that the receiver stays in the last state it was actively driven to, and thus the minimum operating frequency is independent of the values of C1 and C2.

  The time constant of C2, R2, and R3 is given in the following equation:

$$\tau_{(-IN\ A)} = \left(\frac{R2 \times R3}{R2 + R3}\right)C2 = 909\ ns$$

  The time constant of C1, R4, and R5 is given in the following equation:

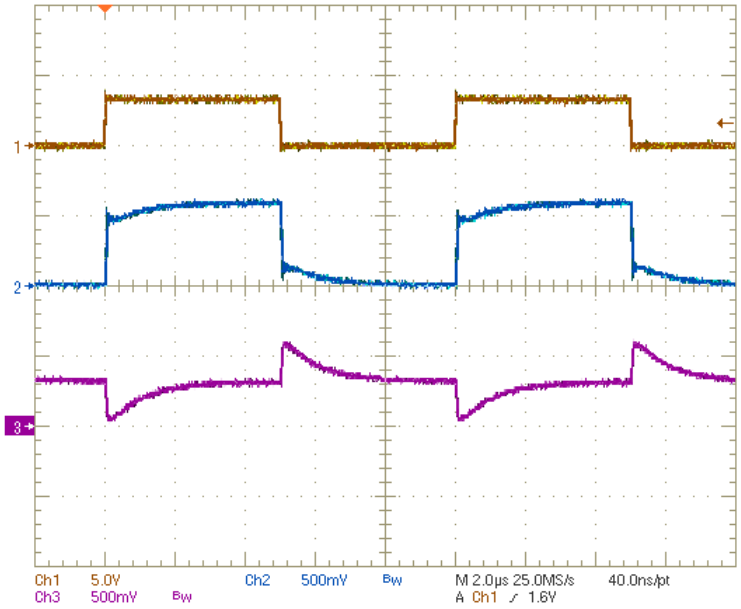
$$\tau_{(-IN\ A)} = \left(\frac{R4 \times R5}{R4 + R5}\right)C1 = 825\ ns$$

- Choose capacitors C1 and C2 with a voltage rating that exceeds the isolation voltage required. For fail-safe circuits, two capacitors in series can be used; however, each individual capacitor must be rated for the full isolation voltage.

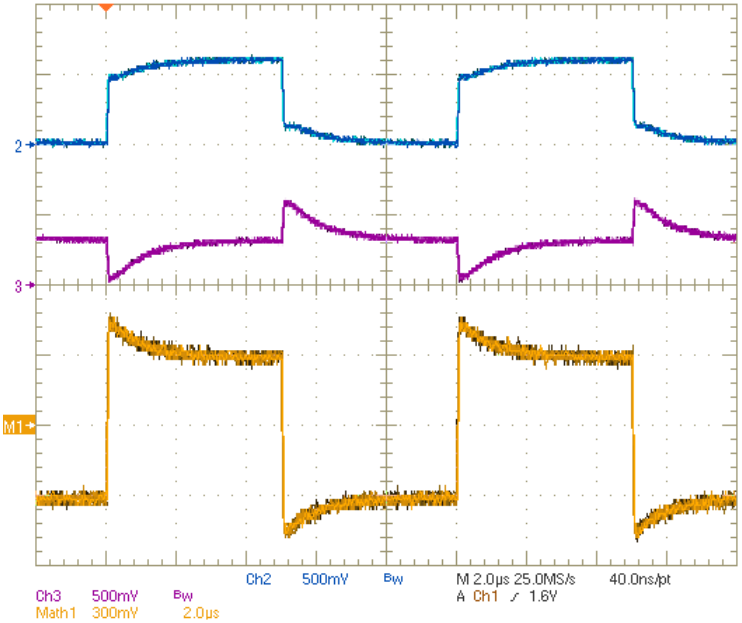
Measurement Results

LVDS-based circuit

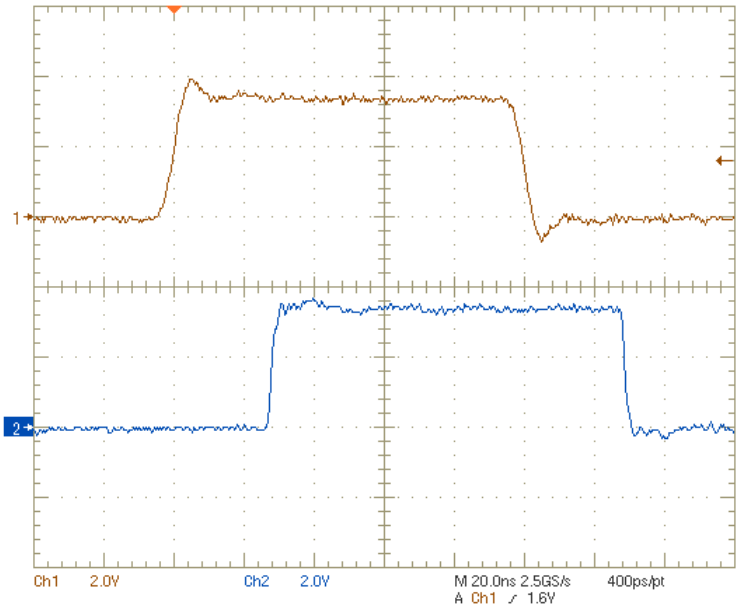
The following scope plot shows the input and output signals measured directly at the receiver input pins after transmission over a 5-m length of 24-AWG twisted-pair cable. Channel 1 shows the driver input signal and channels 2 and 3 the positive and negative inputs of the differential receiver. The hysteresis generated at the positive input of the receiver can be seen in the different quiescent levels to which the input returns after the initial capacitive *kick*. In contrast, the inverting input, which does not have hysteresis, returns to the same quiescent level. This approach ensures that the receiver output remains in the last state to which it was driven and that the minimum switching frequency is independent of the time constant of the AC-coupling components.



The following scope plot shows the waveforms at positive and negative inputs of the receiver (channels 2 and 3, respectively) and the differential signal resulting from them (channel M1).



The following scope plot shows the propagation delay from the input of the driver to the output of the receiver. The propagation delay is about 30ns.



Design References

Design Featured LVDS Transmitter

SN55LVDS31-SP	
Interface Standard	LVDS
# Transmitter Channels	4
# Receiver Channels	0
Nominal Supply Voltage	3.3 V
Operating Temperature Range (T_A)	–55°C to 125°C
Maximum Total Ionizing Dose	150 krad (Si)
Maximum SEL	110 MeV-cm^2/mg
www.ti.com/product/sn55lvds31-sp	

Design Featured LVDS Receiver

SN55LVDS33-SP	
Interface Standard	LVDS
# Transmitters	0
# Receivers	4
Nominal Supply Voltage	3.3 V
Common-Mode Voltage Range	–4 V to 5 V
Operating Temperature Range (T_A)	–55°C to 125°C
Maximum Total Ionizing Dose	100 krad (Si)
Maximum SEL	90 MeV-cm^2/mg
www.ti.com/product/sn55lvds33-sp	

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