LMK00725EVM User’s Guide

User's Guide

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1 Introduction

The LMK00725 is a low skew, high performance clock fanout buffer, which distributes up to five 3.3 V LVPECL outputs. The clocks are derived from one of two selectable inputs, which can accept differential or single-ended input signals.

This evaluation module (EVM) is designed to demonstrate the functionality and electrical performance of the LMK00725 device. For optimum performance, the board is equipped with 50-ohm SMA connectors and 50-ohm controlled impedance traces.

Table 1. Device and Package Configurations

DESIGNATOR	IC	PACKAGE
U1	LMK00725	PW-20 (TSSOP 20 pin)

2 Features

- Easy to use evaluation board to fan-out up to five LVPECL clocks with low phase noise/jitter
- Accepts differential or single-ended/LVCMOS input clock
- Device control pins configurable through jumpers
- Board power at 3.3-V for VCC

3 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the LMK00725EVM.

With this EVM, one could distribute one of two input clocks to up to 5 LVPECL outputs. Therefore, a minimum of one clock source is needed and appropriate test equipment to observe or measure the outputs.

3.1 Input/ Output Connector Description

Connectors:

- **CLK0** and **nCLK0** SMA connectors are used to interface an external AC-coupled clock input to the first of the two differential input pairs (CLK0, nCLK0) of the device.
- **CLK1** and **nCLK1** SMA connectors are used to interface an external AC-coupled clock input to the second of the two differential input pairs (CLK1, nCLK1) of the device..
- **Q1**, **nQ1** and **Q3**, **nQ3** SMA connectors are used to distribute two of the five differential clock outputs. The other three differential clock outputs are not connected to the traces, so their SMA connectors are not populated by default.
- **PWR** is a 3-pin header used to 3.3-V supply power to the board/device. VCC and GND pins are labeled on the top side of the board. The center pin is not connected (N/C).

Jumpers:

- **CLK-SEL** selects between one of two inputs.
  - 0 (position 1-2) = Select CLK0, nCLK0 inputs
  - 1 (position 2-3) = Select CLK1, nCLK1 inputs
- **CLK-EN** selects between U1 clock enabled or disabled modes.
  - 0 (position 1-2) = Clock Disabled
  - 1 (position 2-3) = Clock Enabled (normal operation)

4 Operation

Power:

Before, applying any clock inputs, supply the board with 3.3 V and ground at VCC and GND pins of the PWR header. Make sure the supply current being drawn is less than 115 mA.

Inputs:

Figure 1 shows the LMK00725 input structure. The internal 51 kΩ pull-up and pull-down resistors work with the external 50 Ω termination resistors, which bias the device inputs to mid-rail. Therefore, AC-coupled clock sources from 0.15Vpp to 1.3Vpp (50 Ω terminated) can be tied to either of the two differential clock inputs. With the default input termination shown in Figure 1, the input SMAs expect a 10 0Ω differential clock source. Note that with the default input configuration, the differential input has only very small offset voltage (~3.2 mV) so that when the selected clock inputs are left open/floating, the outputs could have the tendency to chatter.

With DC-coupled clock sources, use a “DC-block” at the input SMAs to ensure DUT input voltage range compliance. Alternatively, adjust the clock source DC bias (if available) to make sure the LMK00725 input voltage range is not violated.

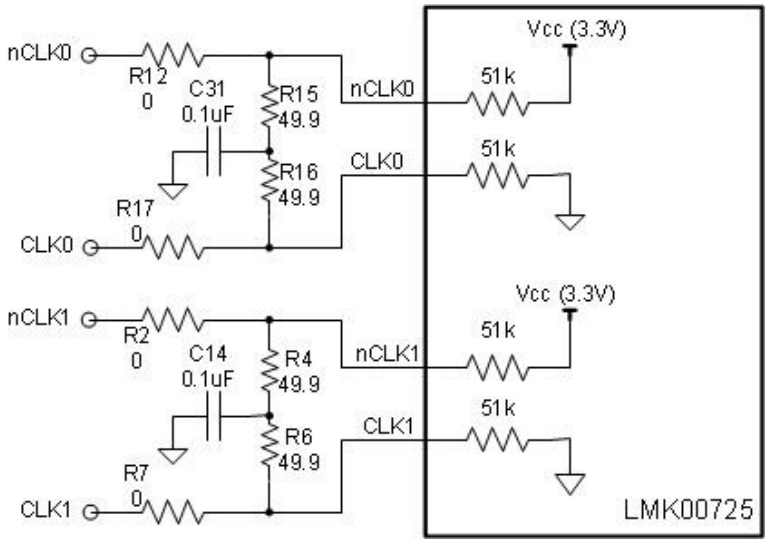

Figure 1. LMK00725 Input Structure and Default Input Termination

The clock inputs can accommodate a differential input or single-ended input signal with the proper external input termination using the various component options on the board. Refer to the datasheet for input interface application circuits.

To achieve the best possible additive jitter and noise floor performance, it is recommended to drive the CLK/nCLK pair using an input signal with fast slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate can degrade the additive jitter and noise floor performance. For this reason, a differential input signal (e.g. LVPECL), is recommended because it typically provides higher slew rate and common-mode noise rejection compared to a single-ended input (LVCMOS/LVTTL or sine-wave, for example).

Outputs:

By default, two of the five LVPECL output pairs are connected to the traces and SMA connectors via series 0-Ω resistors. The remaining three LVPECL pairs are not connected to the traces (0-Ω resistors not installed) and thus do not have SMA connectors installed. The routed outputs have 180-Ω bias resistors to ground and are AC-coupled to the SMA connectors to allow direct connections to RF instruments via SMA cables for test and evaluation. The AC-coupled outputs should be terminated with single-ended 50 Ω or 100 Ω differential loads.

To minimize reflections and signal integrity issues, it is recommended to terminate any driven output trace with a 50-Ω SMA load termination, or otherwise disconnect any unused output from the trace by removing the 0-Ω series resistor (R30 to R39).

5 PCB Layout

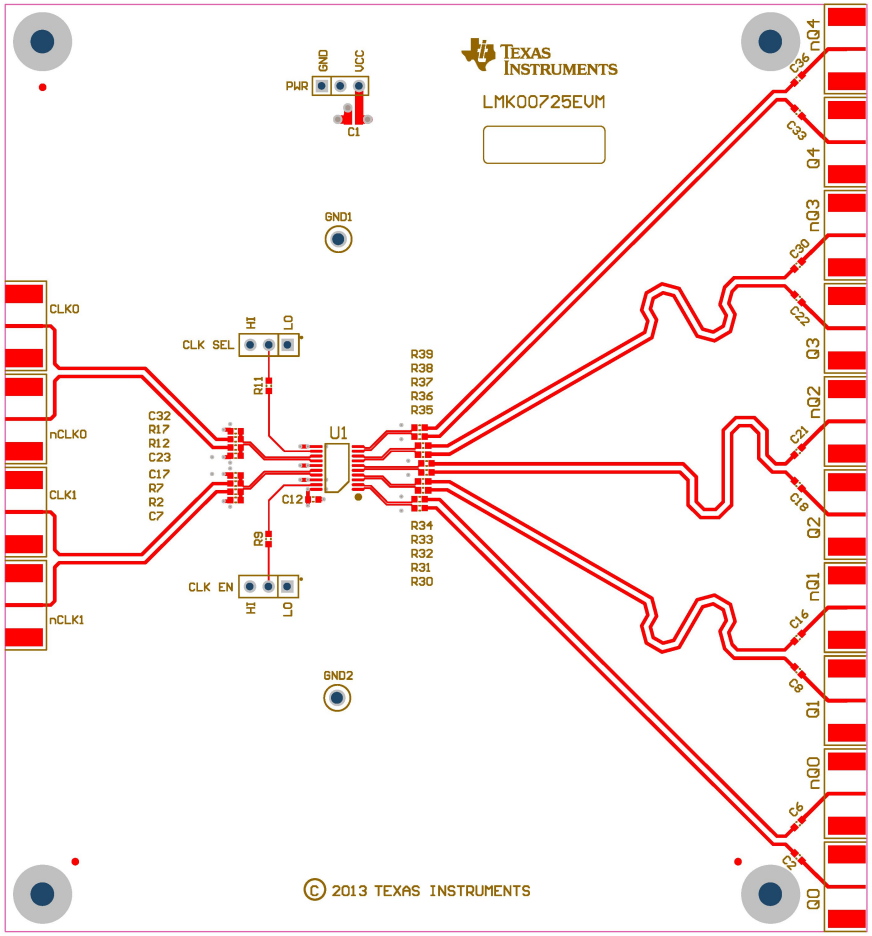

Figure 2. Top Layer

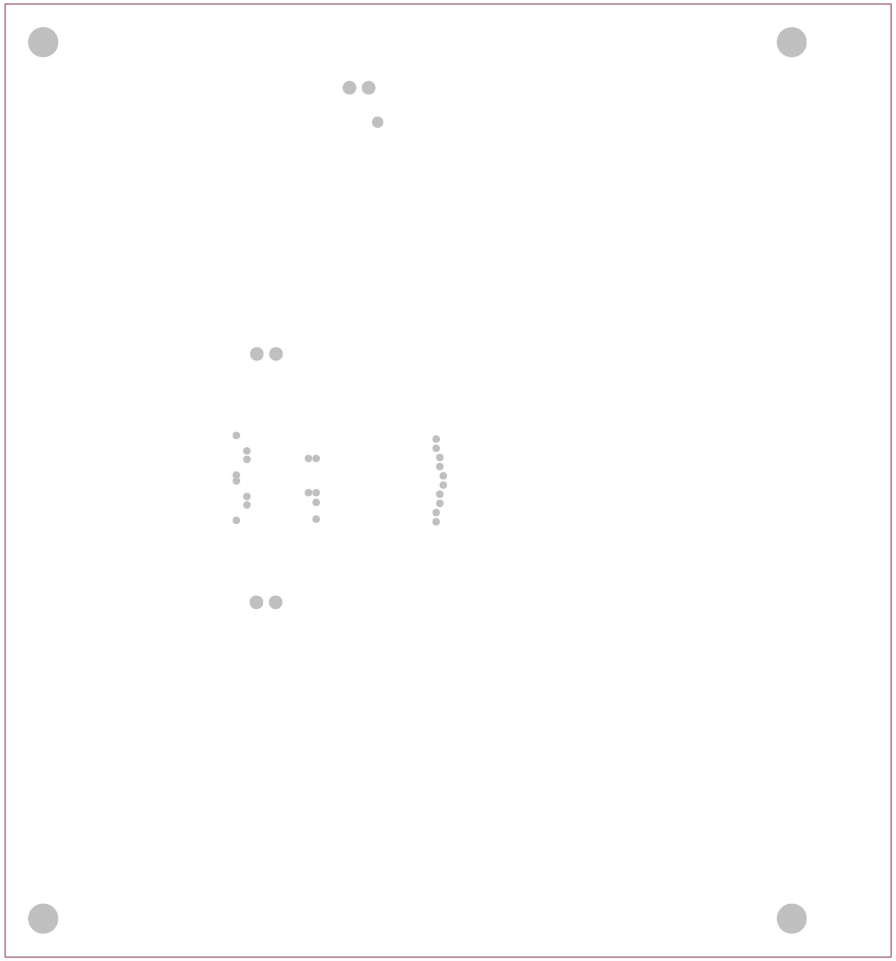

Figure 3. Inner Layer 2 (Ground Plane, Inverted)

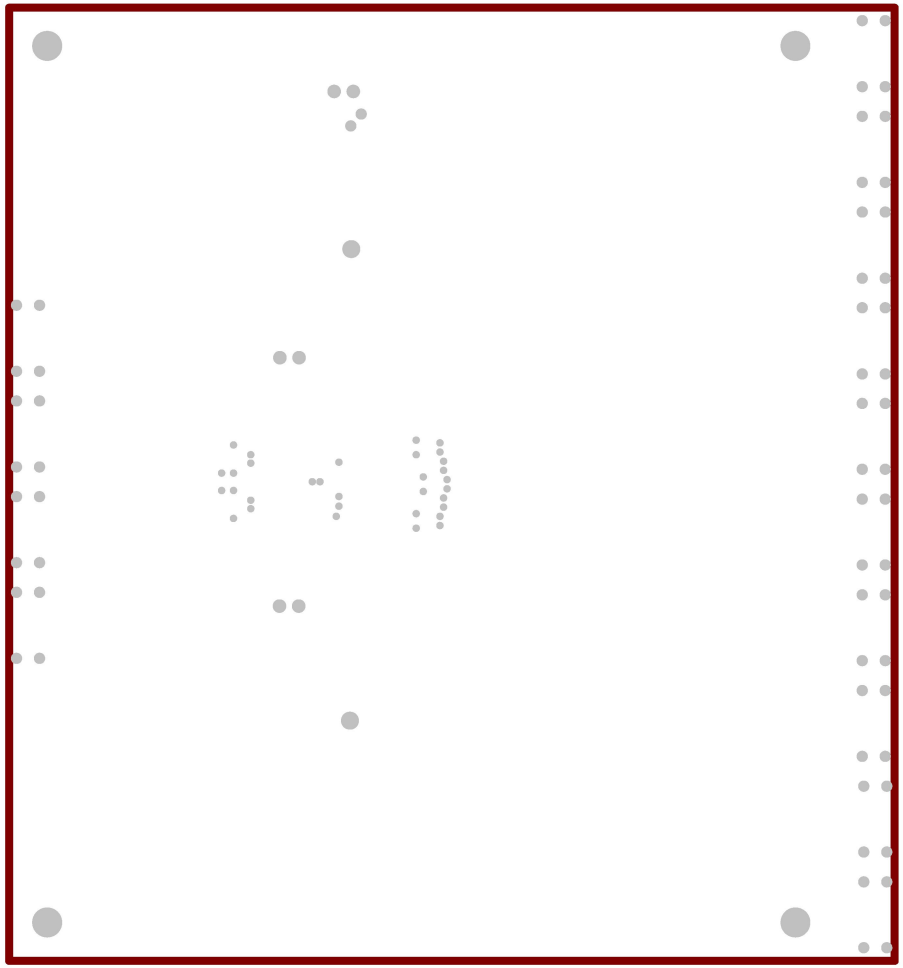

Figure 4. Inner Layer 3 (Supply Plane, Inverted)

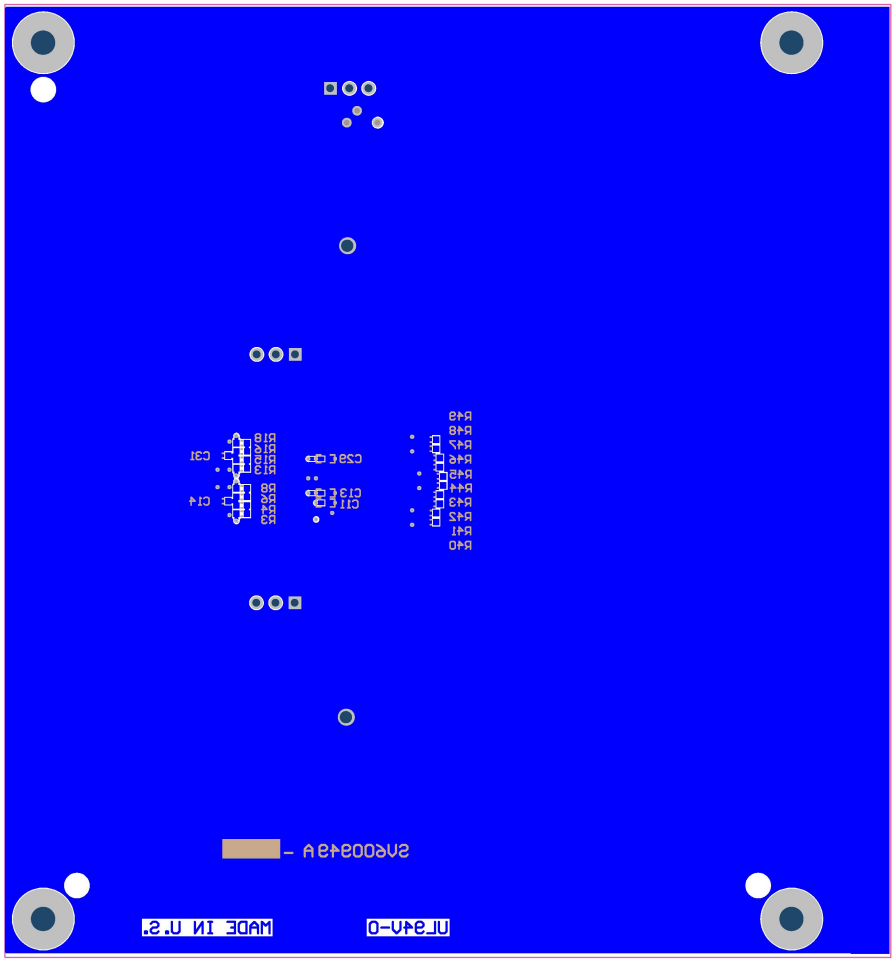

Figure 5. Bottom Layer

6 Schematic

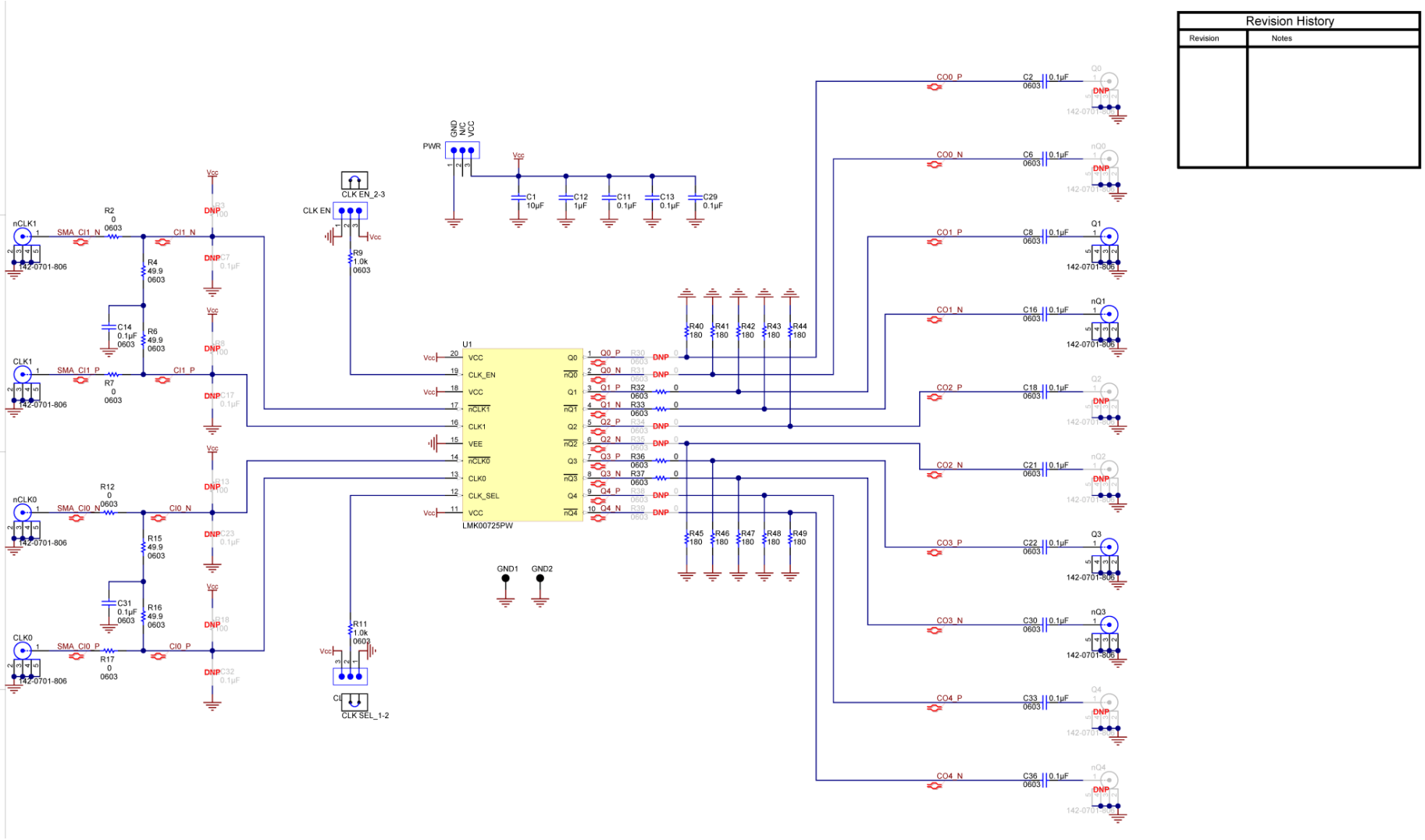

Figure 6. LMK00725EVM Schematic

7 Bill of Materials

Table 2. LMK00725EVM Bill of Materials

Designator	Qty	Value	Description	Pkg Ref	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		SV600949	Any
C1	1	10uF	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	0805	C0805C106K8PACTU	Kemet
C2, C6, C8, C14, C16, C18, C21, C22, C30, C31, C33, C36	12	0.1uF	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C11, C13, C29	3	0.1uF	CAP, CERM, 0.1uF, 10V, +/-10%, X5R, 0402	0402	C1005X5R1A104K	TDK
C12	1	1uF	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	0603	C1608X5R1A105K	TDK
CLKEN, CLKSEL, PWR	3	1x3	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
CLK0, CLK1, nCLK0, nCLK1, nQ1, nQ3, Q1, Q3	8	50 Ohm	Connector, SMT, End launch SMA 50 ohm	SMA	142-0701-806	Emerson Network Power
CLKEN_2-3, CLKSEL_1-2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
GND1, GND2	2	Black	Test Point, TH, Compact, Black	Keystone 5006	5006	Keystone
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NYPMS4400025PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
R2, R7, R12, R17, R32, R33, R36, R37	8	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R4, R6, R15, R16	4	49.9	RES, 49.9 ohm, 1%, 0.1W, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R9, R11	2	1.0k	RES, 1.0k ohm, 5%, 0.1W, 0603	0603	CRCW06031K00JNEA	Vishay-Dale
R40, R41, R42, R43, R44, R45, R46, R47, R48, R49	10	180	RES, 180 ohm, 1%, 0.1W, 0603	0603	RC0603FR-07180RL	Yageo America
U1	1		Low Skew, 1-to-5, Differential-to-3.3V LVPECL Fanout Buffer, PW0020A	PW0020A	LMK00725PW	Texas Instruments
C7, C17, C23, C32	0	0.1uF	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	0603	0603YC104JAT2A	AVX
nQ0, nQ2, nQ4, Q0, Q2, Q4	0	50 Ohm	Connector, SMT, End launch SMA 50 ohm	SMA	142-0701-806	Emerson Network Power

Table 2. LMK00725EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Pkg Ref	Part Number	Manufacturer
R3, R8, R13, R18	0	100	RES, 100 ohm, 1%, 0.1W, 0603	0603	CRCW0603100RFKEA	Vishay-Dale
R30, R31, R34, R35, R38, R39	0	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale

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