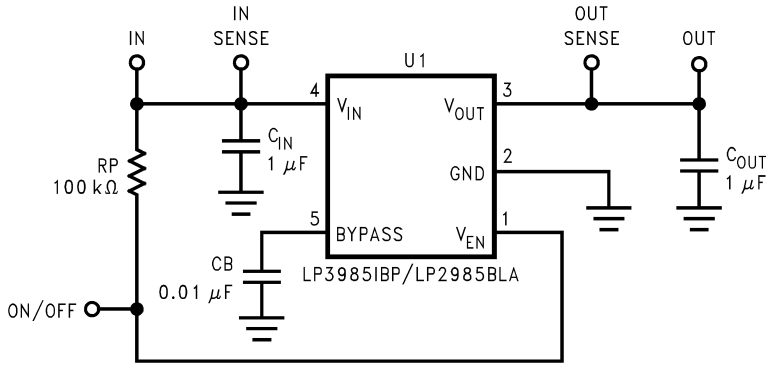
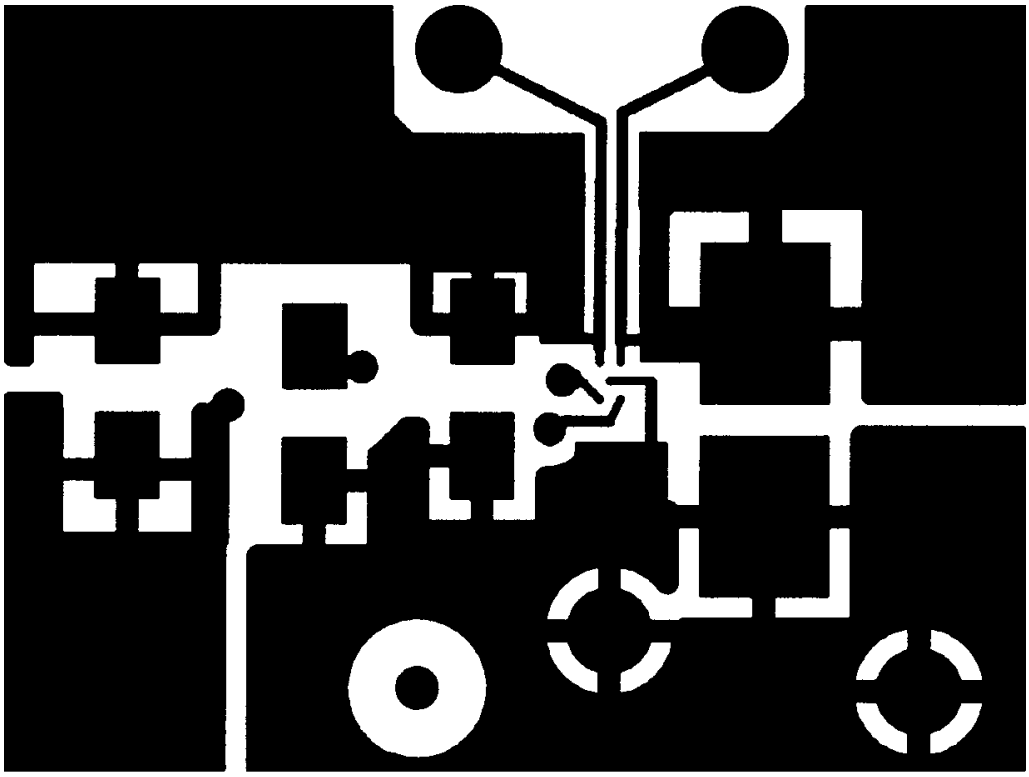
AN-1219 LP3985 DSBGA-5 Evaluation Board Instruction

This evaluation board is designed to enable independent evaluation of the LP3985 electrical performances. Each board is assembled and tested in the factory. This evaluation board instruction is for the DSBGA-5 large bump and small bump packages.

The schematic and layout of the evaluation board are shown below:





Note: The board layout for the large bump and the small bump DSBGA-5 is the same. Only the footprints are different.

The LP3985 is a micropower CMOS voltage regulator that can provide up to 150 mA of output current. The 0.01 µF bypass capacitor is optional; but if used, it will reduce noise on the regulator output. The RP resistor is tied to V_{IN} so that the regulator is on all the time. To control the V_{EN} pin externally, disconnect RP resistor and use the ON/OFF connector on the evaluation board.

The input sense and output sense pins are used for more precise voltage measurements. These pins are connected to the LP3985 input and output via high impedance traces.

The LP3895 is also available in SOT23-5. An evaluation board for the SOT23-5 package is available as well.

Table 1shows the bill of materials for the LP3985 DSBGA-5 board.

Table 1. Bill of Materials (BOM)

Designator	Value	Amount	Footprint	Note
RP	100 kΩ	1	0805	
CB	0.01 µF	1	0805	
C_{IN}	1 µF	1	0805	X5R or X7R
C_{OUT}	1 µF	1	0805/1812	X5R or X7R
U1	LP3985-xx	1	BPA05CMC or BLA05ADC	The “xx” corresponds to the appropriate LDO output voltage option.
Test Pins		7		Keystone 1040

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