AN-1227 LM3485 Evaluation Board

1   Introduction

The LM3485 is a hysteretic P-FET buck controller that uses a pulse-frequency modulation (PFM) scheme to regulate the output voltage. This LM3485 demo board and the recommended components are intended to demonstrate the performance with a 3.3 V output from a 12 V source. The demo board can be used with source voltages from 7 V to 28 V to deliver output load currents up to 1A. By changing the size of a single resistor, regulated output voltages from 1.242 V to 5 V can be obtained.

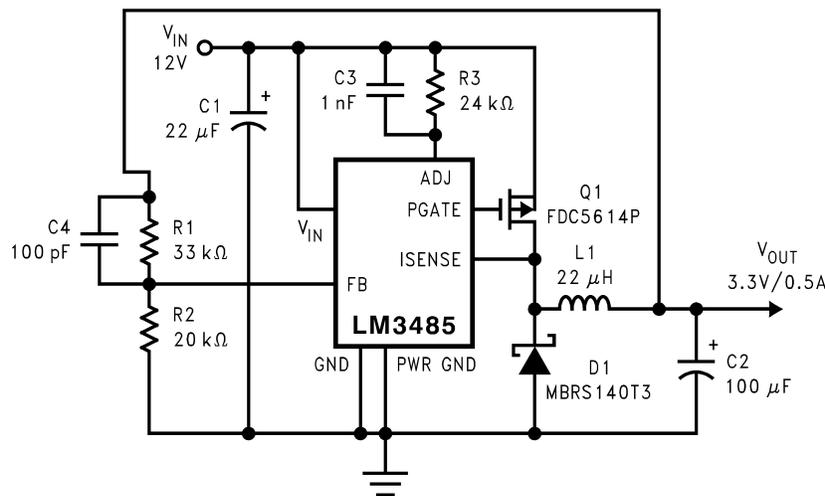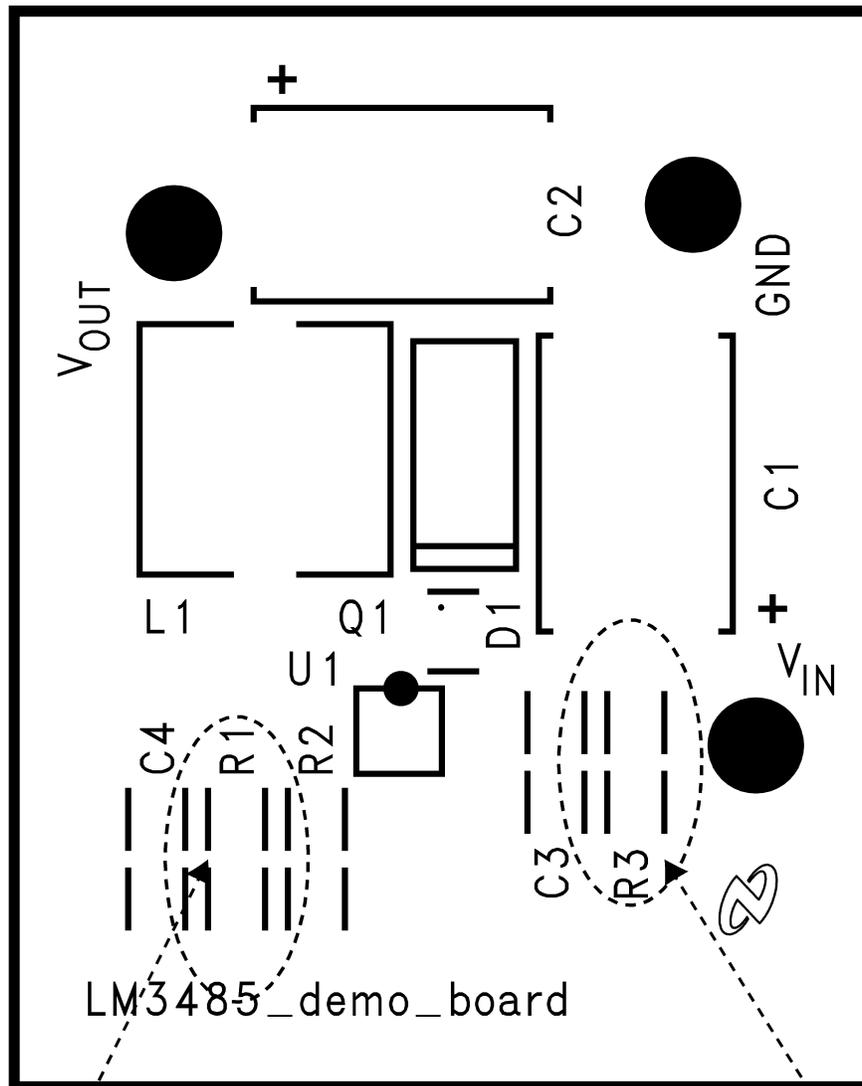The circuit schematic is shown in Figure 1 and the bill of materials is given in Table 1.

Figure 1. Regulator With 3.3 V Output at 0.5A

Table 1. Bill of Materials (BOM)

Code	Description	Manufacturer
C1	Input Capacitor CAP-Tantalum 22 µF 35 V EEJL1VD226R	Panasonic
C2	Output Capacitor CAP-POSCAP 100 µF 6.3 V 6TPC100M	Sanyo
C3	C_{ADJ} CAP-Ceramic Chip 1nF 50 V GRM39X7R102K50	Murata
C4	C_{ff} CAP-Ceramic Chip 100pF 50 V GRM39X7R101K50	Murata
D1	Catch Diode Schottky Diode 1A 30 V MBRS130T3	On Semiconductor
L1	Inductor 22 µH LQH66SN220M01L	Murata
Q1	P-channel MOSFET -60 V FDC5614P	Fairchild
R1	Feedback high side resistor Chip Resistor 33 KΩ MCR10EZHF3302	Rohm
R2	Feedback low side resistor Chip Resistor 20 KΩ MCR10EZHF2002	Rohm
R3	R_{ADJ} Chip Resistor 24KΩ MCR10EZHF2402	Rohm
U1	Buck Controller LM3485	Texas Instruments

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2 Output Voltage Current Limit Setting

Figure 2. Component Location (Top Side)

3   Layout Fundamentals

The LM3485 can work in a wide range of applications. For your application circuit, proper layout for the buck regulator should be implemented by following a few simple guidelines.

1. Place the power components, which are the MOSFET, diode, inductor and filter capacitors, close together. Make the traces between them as short and as wide as possible.

2. Place the trace for the Gate of the external PFET as close as possible to the PGATE pin of the LM3485.

3. Separate any noise sensitive traces, primarily in the voltage feedback path, from noise source traces associated with the inductor.

4. Keep the trace short between the ground pin of the input capacitor and the anode of the diode.

5. Ensure the ground is low impedance.
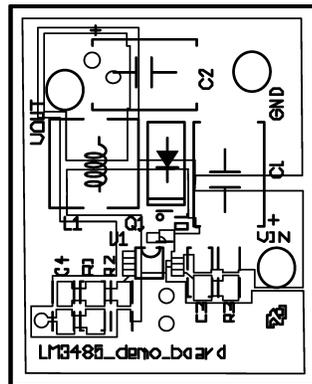
Figure 3. Top Layer
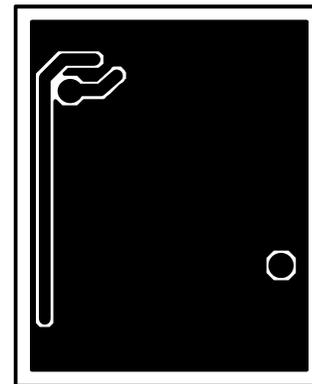
Figure 4. Bottom Layer

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