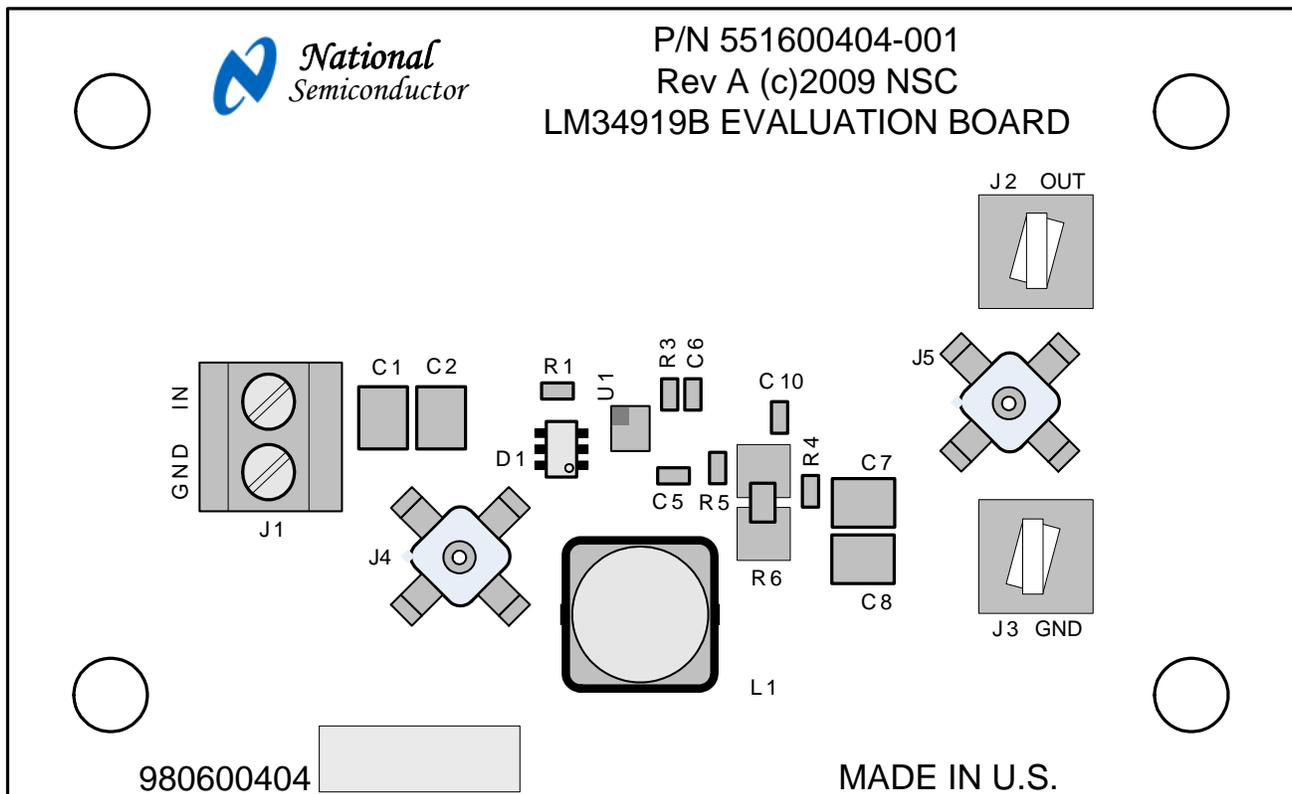# AN-2016 LM34919B Evaluation Board

1 Introduction

The LM34919BEVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 3.3V output over an input range of 6V to 24V. The circuit delivers load currents to 600 mA, with current limit set at a nominal 800 mA. The board is populated with all components except R5, C9 and C10. These components provide options for managing the output ripple as described later in this document.

The board's specification are:

- Input Voltage: 6V to 24V
- Output Voltage: 3.3V
- Maximum load current: 600 mA
- Minimum load current: 0A
- Current Limit: 780 mA to 815 mA
- Measured Efficiency: 88.7% (V_{IN} = 6V, I_{OUT} = 300 mA)
- Nominal Switching Frequency: 1.5 MHz
- Size: 2.6 in. x 1.6 in. x 0.5 in

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Note: R2, C3, C4, and C9 are located on board's back side.

Figure 1. Evaluation Board - Top Side

2   Theory of Operation

Figure 1 shows the evaluation board schematic, which contains a simplified block diagram of the LM34919B. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and V_{IN} according to Equation 1:

$$t_{ON} = \frac{0.565 \times 10^{-10} \times (R1 + 1.4 \text{ k}\Omega)}{V_{IN} - 1.5V} + 55 \text{ ns}$$

(1)

The on-time of this evaluation board ranges from ≈424 ns at V_{IN} =6V, to ≈129 ns at V_{IN} = 24V. The on-time varies inversely with V_{IN} to maintain a nearly constant switching frequency. At the end of each on-time the Minimum Off-Timer ensures the buck switch is off for at least 88 ns. In normal operation, the off-time is much longer. During the off-time, the load current is supplied by the output capacitor (C7, C8). When the output voltage falls sufficiently that the voltage at FB is below 2.5V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at FB to switch the regulation comparator. The current limit threshold is ≈780 mA at V_{IN} = 6V, and ≈812 mA at V_{IN} = 24V. The variation is due to the change in ripple current amplitude as V_{IN} varies. for a more detailed block diagram, and a complete description of the various functional blocks, see the *LM34919B, LM34919B-Q1 Ultra-Small 40-V 600-mA Constant On-Time Buck Switching Regulator Data Sheet* (SNVS623).

3   Board Layout and Probing

The pictorial in Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

- The LM34919B, and diode D1 may be hot to the touch when operating at high input voltage and high load current.
- Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.
- At maximum load current (0.6A), the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

4   Board Connection/Start-up

The input connections are made to the J1 connector. The load is connected to the J2 (OUT) and J3 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 6V, at which time the output voltage should be 3.3V. If the output voltage is correct with 6V at V_{IN}, then increase the input voltage as desired and proceed with evaluating the circuit. DO NOT EXCEED 40V AT V_{IN}.

5   Output Ripple Control

The LM34919B requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW pin, for proper operation. The required ripple can be supplied from ripple at V_{OUT}, through the feedback resistors as described in Section 5.1 and Section 5.2, or the ripple can be generated separately (using R5, C9, and C10) in order to keep the ripple at V_{OUT} at a minimum (Section 5.3).

5.1   *Option A) Lowest Cost Configuration*

This evaluation board is supplied with R4 installed in series with the output capacitance (C7, C8). R4 is chosen to generate ≥25 mVp-p at V_{OUT}, knowing that the minimum ripple current in this circuit is ≅140 mAp-p at minimum V_{IN}. Using 0.27Ω for R4, the ripple at V_{OUT} ranges from ≅37 mVp-p to ≅88 mVp-p over the input voltage range. If the application can accept this ripple level, this is the most economical solution. The circuit is shown in Figure 2. See Figure 8.
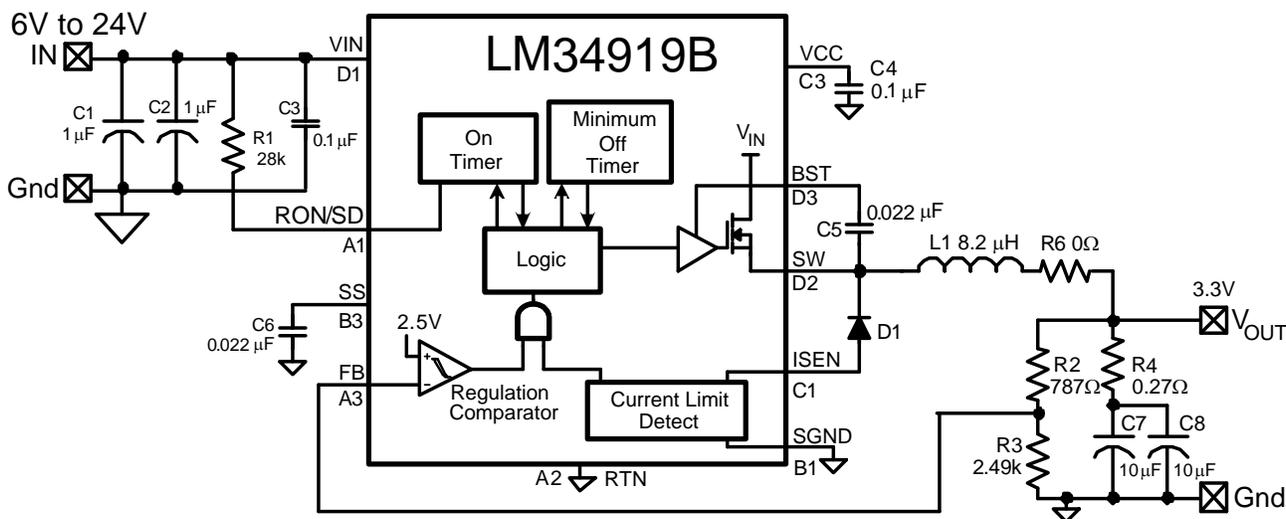

Figure 2. Lowest Cost Configuration

5.2 Option B) Intermediate Ripple Configuration

This configuration generates less ripple at V_{OUT} than Section 5.1 by the addition of one capacitor (Cff) across R2, as shown in Figure 3.
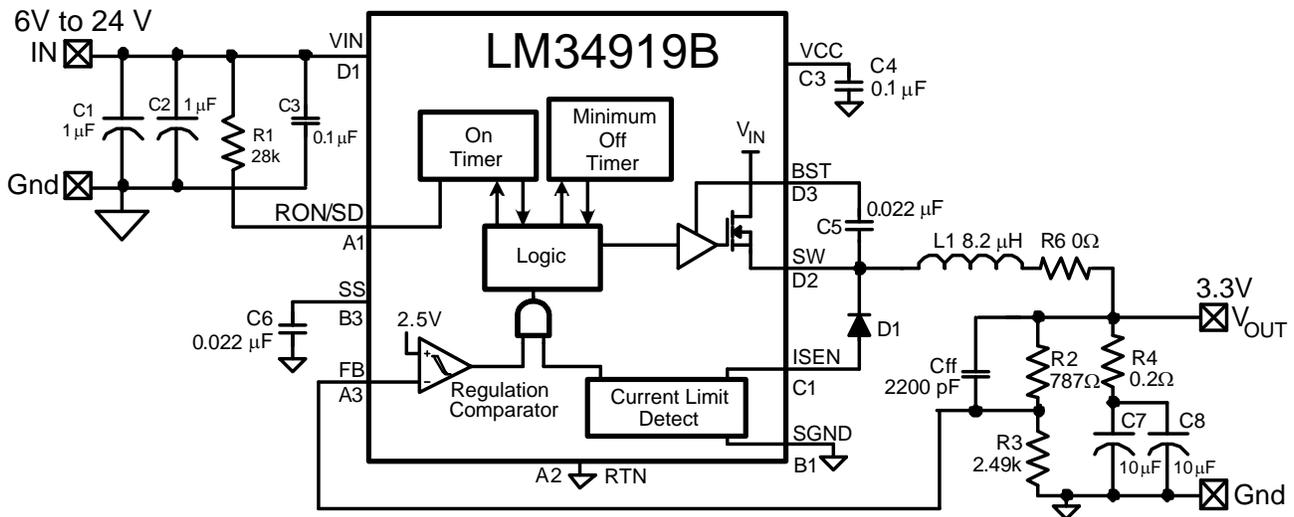

Figure 3. Intermediate Ripple Configuration

Since the output ripple is passed by Cff to the FB pin with little or no attenuation, R4 can be reduced so the minimum ripple at V_{OUT} is ≅25 mVp-p. The minimum value for Cff is calculated from:

$$Cff \geq \frac{t_{ON\,(max)} \times 3}{(R2//R3)}$$

(2)

where $t_{ON(max)}$ is the maximum on-time (at minimum V_{IN}), and R2//R3 is the parallel equivalent of the feedback resistors, see Figure 8.

5.3 Option C) Minimum Ripple Configuration

To obtain minimum ripple at V_{OUT}, R4 is set to 0Ω, and R5, C9, and C10 are added to generate the required ripple for the FB pin. In this configuration, the output ripple is determined primarily by the ESR of the output capacitance and the inductor's ripple current.

The ripple voltage required by the FB pin is generated by R5, C10, and C9 since the SW pin switches from -1V to V_{IN}, and the right end of C10 is a virtual ground. The values for R5 and C10 are chosen to generate a 50-100 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through C9. The following procedure is used to calculate values for R5, C10 and C9.

1) Calculate the voltage V_A:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN})))$$

(3)

where, V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1V), and V_{IN} is the minimum input voltage. For this circuit, V_A calculates to 2.84V. This is the approximate DC voltage at the R5/C10 junction, and is used in Equation 4.

2) Calculate the R5 x C10 product:

$$R5 \times C10 = \frac{(V_{IN} - V_A) \times t_{ON}}{\Delta V}$$

(4)

where, t_{ON} is the maximum on-time (≅424 ns), V_{IN} is the minimum input voltage, and ΔV is the desired ripple amplitude at the R5/C10 junction, 50 mVp-p for this example.

$$R5 \times C10 = \frac{(6V - 2.84V) \times 424\ ns}{0.05V} = 26.8 \times 10^{-6}$$

(5)

R5 and C10 are then chosen from standard value components to satisfy the above product. Typically C10 is 3000 to 5000 pF, and R5 is 10kΩ to 300 kΩ. C9 is chosen large compared to C10, typically 0.1 µF, see Figure 4 and Figure 8.
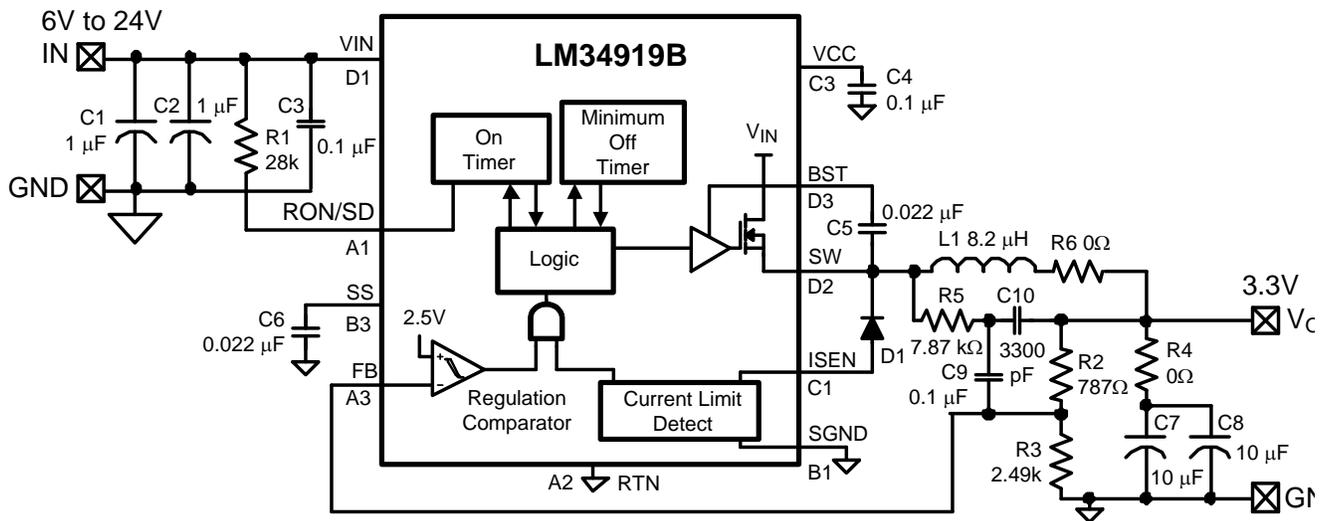
Figure 4. Minimum Output Ripple Configuration

6 Monitor The Inductor Current

The inductor's current can be monitored or viewed on a scope with a current probe. Remove R6, and install an appropriate current loop across the two large pads where R6 was located. In this way, the inductor's ripple current and peak current can be accurately determined.

7 Scope Probe Adapters

Scope probe adapters are provided on this evaluation board for monitoring the waveform at the SW pin, and at the circuit's output (V_{OUT}), without using the probe's ground lead that can pick up noise from the switching waveforms..

8 Minimum Load Current

The LM34919B requires a minimum load current of ≅1 mA to ensure the boost capacitor (C5) is recharged sufficiently during each off-time. In this evaluation board, the minimum load current is provided by the feedback resistors allowing the board's minimum load current at V_{OUT} to be specified at zero.
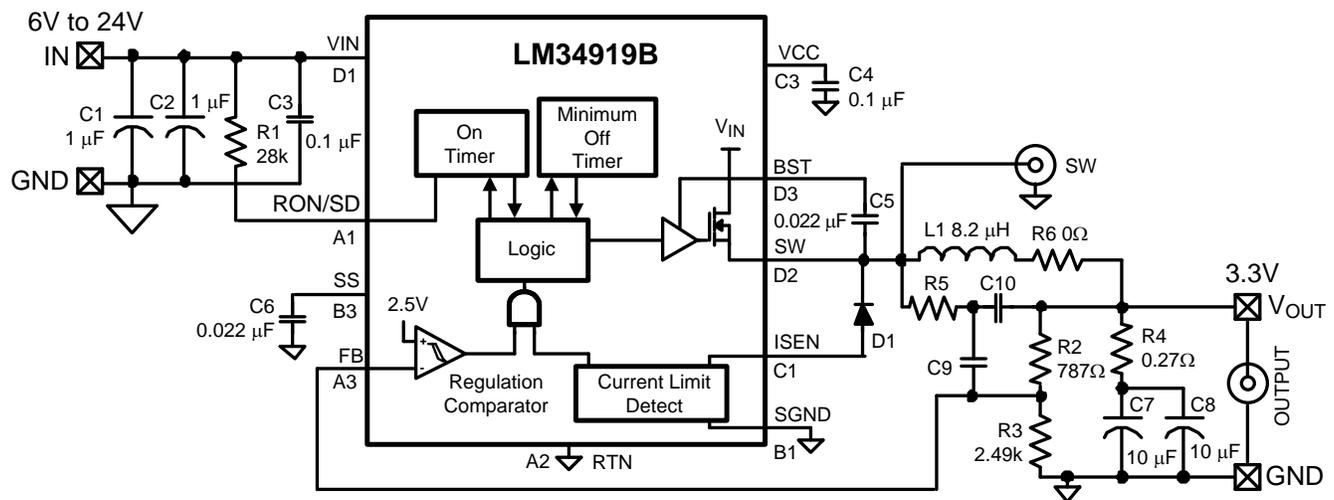
Figure 5. Complete Evaluation Board Schematic

Table 1. Bill of Materials (BOM)

Item	Description	Mfg., Part Number	Package	Value
C1	Ceramic Capacitor	TDK C3216X7R1H105M	1206	1.0 µF, 50V
C2	Ceramic Capacitor	TDK C3216X7R1H105M	1206	1.0 µF, 50V
C3	Ceramic Capacitor	TDK C1608X7R1H104K	0603	0.1 µF, 50V
C4	Ceramic Capacitor	TDK C1608X7R1H104K	0603	0.1 µF, 50V
C5	Ceramic Capacitor	TDK C1608X7R1H223K	0603	0.022 µF, 50V
C6	Ceramic Capacitor	TDK C1608X7R1H223K	0603	0.022 µF, 50V
C7, C8	Ceramic Capacitor	TDK C3216X7R1C106K	1206	10 µF, 16V
C9	Ceramic Capacitor	Unpopulated	0603	
C10	Ceramic Capacitor	Unpopulated	0603	
D1	Schottky Diode	Zetex ZLLS2000	SOT23-6	40V, 2.2A
L1	Power Inductor	Bussman DR74-8R2–R	7.6 mm x 7.6 mm	8.2 µH, 2.5A
R1	Resistor	Vishay CRCW060328KOFK	0603	28 kΩ
R2	Resistor	Vishay CRCW0603787RFK	0603	787 Ω
R3	Resistor	Vishay CRCW06032K49FK	0603	2.49 kΩ
R4	Resistor	Panasonic ERJ3RQFR27	0603	0.27Ω
R5	Resistor	Unpopulated	0603	
R6	Resistor	Vishay CRCW08050000Z	0805	0Ω Jumper
U1	Switching Regulator	LM34919	10 Bump DSBGA	

9   Circuit Performance
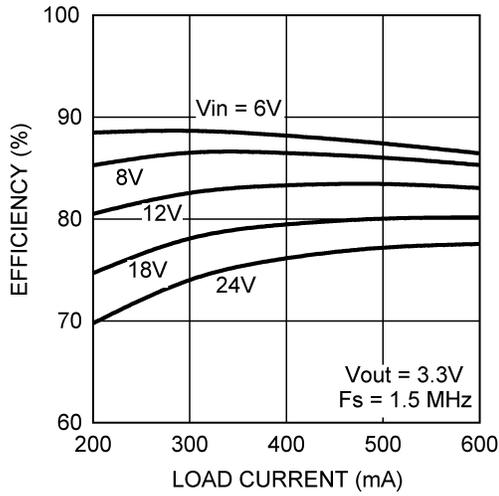
Figure 6. Efficiency vs Load Current
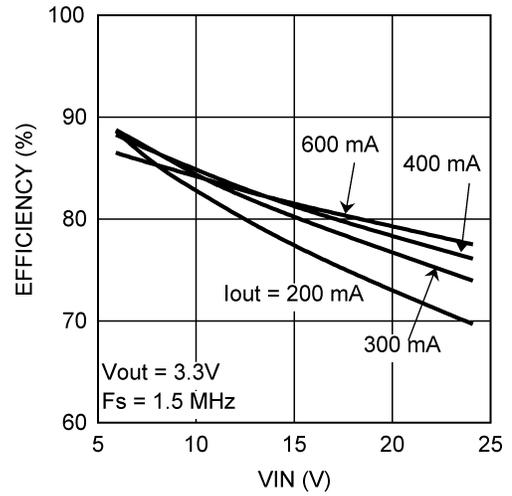
Figure 7. Efficiency vs Input Voltage
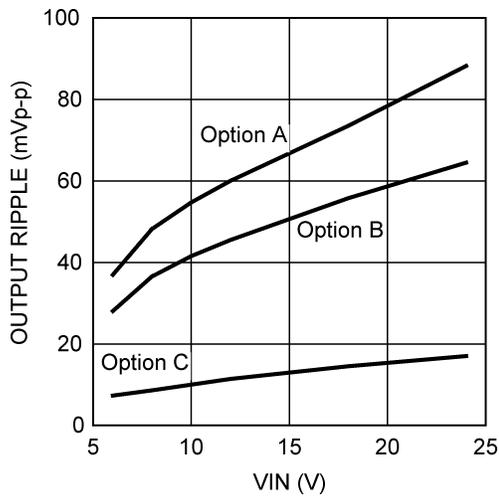
Figure 8. Output Voltage Ripple
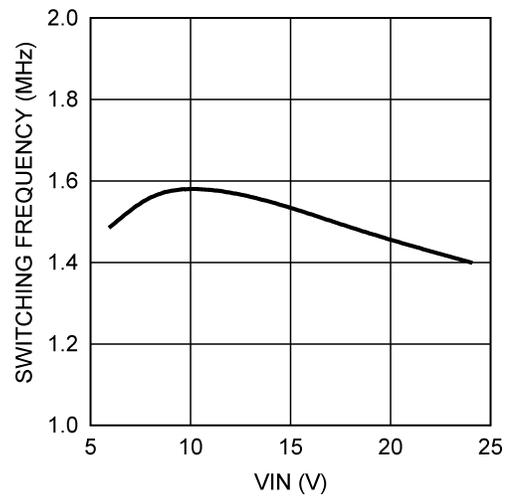
Figure 9. Switching Frequency vs. Input Voltage
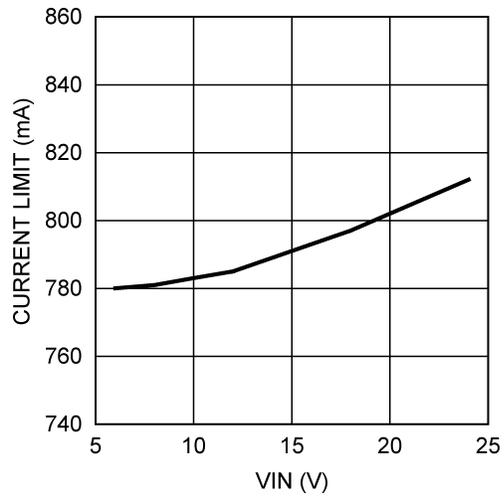
Figure 10. Load Current Limit vs Input Voltage

10   Typical Waveforms
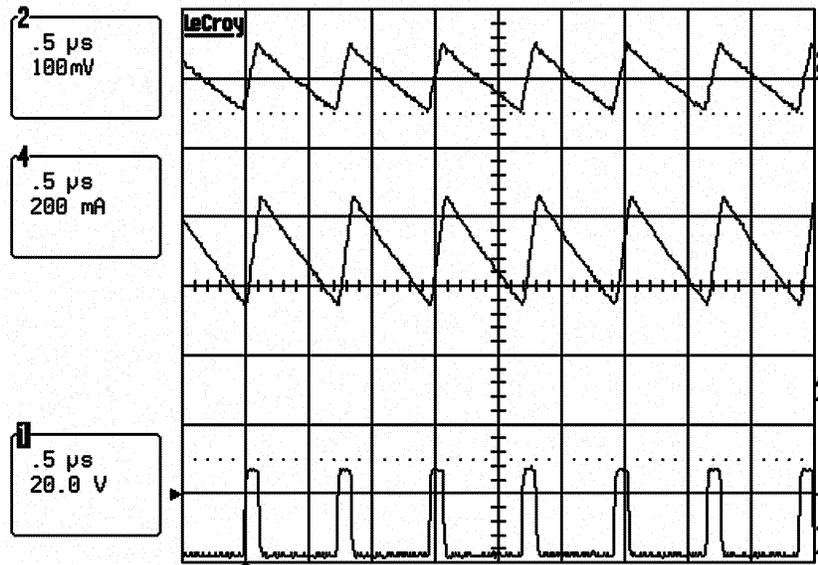
Trace 2= V_{OUT}
Trace 4= inductor Current
Trace 1= SW Pin
V_{IN} = 24V, I_{OUT} = 400 mA

Figure 11. Continuous Conduction Mode
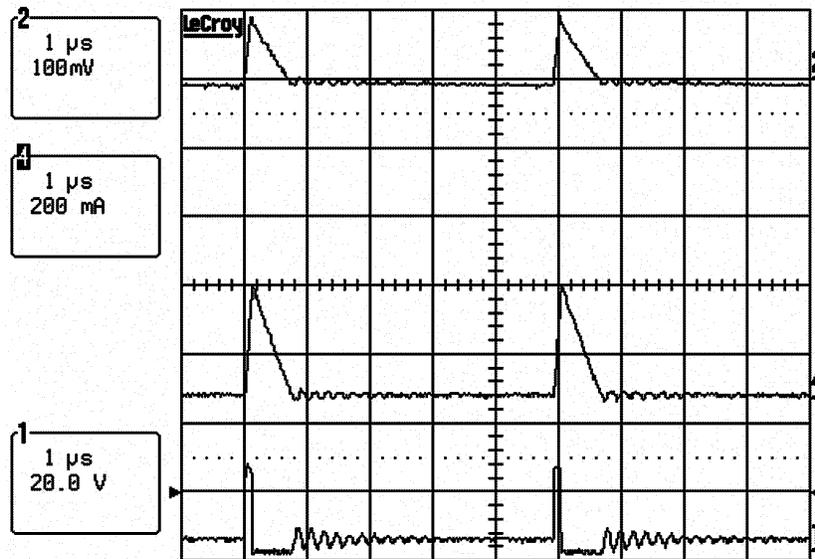
Trace 2= V_{OUT}
Trace 4= inductor Current
Trace 1= SW Pin
V_{IN} = 24V, I_{OUT} = 20 mA

Figure 12. Discontinuous Conduction Mode

11 PC Board Layout
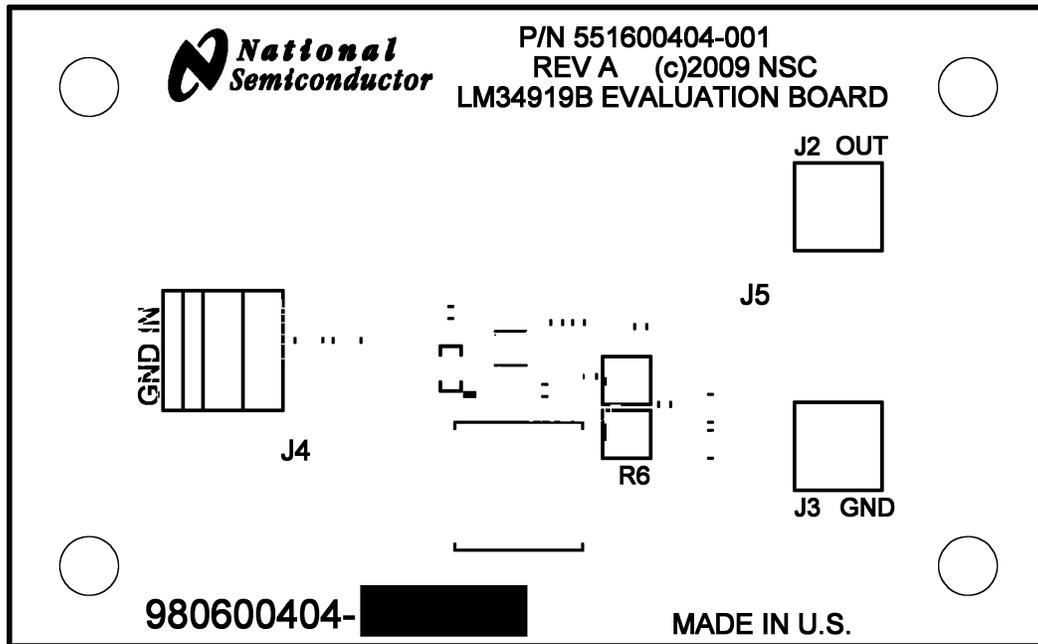
Figure 13. Board Silkscreen
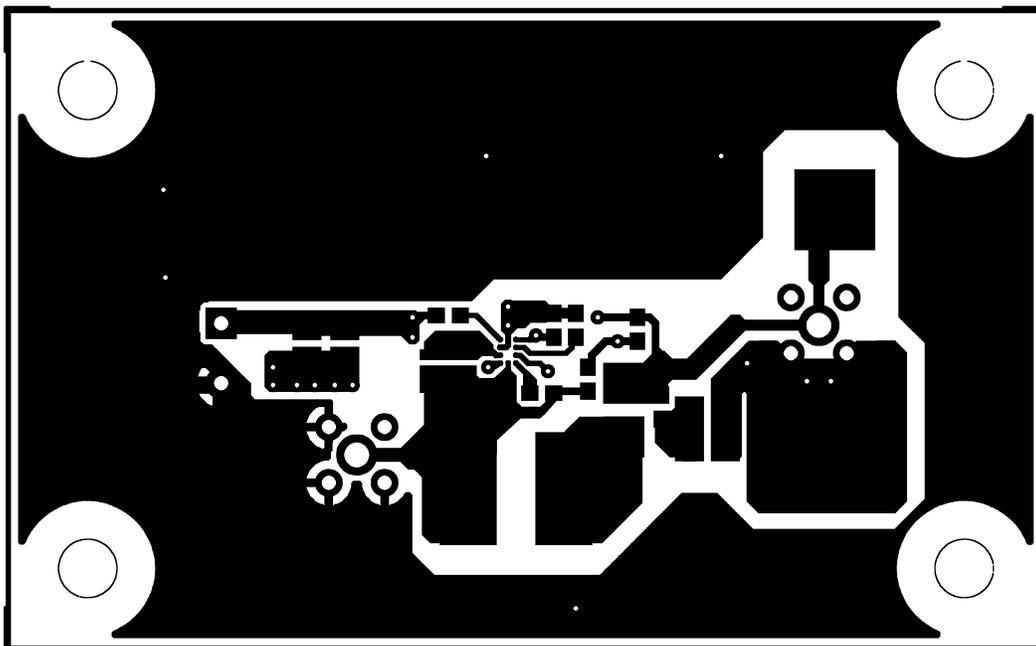
Figure 14. Board Top Layer
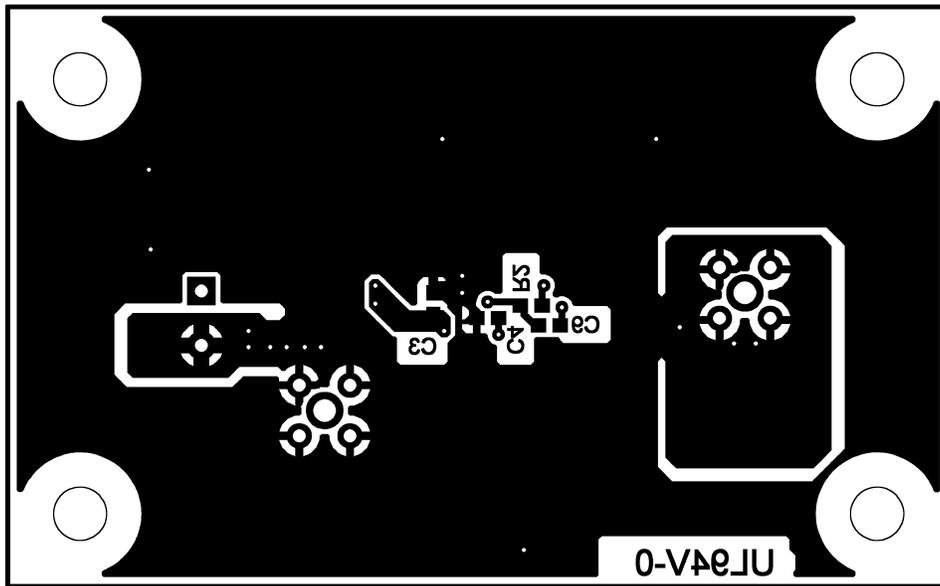
Figure 15. Board Bottom Layer (Viewed from Top)

IMPORTANT NOTICE

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