Application Report

LM60430 and LM60440 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LM60430 and LM60440 (WQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 show the device functional block diagrams for reference.

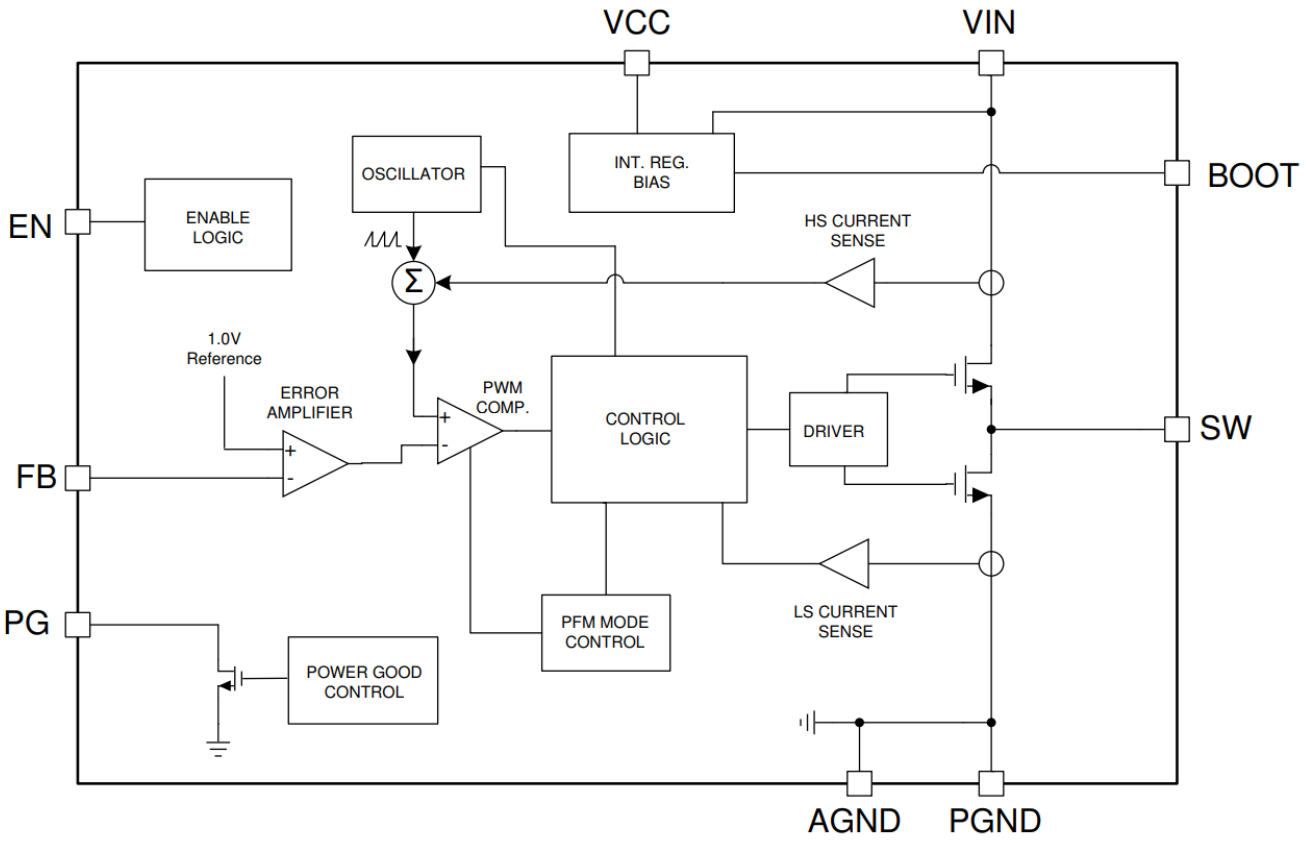

Figure 1-1. Functional Block Diagram: LM60430, LM60440

LM60430 and LM60440 were developed using a quality-managed development process, but were not developed in accordance with the ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM60430 and LM60440 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	LM60430 FIT (Failures Per 10^9 Hours)	LM60440 FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	13	14
Die FIT Rate	5	6
Package FIT Rate	8	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 400 mW (for LM60430) and 500 mW (for LM60440)
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, Analog, Mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM60430 and LM60440 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW No output	35%
SW output not in specification - voltage or timing	45%
SW power FET stuck on	10%
PGOOD false trip, fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM60430 and LM60440. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of critical functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM60430 and LM60440 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the LM60430 and LM60440 data sheet.

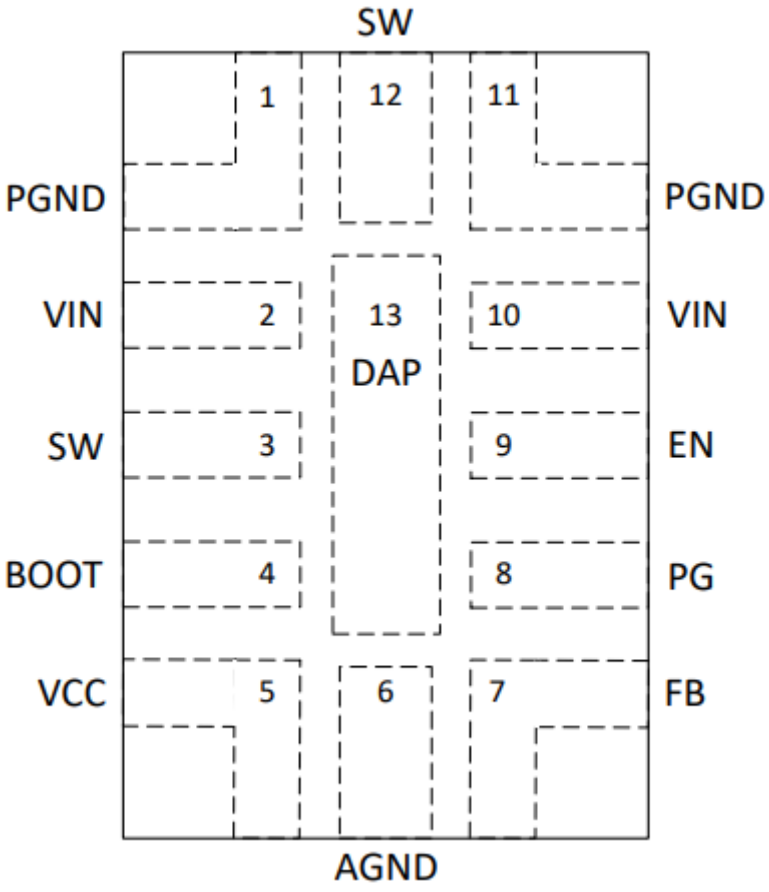

Figure 4-1. Pin Diagram: LM60430, LM60440

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	Normal Operation	D
VIN	2,10	Input supply would collapse and as a result there will be no output voltage	B
SW	3,12	Damage to power switches likely; loss of VOUT regulation	A
BOOT	4	No switching	B
VCC	5	No switching; loss of all functionality	B
AGND	6	Normal operation	D
FB	7	Loss of VOUT regulation	B
PG	8	Loss of power good indicator if used	C
EN	9	IC will not start	B
PGND	11	Normal operation	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	Vout normal; current distribution in power switched will be affected, potentially degrading jitter/EMI/reliability	C
VIN	2,10	Vout normal; current distribution in power switched will be affected, potentially degrading jitter/EMI/reliability	C
SW	3	Loss of VOUT regulation	B
BOOT	4	No switching	B
VCC	5	Internal VCC supply will be unstable without VCC bypass capacitor; abs max maybe exceeded; possibly loss of VOUT regulation	A
AGND	6	May increase noise/jitter and possibly loss of regulation	B
FB	7	Loss of VOUT regulation	B
PG	8	Loss of power good indicator if used	C
EN	9	Possible loss of VOUT regulation	B
PGND	11	Vout normal; current distribution in power switched will be affected, potentially degrading jitter/EMI/reliabilit	C
SW	12	No switching, if CB returns via this pin	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	Input supply would collapse and as a result there will be no output voltage	B
VIN	2	Damage to power siwtches likely; loss of VOUT regulation	A
SW	3	Loss of VOUT regulation	B
BOOT	4	No switching	B
VCC	5	No switching; loss of all functionality	B
AGND	6	Loss of VOUT regulation	B
FB	7	Abs max may be exceeded, and loss of VOUT regulation	A
PG	8	Abs max may be exceeded, and possibly unable to start	A
EN	9	Normal operation; IC will not shut down	C
VIN	10	Input supply would collapse and as a result there will be no output voltage	B
PGND	11	Damage to the power switches likely; loss of VOUT regulation	A
SW	12	Damage to the power switches likely; loss of VOUT regulation	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Input

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	Input supply would collapse and as a result there will be no output voltage	B
VIN	2,10	Normal operation	D
SW	3,12	Damage to the power switches likely; loss of VOUT regulation	A
BOOT	4	Damage to the driver circuitry likely; loss of VOUT regulation	A
VCC	5	Abs max may be exceeded	A
AGND	6	Input supply would collapse and as a result there will be no output voltage	B
FB	7	Abs max may be exceeded; loss of VOUT regulation	A
PG	8	Abs max may be exceeded	A
EN	9	Normal operation; IC will not shut off	C
PGND	11	Input supply would collapse and as a result there will be no output voltage	B

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