User's Guide

TPSM846C24 Power Module Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPSM846C24EVM-006 evaluation module (BSR006). The user's guide also includes the performance specifications, schematic, bill of materials (BOM), and layout of the EVM.

Table of Contents

Trademarks

1 Description

The TPSM846C24 device is a highly integrated, synchronous buck power module that combines a 35-A DC/DC converter with power MOSFETs, a shielded inductor, some input and output capacitors, and passives into a low profile package. The input voltage range is from 4.5 V to 15 V. The output voltage range is from 0.5 V to 2 V.

This evaluation module is designed to demonstrate the ease-of-use and small printed-circuit-board area that may be achieved when designing with the TPSM846C24 power module. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. Additionally, control test points are provided for use of the power good, enable control, and synchronization features of the device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

2 Getting Started

Figure 2-1 highlights the user interface items associated with the EVM. The polarized input power terminal block (TB1) is used for connection to the host input supply. TB2 allows two terminals for VOUT and TB3 allows two terminals for PGND for connection to the load. These terminal blocks can except up to 10-AWG wire.

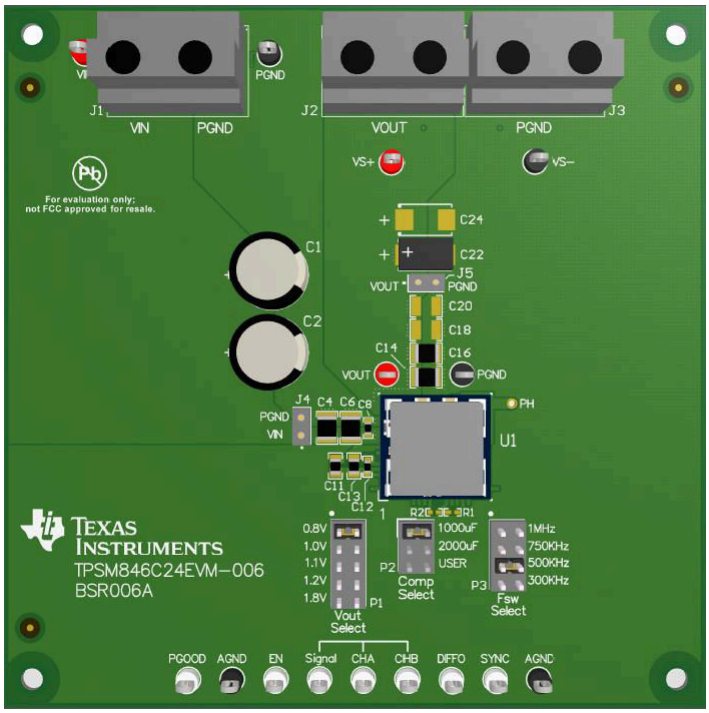

Figure 2-1. EVM User Interface

The VIN monitor (VIN and PGND) test points and VOUT monitor (VS+ and VS–) test points located near the input terminal block and the output terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure the input and output voltages. Do *not* use these VIN and VOUT monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents.

The VIN scope (J1) and VOUT scope (J2) test points can be used to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1-inch centers. Insert the scope probe tip into the socket labeled VIN or VOUT, and insert the scope ground lead into the hole of the socket labeled PGND.

The test points located along the bottom of the EVM are made available to test the features of the device. Any external connections made to these test points should be referenced to one of the AGND test points. Refer to Section 3 for more information on the individual control test points.

The *Vout Select* jumper (P1) is used to set the output voltage. Select one of the five output voltages using a jumper. If a different voltage is required than the five selected using the jumper, leave the P1 jumper open and populate the correct resistor in position R2 on the EVM.

The *Comp Select* jumper (P2) sets the proper frequency compensation for the total amount of output capacitance present on the V_{OUT} bus. The EVM is shipped with approximately 1000 µF of output capacitance loaded on the board. Locations are provided on the board to add additional output capacitance (C18–C21, C24, C25). The default *Comp Select* jumper is loaded in the 1000-µF position, which is the correct setting for output capacitance from 1000 µF to 1500 µF. The jumper position labeled 2000 µF selects compensation components for 1500 µF to 3000 µF of output capacitance. The jumper position labeled *USER* selects compensation components for 3000 µF to 5000 µF of output capacitance. See the *TPSM846C24 4.5-V to 15-V Input, 0.5-V to 2.0-V Output, 35-A Power Module Data Sheet* for more information on selecting compensation components.

The *Fsw Select* jumper (P3) is used to set the switching frequency. Select from 300 kHz, 500 kHz, 750 kHz, and 1 MHz. The default jumper loading is the 500-kHz position.

3 Test Point Descriptions

Wire-loop test points and scope probe test points are provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. Table 3-1 provides a description of each test point:

Table 3-1. Test Points

Test Point	Description
VIN	Input voltage monitor. Connect DVM across this point and PGND for measuring efficiency.
VS+	Supply path output voltage monitor. Connect DVM positive lead to this point for line and load regulation.
VS–	Return path output voltage monitor. Connect DVM negative lead to this point for measuring line and load regulation.
VOUT	Output voltage monitor. Connect DVM to this point and PGND for measuring efficiency.
PGND	Input and output voltage monitor grounds. Reference the VIN and VOUT DVMs to these ground points.
VIN MON (J1)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT MON (J2)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
AGND	Analog ground point. Use any of the AGND test points as the ground reference for the control signals.
ALERT	PMBus ALERT line, used to monitor the ALERT signal.
CLK	PMBus CLK line, used to monitor the CLK signal.
DATA	PMBus DATA line, used to monitor the DATA signal.
PGOOD	Monitors the power-good signal of the device. This is an open-drain signal that has an on-board 10-kΩ pullup resistor to 3.3 V.
CNTL	Control pin, pull to GND to stop power conversion. Float or pull to 3.3 V to enable power conversion. An internal 10-kΩ pullup resistor to 3.3 V is present on the EVM.
Signal	Signal injection point for the Bode plot analyzer. Inject from Signal to CHB.
CHA	Input signal monitoring point for the Bode plot analyzer
CHB	Output signal monitoring point for the Bode plot analyzer
DIFFO	Output of remote sense differential amplifier
SYNC	Connects to the SYNC pin of the device. An external clock signal can be applied to this point to synchronize the device to an appropriate frequency.
PH	Switch node of the TPSM846C24 device. Use an un-hooded scope probe to monitor this point.

Note

Refer to the *TPSM846C24 4.5-V to 15-V Input, 0.5-V to 2.0-V Output, 35-A Power Module Data Sheet* for absolute maximum ratings associated with features in Table 3-1.

4 Operation Notes

To operate the EVM, apply a valid input voltage from 4.5 V to 15 V. The power supply providing the input voltage must be rated for sufficient input current. The undervoltage lockout (UVLO) can be programmed using the PMBus commands.

The output voltage range is from 0.5 V to 2.0 V. The EVM can be evaluated at five popular output voltage settings by selecting a jumper (P1).

The TPSM846C24 is a 35-A device. When connecting the EVM to the external load, use wiring capable of safely handling 35 A of output current.

The Power-Good (PGOOD) indicator of the EVM will assert high when the output voltage is within ±5% of the programmed output voltage value. A 10-kΩ pullup resistor (R11) is populated between the PGOOD pin and the BP3 pin.

The TPSM846C24 EVM is set-up to operate at 500 kHz, but the switching frequency can be adjusted using the P3 jumper. If an exact switching frequency is required, the device can be synchronized to an external clock over the frequency range of 300 kHz to 1 MHz. Refer to *TPSM846C24 4.5-V to 15-V Input, 0.5-V to 2.0-V Output, 35-A Power Module Data Sheet* for further information on synchronization.

The TPSM846C24EVM-006 includes both input and output capacitors. The EVM includes footprints for adding additional input and output capacitors to the EVM. Adding additional capacitance will improve transient response. The actual capacitance required will depend on the input and output voltage conditions of the particular application, along with the desired transient response. Refer to the product data sheet for further information on input and output capacitance and transient response.

The EVM uses remote sense connections to regulate the output voltage at the output terminals of the EVM. The remote sense connections are made through 0-Ω resistors, R16 and R18. If remote sense is required at a different point, R16 and R18 can be replaced with 10-Ω resistors and VS+ and VS– test points can be extended to the new sense point.

5 Performance Data

Figure 5-1 through Figure 5-3 provide the EVM performance data using the following conditions:

V_{IN} = 12 V, F_{sw} = 500 kHz, C_{OUT} = 4 × 47-µF ceramic plus 2 × 470-µF polymer

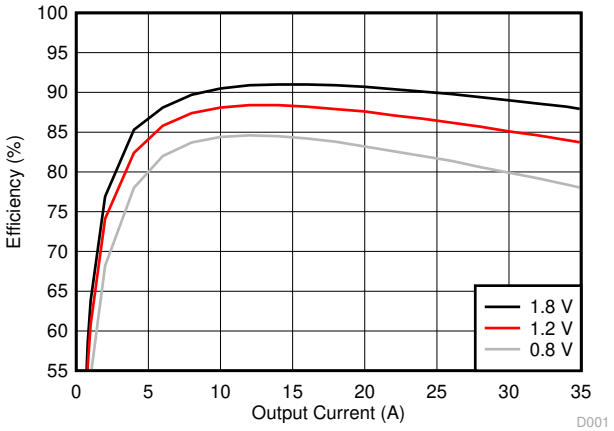

Figure 5-1. Efficiency

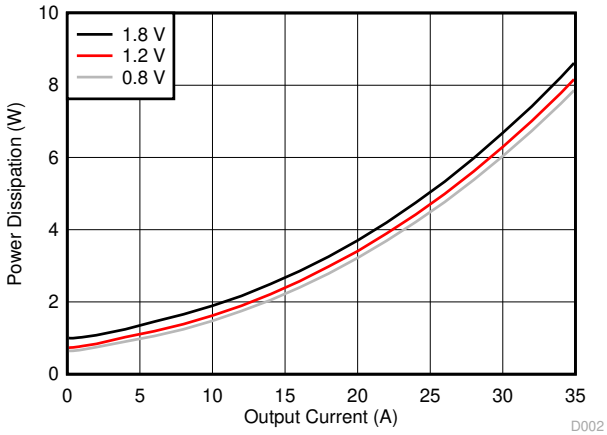

Figure 5-2. Power Dissipation

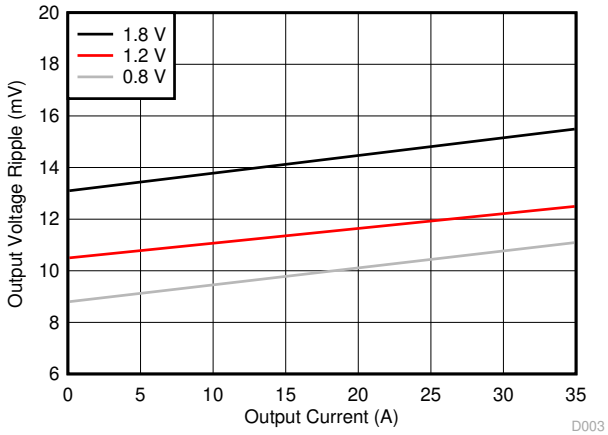

Figure 5-3. Output Voltage Ripple

6 Schematic

Figure 6-1 illustrates the TPSM846C24EVM schematic.

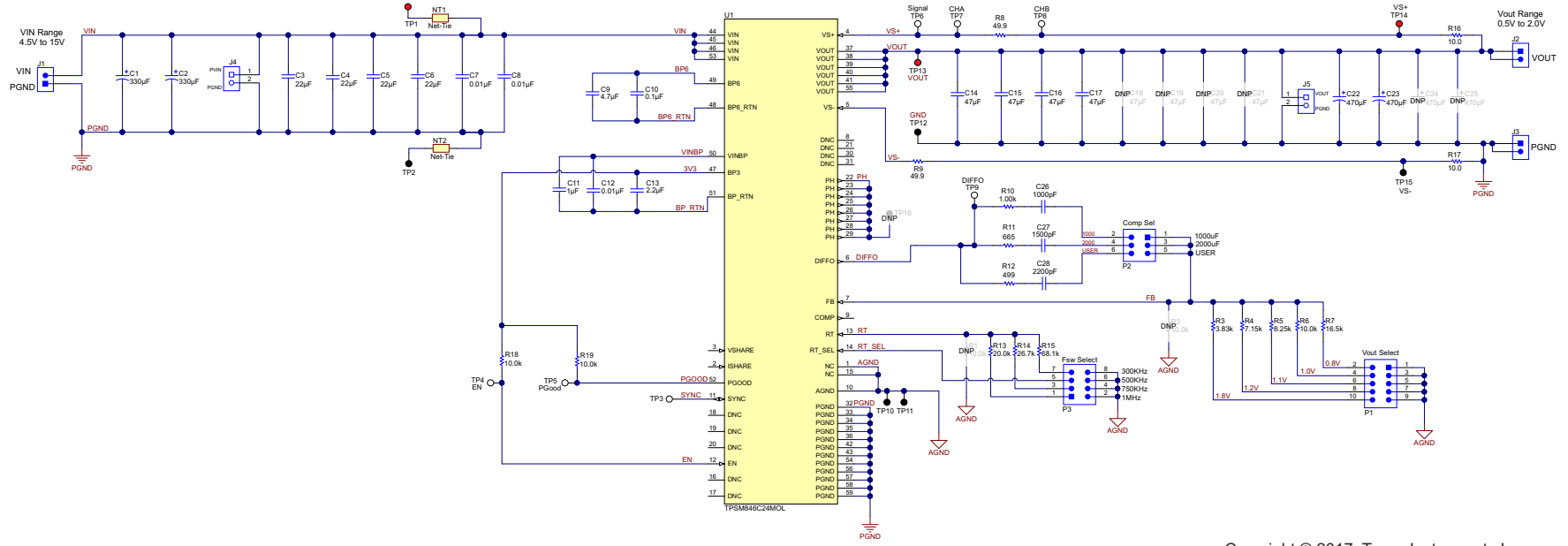

Figure 6-1. TPSM846C24EVM Schematic

7 Bill of Material

Table 7-1 lists the EVM BOM.

Table 7-1. TPSM846C24EVM Bill of Material

Designator	QTY	Description	Part Number	Manufacturer
PCB	1	Printed Circuit Board	74-01196	Any
U1	1	TPSM846C24	TPSM846C24MOL	Texas Instruments
C1, C2	2	CAP, AL, 330 µF, 25 V, ±20%, 0.053 Ω, TH	25ZL330MEFC10X12.5	Rubycon
C3, C4, C5, C6	4	CAP, CERM, 22 µF, 25 V, ±10%, X5R, 1210	GRM32ER61E226KE15L	Murata
C7, C8, C12	3	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	GRM188R71H103KA01D	Murata
C9	1	CAP, CERM, 4.7 µF, 16 V, ±10%, X5R, 0805	GRM21BR61C475KA88L	Murata
C10	1	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0603	GRM188R71C104KA01D	Murata
C11	1	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0805	GRM21BR71E105KA99L	Murata
C13	1	CAP, CERM, 2.2 µF, 16 V, ±10%, X7R, 0805	GRM21BR71C225KA12L	Murata
C14, C15, C16, C17	4	CAP, CERM, 47 µF, 6.3 V, ±20%, X5R, 1210	GRM32ER60J476ME20L	Murata
C22, C23	2	CAP, Tantalum Polymer, 470 µF, 6.3 V, ±20%, 0.01 Ω, 7343-40 SMD	6TPF470MAH	Panasonic
C26	1	CAP, CERM, 1000 pF, 16 V, ±10%, X7R, 0402	GRM155R71C102KA01D	Murata
C27	1	CAP, CERM, 1500 pF, 50 V, ±10%, X7R, 0402	GRM155R71H152KA01D	Murata
C28	1	CAP, CERM, 2200 pF, 50 V, ±10%, X7R, 0402	GRM155R71H222KA01D	Murata
J1, J2, J3	3	Terminal Block, 30 A, 9.52-mm (.375) Pitch, 2-Pos, TH	OSTT7022150	On-Shore Technology
J4, J5	2	Socket Strip, 2 × 1, 100 mil, Black, Tin, TH	310-43-102-41-001000	Mill-Max
P1	1	Header, 100mil, 5x2, Tin, TH	PEC05DAAN	Sullins Connector Solutions
P2	1	Header, 100mil, 3 × 2, Tin, TH	PEC03DAAN	Sullins Connector Solutions
P3	1	Header, 100 mil, 4 × 2, Tin, TH	PEC04DAAN	Sullins Connector Solutions
R3	1	RES, 3.83 k, 1%, 0.063 W, 0402	CRCW04023K83FKED	Vishay-Dale
R4	1	RES, 7.15 k, 1%, 0.063 W, 0402	CRCW04027K15FKED	Vishay-Dale
R5	1	RES, 8.25 k, 1%, 0.063 W, 0402	CRCW04028K25FKED	Vishay-Dale
R6, R18, R19	3	RES, 10.0 k, 1%, 0.063 W, 0402	CRCW040210K0FKED	Vishay-Dale
R7	1	RES, 16.5 k, 1%, 0.063 W, 0402	CRCW040216K5FKED	Vishay-Dale
R8, R9	2	RES, 49.9, 1%, 0.1 W, 0603	CRCW060349R9FKEA	Vishay-Dale
R10	1	RES, 1.00 k, 1%, 0.063 W, 0402	CRCW04021K00FKED	Vishay-Dale
R11	1	RES, 665, 1%, 0.063 W, 0402	CRCW0402665RFKED	Vishay-Dale
R12	1	RES, 499, 1%, 0.063 W, 0402	CRCW0402499RFKED	Vishay-Dale
R13	1	RES, 20.0 k, 1%, 0.063 W, 0402	CRCW040220K0FKED	Vishay-Dale
R14	1	RES, 26.7 k, 1%, 0.063 W, 0402	CRCW040226K7FKED	Vishay-Dale
R15	1	RES, 68.1 k, 1%, 0.063 W, 0402	CRCW040268K1FKED	Vishay-Dale
R16, R17	2	RES, 10.0, 5%, 0.1 W, 0603	CRCW060310R0FKEA	Vishay-Dale
TP1, TP13, TP14	3	Test Point, Multipurpose, Red, TH	5010	Keystone
TP2, TP10, TP11, TP12, TP15	5	Test Point, Multipurpose, Black, TH	5011	Keystone
TP3, TP4, TP5, TP6, TP7, TP8, TP9	7	Test Point, Multipurpose, White, TH	5012	Keystone
C18, C19, C20, C21	0	CAP, CERM, 1210	1210	Murata
C24, C25	0	CAP, Tantalum Polymer, 7343-40 SMD	7343-40	Panasonic
R1, R2	0	RES, 0402	0603	Vishay-Dale

8 PCB Layout

Figure 8-1 through Figure 8-8 display the EVM PCB layout images.

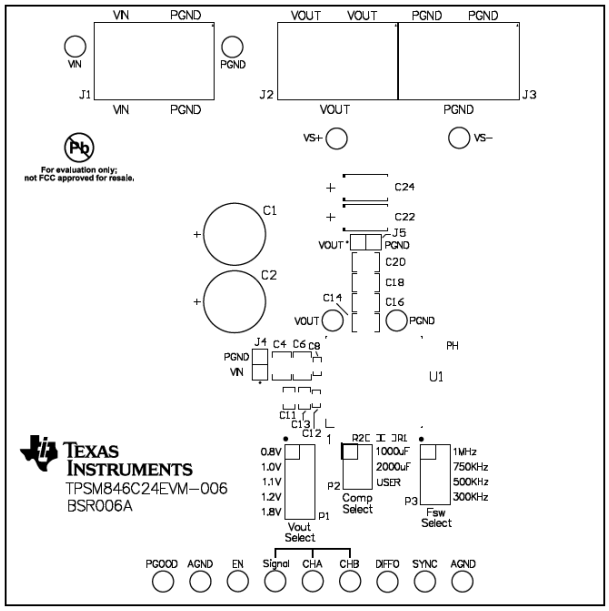

Figure 8-1. Top Components (Top View)

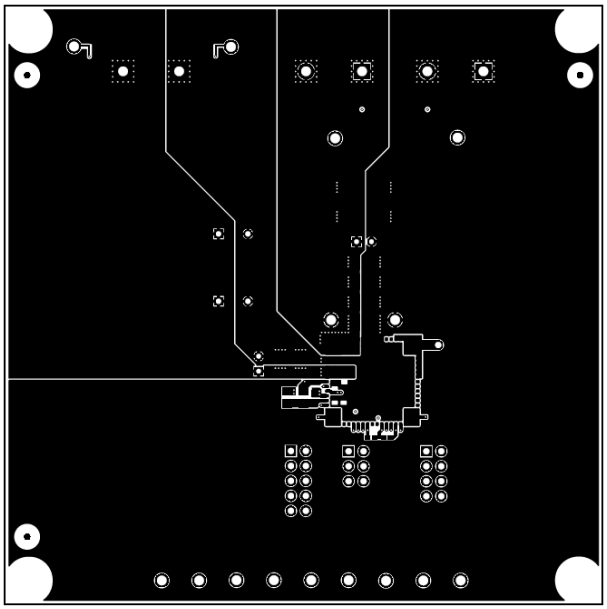

Figure 8-2. Topside Copper (Top View)

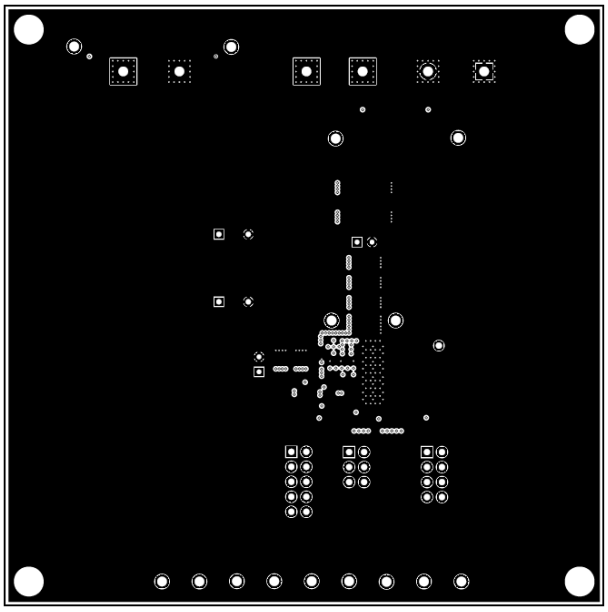

Figure 8-3. Layer 2 Copper (Top View)

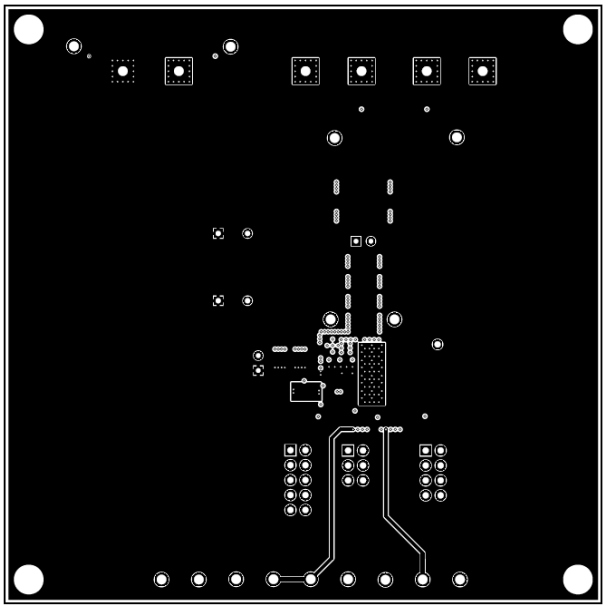

Figure 8-4. Layer 3 Copper (Top View)

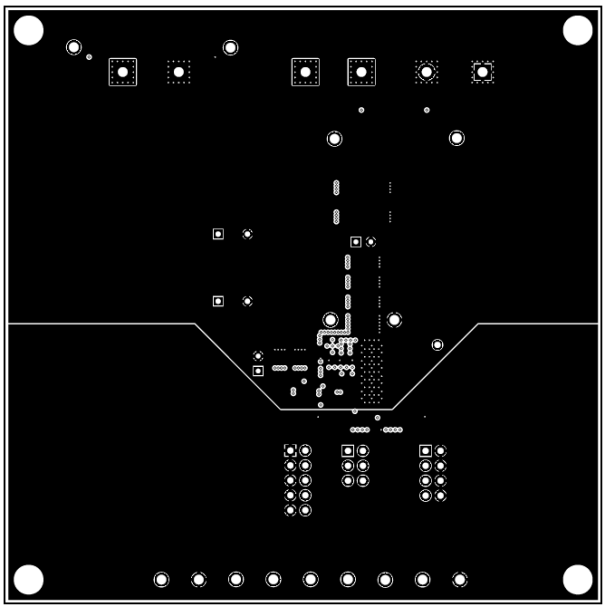

Figure 8-5. Layer 4 Copper (Top View)

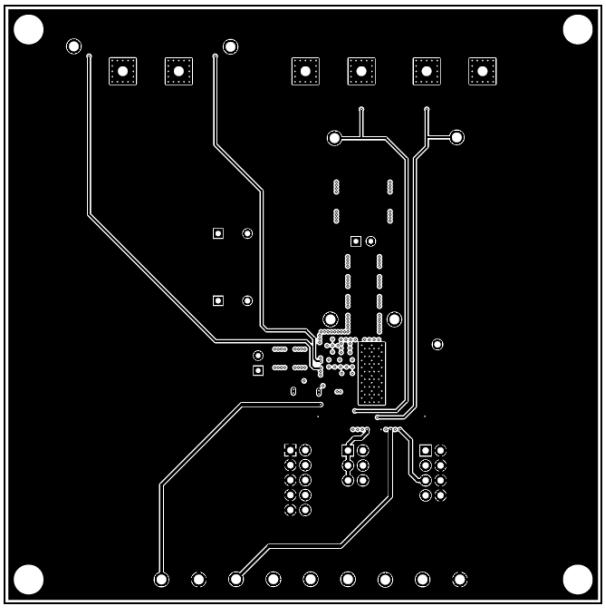

Figure 8-6. Layer 5 Copper (Top View)

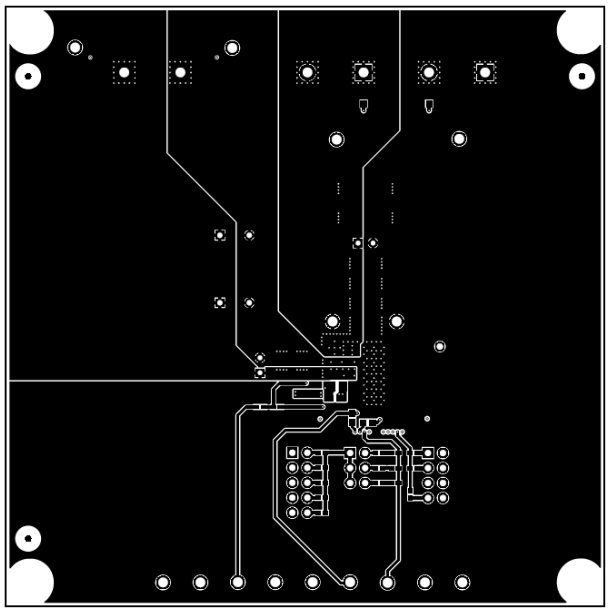

Figure 8-7. Bottom-Side Copper (Top View)

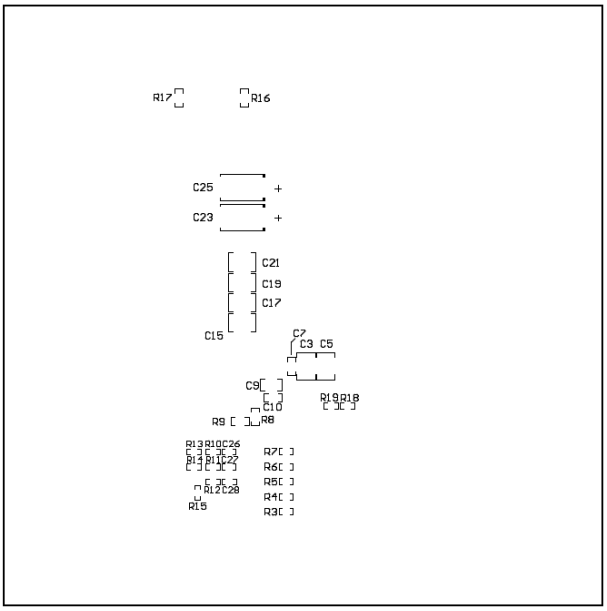

Figure 8-8. Bottom Components (Bottom View)

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2017) to Revision A (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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