TMS320C6000 Expansion Bus to Intel80960Kx/Jx Microprocessor Interface

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ABSTRACT

This application report describes how to interface the Texas Instruments (TI) TMS320C6000™ (C6000™) digital signal processor (DSP) to the Intel 80960Kx/Jx microprocessor. This document contains:

- A block diagram of the interface
- Information required to configure the Intel80960
- Timing diagrams illustrating the interface functionality

Note:
The information presented in this application report has been verified using VHDL simulation.

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1 Intel80960Kx/Jx Interface

The Intel80960Kx/Jx microprocessors have a multiplexed data/address bus similar to the expansion bus. The only glue required is the address decoder that selects the expansion bus. Figure 1 shows the interface between the Intel80960Kx/Jx and the expansion bus. Note that the internal bus arbiter of the expansion bus is disabled. The TMS320C6000 DSP requests the expansion bus only if it needs to access the FIFO or asynchronous I/O port (this is not shown in the block diagram).

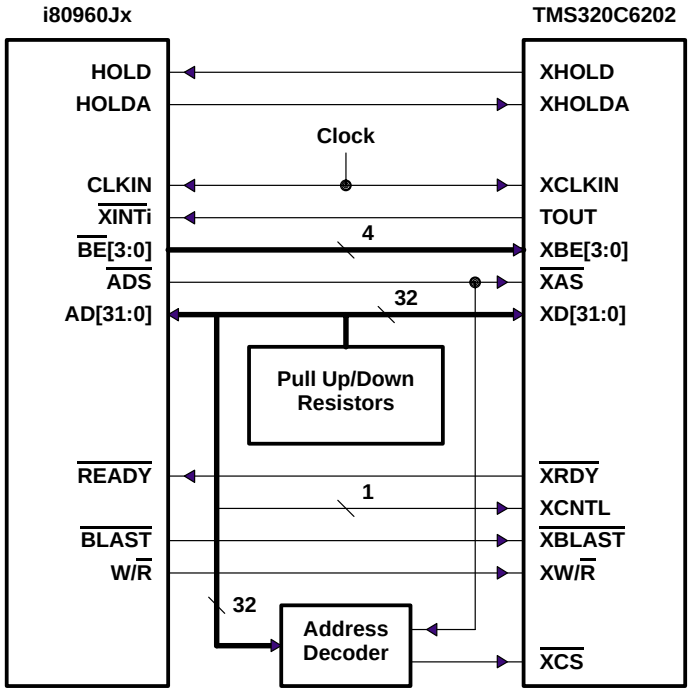

Figure 1. Intel80960Jx to Expansion Bus Interface

Table 1. Intel80960Jx/Kx to Expansion Bus Signal Connections

Expansion Bus Signal	Intel80960Jx/Kx Pin	Comments
XCNTL	A[2]	Address bit of Intel80960 is used as control signal.
$\overline{\text{XBLAST}}$	$\overline{\text{BLAST}}$	Indicates the last transfer in a burst. The polarity of XBLAST (in this case active low) is determined during reset using pull-down resistor on XD[13].
XW/$\overline{\text{R}}$	W/$\overline{\text{R}}$	Indicates a read or write access. The polarity of XW/$\overline{\text{R}}$ is determined during reset using pull-down resistor on XD[12].
XD[31:0]	AD[31:0]	32 bits of data
XHOLD	HOLD	Bus arbitration signal (internal bus arbiter of the expansion bus is disabled).
XHOLDA	HOLDA	Bus arbitration signal (internal bus arbiter of the expansion bus is disabled).
$\overline{\text{XAS}}$	$\overline{\text{ADS}}$	Address strobe indicates the transfer of a physical address.
$\overline{\text{XCS}}$	Address lines are decoded and synchronized using ADS-.	Because the Intel80960Jx/Kx does not have a chip select line, it is necessary to use some decode logic as an input to $\overline{\text{XCS}}$. The XBISA and XBD registers were mapped to locations 0x10000004 and 0x10000000, respectively.
XBE[3:0]	$\overline{\text{BE}}$[3:0]	Expansion bus byte enables
$\overline{\text{XINTi}}$	TOUT	The expansion bus does not have an interrupt pin, so general-purpose output TOUT is used as an interrupt output.
$\overline{\text{XRDY}}$	$\overline{\text{RDYRCV}}$	Ready signal
XCLK	CLKIN	Expansion bus clock

If a 5-V host device is used (for example, the Intel80960Kx), the voltage translation interface is needed. (The voltage translation logic is not shown in the block diagram.)

The C6000 DSP uses the data pins on the expansion bus to latch the configuration word during reset. The configuration word is set using pull-up/down resistors. When in reset, the Intel microprocessor drives the bus; and if the DSP and the i80960Kx/Jx are in reset together, the DSP cannot latch proper configuration values. Therefore, the i80960Kx/Jx has to be reset first. After the i80960Kx/Jx gets out of reset, the HOLD signal has to be sent to the i80960Kx/Jx to ensure that the bus is not driven during the period when the DSP is getting out of reset. This way the i80960Kx/Jx does not interfere with the DSP configuration procedure. The reset circuitry that ensures that the DSP latches the correct configuration word of the expansion bus during reset is not shown in Figure 1.

2 Configuration

The only programmable physical memory attribute for the Intel80960Jx/Kx microprocessor is the bus width, which can be 8-, 16- or 32-bits wide.

For the purposes of assigning memory attributes, the physical address space is partitioned into eight fixed 512-MB regions determined by the upper three address bits. The physical memory attributes for each region are programmable through the PMCON registers. The PMCON registers are loaded from the control table. The Intel80960Jx microprocessor provides one PMCON register for each region.

The bus width for a region is controlled by the BW[1:0] bits in the PMCON register. The BW1 = 1 and BW0 = 0 for the 32-bit expansion-bus interface.

All eight PMCON registers are loaded automatically during system auto-initialization. Immediately after a hardware reset, the PMCON register contents are marked invalid in the bus control (BCON) register. The initial PMCON register values are stored in the control table in the initialization boot record. After hardware reset, the processor first loads all PMCON registers from the control table. The processor then loads BCON from the control table. The BCON.ctv bit in BCON must be set to use the programmed PMCON values for each memory region.

The default logical memory configuration register (DLMCON) provides default logical memory control for those accesses not falling within a region defined by the logical memory control register pairs. On the Intel80960Jx, the byte order programmed in the DLMCON register controls byte ordering for the entire 32-bit memory space. The DCEN bit field of the DLMCON register must be set to zero to disable data caching. The BE bit field of the DLMCON register must be set to zero to enable little-endian byte order for all accesses.

The interrupt controller register of the Intel80960Jx processors controls basic functionality such as interrupt mode, signal detection, global enable/disable, mask operation, interrupt vector caching, and sampling mode (for more detailed information on interrupt configuration, please see the *i960 Jx Microprocessor User's Manual*).

The Timers chapter in the *TMS320C6000 Peripherals Reference Guide* (SPRU190) describes how to configure timer pins for general-purpose input and output (Tout is used to generate an interrupt to the host microprocessor.).

The TMS320C6000 DSP boot configuration is presented in Table 2.

Table 2. TMS320C6000 Boot Configuration via Pull-Up/Pull-Down Resistors on XD[31:0]

Field	Description
BLPOL	Determines polarity of /XBLAST signal BLPOL = 0, XBLAST is active low.
RWPOL	Determines polarity of expansion bus read/write signal RWPOL = 0, XW/$\overline{R}$
HMOD	Host mode (status in XB HPIC) HMOD = 1, external host interface is in synchronous master/slave mode
XARB	Expansion bus arbiter (status in XBGC) XARB = 0, internal expansion bus arbiter is disabled.
FMOD	FIFO mode (status in XBGC)
LEND	Little-endian mode LEND = 1, system operates in little-endian mode
BootMode[4:0]	Dictates the boot mode of the device, including host port boot, ROM boot, memory map selection. For a complete list of boot modes, see the *TMS320C6000 Peripherals Reference Guide* (SPRU190).

3 Timing Verification

To verify proper operation, two functions have been examined:

1. An Intel80960JD write to the expansion bus

2. An Intel80960JD read from the expansion bus

In each instance, timing requirements were compared for each of the devices and the results are shown in Figure 2, Figure 3, Table 3, and Table 4.

The interface was functionally verified using VHDL simulation (Synopsys SmartModel of the Intel80960KA was used in the test bench). The timing diagrams shown in Figure 2 and Figure 3 are outputs from the simulation. The clock ratio between the operating frequency of the TMS320C6202 and the XCLKIN frequency was set to 7.5.

Note that the expansion bus timing parameters for the TMS320C6202, C6202B, C6203, and C6204 are similar.

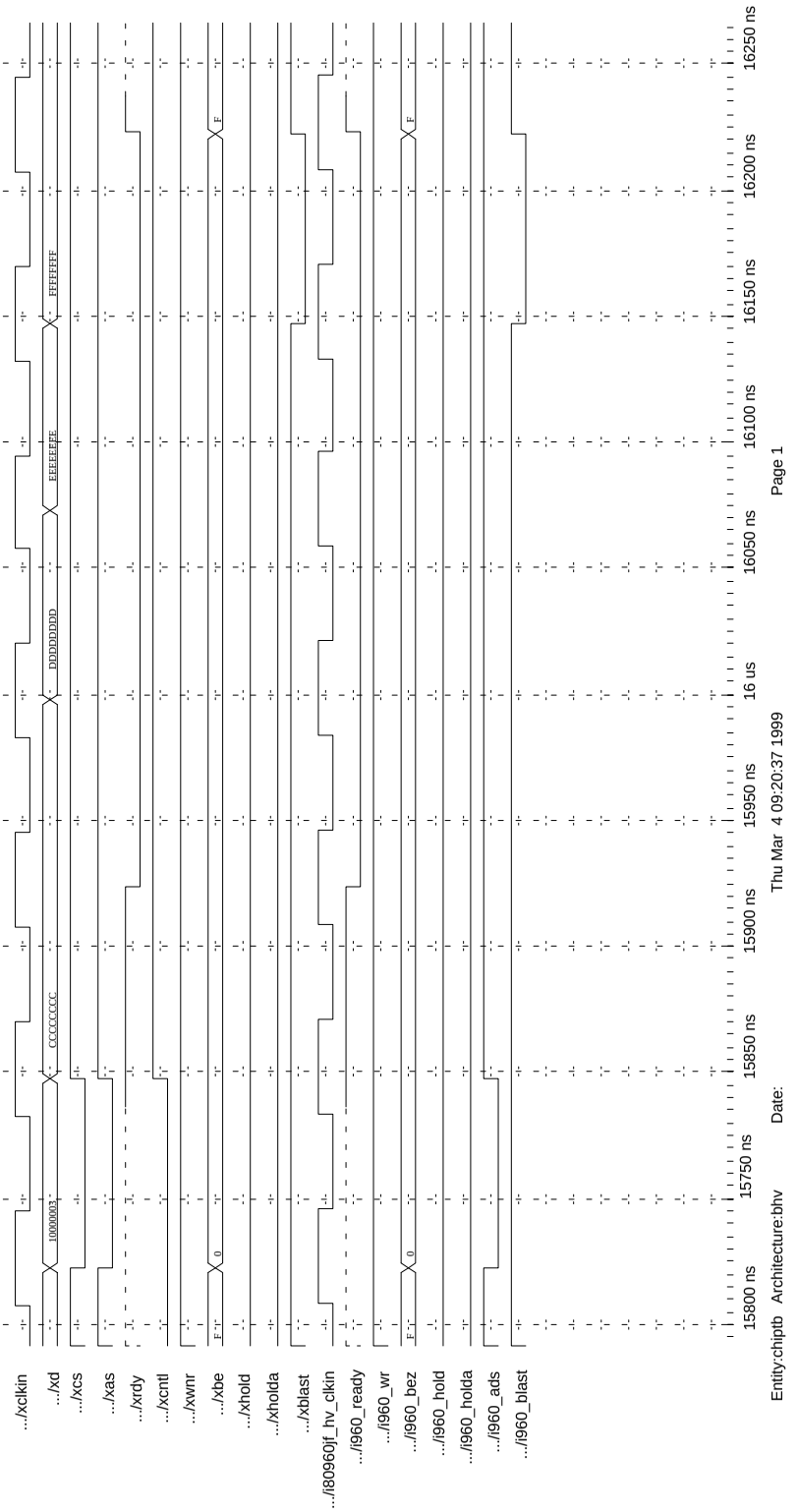

Figure 2. Burst Write Initiated by Intel80960Kx/Jx to Expansion Bus

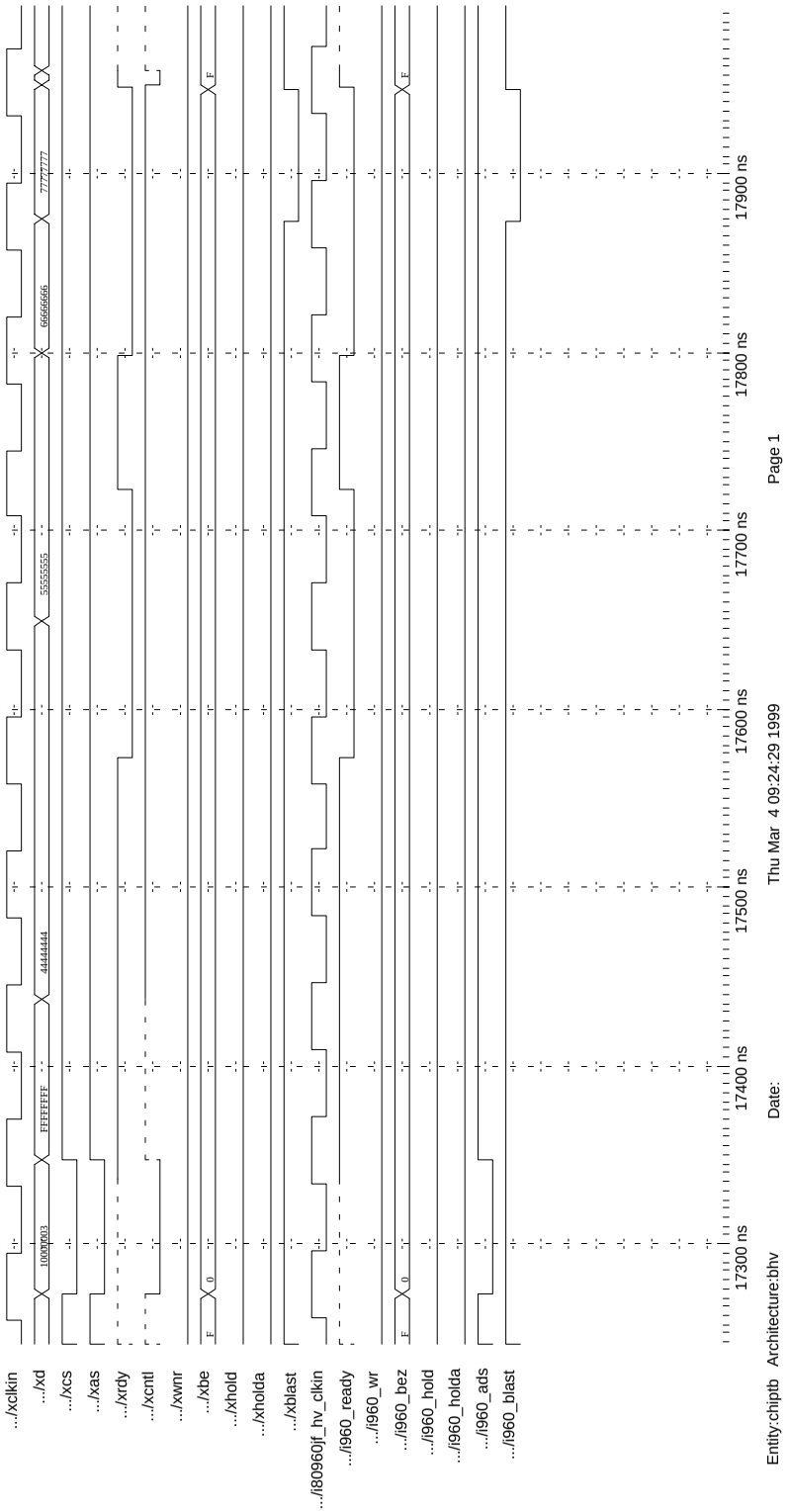

Figure 3. Burst Read Initiated by Intel80960Kx/Jx to Expansion Bus

Table 3. Timing Requirements for TMS320C6000 (Intel80960JD Expansion Bus Master)

Intel80960JD Symbol	C6000 Symbol	Parameter	Intel80960JD Min (ns)	C6000* Min (ns)
Tcyc-tOV1-tPAL	Tsu(XCSV-XCKIH)	Chip-select (XCS) valid before XCLKIN high	11.5	3.5
tOV1+tPAL	Th(XCKIH -XCSV)	Chip-select (XCS) valid after XCLKIN high	7.5	2.8
Tcyc-tOV1	Tsu(XASV-XCKIH)	Address strobe (XAS) valid before XCLKIN high	16.5	3.5
TOV1	Th(XCKIH-XASV)	Address strobe (XAS) valid after XCLKIN high	13.5	2.8
Tcyc-tOV1	Tsu(XBLTV-XCKIH)	Burst last (XBLAST) valid before XCLKIN high	16.5	3.5
TOV1	Th(XCKIH-XBLTV)	Burst last (XBLAST) valid after XCLKIN high	13.5	2.8
Tcyc-tOV1	Tsu(XD-XCKIH)	Data (XD) valid before XCLKIN high (WRITE)	16.5	3.5
TOV1	Th(XCKIH-XD)	Data (XD) valid after XCLKIN high (WRITE)	13.5	2.8
Tcyc-tOV1	Tsu(XBEV-XCKIH)	Byte enable (XBE[3:0]) valid before XCLKIN high	16.5	3.5
TOV1	Th(XCKIH-XBEV)	Byte enable (XBE[3:0]) valid after XCLKIN high	13.5	2.8
Tcyc-tOV1	Tsu(XWR-XCKIH)	Read/write (XR/W) valid before XCLKIN high	16.5	3.5
TOV1	Th(XCKIH-XWR)	Read/write (XR/W) valid after XCLKIN high	13.5	2.8

* C6000 in this case refers to C6202, C6202B, C6203, and C6204.

Table 4. Timing Requirements for i960JD (i960JD Expansion Bus Master)

Intel80960JD Symbol	C6000 Symbol	Parameter	Intel80960JD Min (ns)	C6000* Min (ns)
TIS2	Tcyc-Td(XCKIH-XRY)	Ready signal (RDYRCV) valid before XCLKIN high	6.5	14.5
TIH2	Td(XCKIH-XRY)	Ready signal (RDYRCV) valid after XCLKIN high	1	5
TIS1	Tcyc-Td(XCKIH-XDV)	Data (XD) valid before XCLKN high (READ)	6	14.5
TIH1	Td(XCKIH-XDIV)	Data (XD) invalid after XCLKIN high (READ)	1.5	5

* C6000 in this case refers to C6202, C6202B, C6203, and C6204.

The timing tables above show that the timing parameters for both devices are met in the interface of Intel80960JD and TMS320C6202. This interface is based on the Intel80960JD (local bus is running at 33 MHz) and the TMS320C6000 device (C6202, C6202B, C6203, and C6204) at any frequency ranging from 100 MHz-250 MHz.

4 References

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
2. *TMS320C6202, TMS320C6202B Fixed-Point Digital Signal Processors* (SPRS104).
3. *TMS320C6204 Fixed-Point Digital Signal Processor* (SPRS152).
4. *I960 Jx Microprocessor User's Manual*, Order #272483, Intel Corporation.

Appendix A i80960 Timing Requirements

Table A–1. Intel 80960JD Timing Parameters

Characteristic	Symbol	Min (ns)	Max (ns)
Output valid delay, except ALE inactive and DT/R- for 3.3-V input signals	tOV1	2.5	13.5
Output float delay	tOF	2.5	13.5
input setup to CLKIN- AD[31:0]	tIS1	6	
Input hold from CLKIN AD[31:0]	tIH1	1.5	
Input setup to CLKIN RDYRCV-	tIS2	6.5	
Input hold from CLKIN RDYRCV-	tIH2	1	
Address valid to ALE Inactive	tLX	10	
ALE width	tLXL	8	
Address hold from ALE inactive	tLXA	8	
DT/R- valid to DEN- active	tDXD	8	

The timing requirements in Table A–1 are provided for quick reference only. For detailed description, notes, and restrictions, please see the *I960JD Microprocessor User's Manual*.

Appendix B TMS320C6000 Timing Parameters

Table B–1. TMS320C6202/C6202B/C6203/C6204 Timing Parrameters (External Device is a Master)

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, XCS valid before XCLKIN high	Tsu(XCSV-XCKIH)	3.5	
Hold time, XCS valid after XCLKIN high	Th(XCKIH-XCSV)	2.8	
Setup time, XAS valid before XCLKIN high	Tsu(XASV-XCKIH)	3.5	
Hold time, XAS valid after XCLKIN high	Th(XCKIH-XASV)	2.8	
Setup time, XCNTL valid before XCLKIN high	Tsu(XCTL-XCKIH)	3.5	
Hold time, XCNTL valid after XCLKIN high	Th(XCKIH-XCTL)	2.8	
Setup time, XWR valid before XCLKIN high	Tsu(XWR-XCKIH)	3.5	
Hold time, XWR valid after XCLKIN high	Th(XCKIH-XWR)	2.8	
Setup time, XBLAST valid before XCLKIN high	Tsu(XBLTV-XCKIH)	3.5	
Hold time, XBLAST valid after XCLKIN high	Th(XCKIH-XBLTV)	2.8	
Setup time, XBE valid before XCLKIN high	Tsu(XBEV-XCKIH)	3.5	
Hold time, XBE valid after XCLKIN high	Th(XCKIH-XBEV)	2.8	
Setup time, XD valid before XCLKIN high	Tsu(XD-XCKIH)	3.5	
Hold time, XD valid after XCLKIN high	Th(XCKIH-XD)	2.8	
Delay time, XCLKIN high to XD low impedance	Td(XCKIH-XDLZ)	0	
Delay time, XCLKIN high to XD valid	Td(XCKIH-XDV)		16.5
Delay time, XCLKIN high to XD invalid	Td(XCKIH-XDIV)	5	
Delay time, XCLKIN high XD high impedance	Td(XCKIH-XDHZ)		4P
Delay time, XCLKIN high to XRDY valid	Td(XCKIH-XRY)	5	16.5

Table B–2. TMS320C6202/C6202B/C6203/C6204 Timing Parameters (TMS320C620x is a Master)

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, XD valid before XCLKIN high	Tsu(XDV-XCKIH)	3.5	
Hold time, XD valid after XCLKIN high	Th(XCKIH-XDV)	2.8	
Setup time, XRDY valid before XCLKIN high	Tsu(XRY-XCKIH)	3.5	
Hold time, XRDY valid after XCLKIN high	Th(XCKIH-XRY)	2.8	
Setup time, XBOFF valid before XCLKIN high	Tsu(XBFF-XCKIH)	3.5	
Hold time, XBOFF valid after XCLKIN high	Th(XCKIH-XBFF)	2.8	
Delay time, XCLKIN high to XAS valid	Td(XCKIH-XAS)	5	16.5
Delay time, XCLKIN high to XWR valid	Td(XCKIH-XWR)	5	16.5
Delay time, XCLKIN high to XBLAST valid	Td(XCKIH-XBLTV)	5	16.5
Delay time, XCLKIN high to XBE valid	Td(XCKIH-XBEV)	5	16.5
Delay time, XCLKIN high to XD low impedance	Td(XCKIH-XDLZ)	0	
Delay time, XCLKIN high to XD valid	Td(XCKIH-XDV)		16.5
Delay time, XCLKIN high to XD invalid	Td(XCKIH-XDIV)	5	
Delay time, XCLKIN high to XD high impedance	Td(XCKIH-XDHZ)		16
Delay time, XCLKIN high to XWE/XWAIT valid	Td(XCKIH-XWTV)	5	16.5

The timing parameters in Table B–1 through Table B–2 are provided for quick reference only. For detailed description, notes, and restrictions, please see the corresponding *Fixed-Point Digital Signal Processor* data sheet.

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