Implementing DDR2 PCB Layout on the TMS320C6421 DSP

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High Speed HW Productization

ABSTRACT

This application report contains implementation instructions for the DDR2 interface contained on the TMS320C6421 digital signal processor (DSP) device. The approach to specifying interface timing for the DDR2 interface is quite different than on previous devices.

The previous approach specified device timing in terms of data sheet specifications and simulation models. The system designer was required to obtain compatible memory devices, as well as the device-specific data sheets and simulation models. This information would then be used to design the printed circuit board (PCB) using high-speed simulation to close system timing.

For the C6421 DDR2 interface, the approach is to specify compatible DDR2 devices and provide the PCB routing rule solution directly. TI has performed the simulation and system design work to ensure DDR2 interface timings are met. This document describes the required routing rules.

The C6424 EVM provides an example of a PCB layout following these routing rules that passes FCC EMI requirements. You may copy the DDR2 portion of this layout directly, but the intent is to allow enough flexibility in the routing rules to meet other PCB requirements.

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1 TMS320C6421

1.1 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding guidelines for using this DDR2 specification, *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0).

1.1.1 DDR2 Interface Schematic

Table 2 shows the DDR2 interface schematic for a x16 DDR2 memory system. Pin numbers for the C6421 can be obtained from the pin description section of the *TMS320C6421 Fixed-Point Digital Signal Processor Data Manual* (SPRS346) and the DDR2 device pin numbers can be obtained from their device-specific data sheets.

1.2 Compatible JEDEC DDR2 Devices

Table 1 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-400 speed grade DDR2 devices.

Table 1. Compatible JEDEC DDR2 Devices

No.	Parameter	Min	Max	Unit	Notes
1	JEDEC DDR2 Device Speed Grade	DDR2-400			See Note [1]
2	JEDEC DDR2 Device Bit Width	x16	x16	Bits	
3	JEDEC DDR2 Device Count	1	1	Device	
4	JEDEC DDR2 Device Ball Count	84	92	Balls	See Note [2]

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
(2) 92 ball devices retained for legacy support. New designs will migrate to 84 ball DDR2 devices. Electrrically the 92 and 84 ball DDR2 devices are the same.

1.3 PCB Stackup

The minimum stackup required for routing the C6421 is a six layer stack as shown in Table 2. Additional layers may be added to the PCB stack up to accommodate other circuity or to reduce the size of the PCB footprint.

Table 2. C6421 Minimum PCB Stack Up

Layer	Type	Description
1	Signal	Top Routing Mostly Horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing Mostly Vertical

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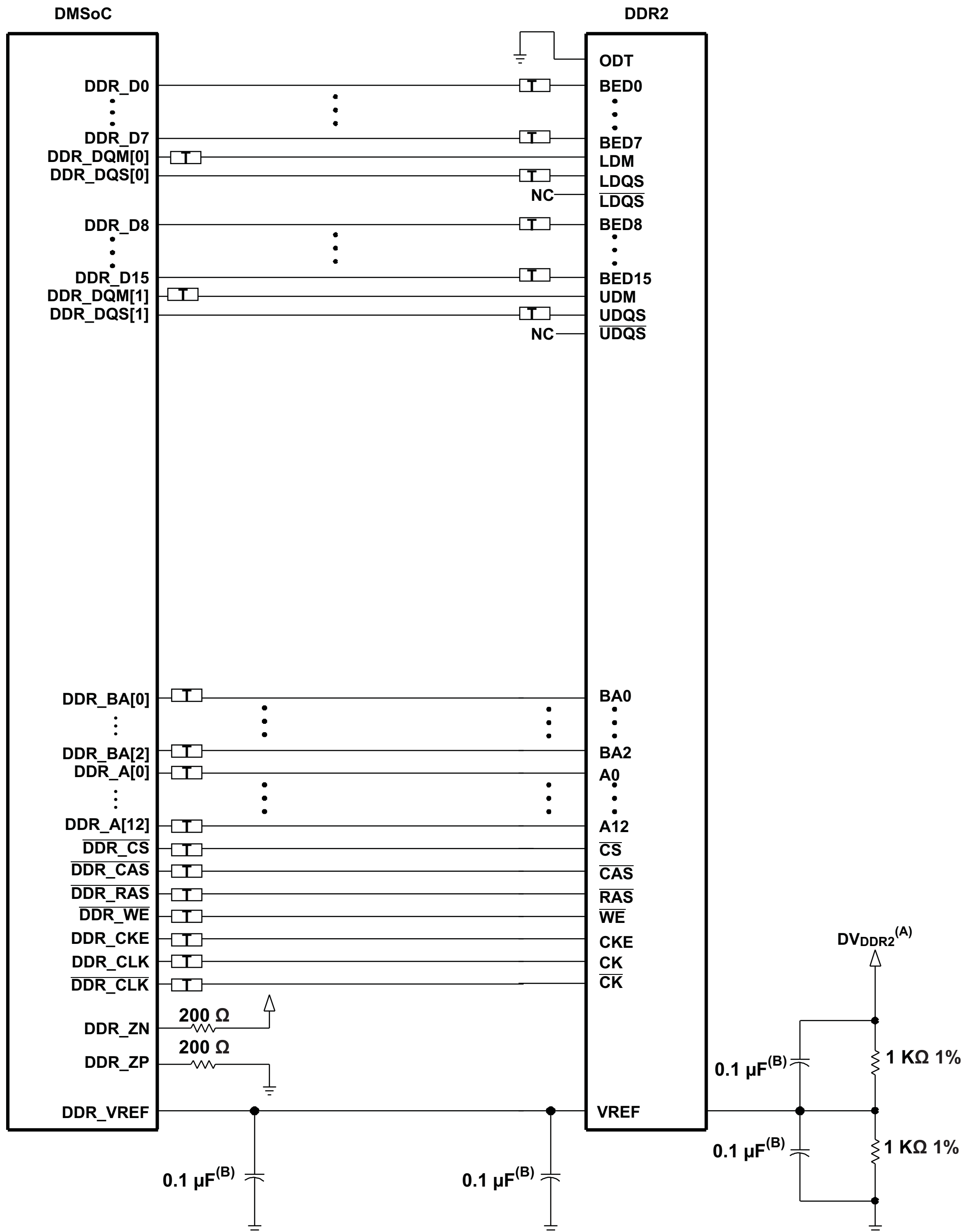

NOTES: A. DV_{DDR2} is the power supply for the DDR2 memory and DMSoC DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin.

T Terminaror, if desired See terminato comments

Figure 1. C6421 16-Bit DDR2 High Level Schematic

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1.3.1 Minimizing PCB Area

The maximum placement and minimum PCB stackup uses the lowest cost PCB technology and generally results in the lowest unit cost PCB at the penalty of the largest footprint for the DDR2 interface. Customers need to evaluate the cost/benefit tradeoffs of smaller feature sizes and additional signal layers for their systems. Note that the minimum feature size and stackup may be limited by other circuitry on the PCB.

Complete stack up specifications are provided in Table 3.

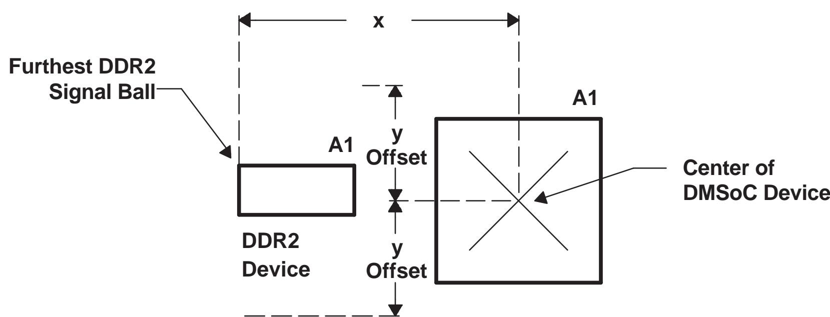
Table 3. PCB Stack Up Specifications

No.	Parameter	Min	Typ	Max	Unit	Notes
1	PCB Routing/Plane Layers	6				
2	Signal Routing Layers	3				
3	Full ground layers under DDR2 routing Region	2				
4	Number of ground plane cuts allowed within DDR routing region			0		
5	Number of ground reference planes required for each DDR2 routing layer	1				
6	Number of layers between DDR2 routing layer and reference ground plane			0		
7	PCB Routing Feature Size		4		Mils	
8	PCB Trace Width w		4		Mils	
8	PCB BGA escape via pad size		18		Mils	
9	PCB BGA escape via hole size		8		Mils	
10	DSP Device BGA pad size					See Note (1)
11	DDR2 Device BGA pad size					See Note (2)
12	Single Ended Impedance, Zo	50		75	Ω	
13	Impedance Control	Z-5	Z	Z+5	Ω	See Note (3)

(1) Please refer to the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811) for DSP device BGA pad size.
(2) Please refer to the DDR2 device manufacturer documenation for the DDR2 device BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

1.3.2 Placement

Figure 2 shows the required placement for the C6421 device as well as the DDR2 device. The dimensions for Figure 2 are defined in Table 4. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space.



Maximum placement distances from center of DMSoC package to furthest DDR2 signal ball. Does not include distances to possible DDR2 NC outrigger balls. All dimensions in mils.

Figure 2. C6421 and DDR2 Device Placement Specification (16-bit connection)

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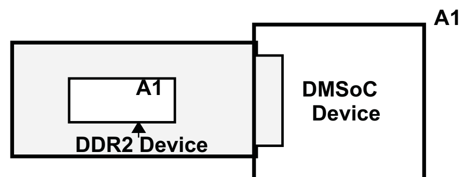
Table 4. Placement Specifications

No.	Parameter	Min	Max	Unit	Notes
1	X		1750	Mils	See Notes [1], [2]
2	Y		1280	Mils	See Notes [1], [2]
3	Y Offset		700	Mils	See Notes [1], [2], [3]
4	DDR2 Keepout Region				See Note [4]
5	Clearance from non-DDR2 signal to DDR2 Keepout Region	4		w	See Note [5]

(1) See Figure 2 for dimension defintions.
(2) Measurements from center of DSP device to center of DDR2 device.
(3) It is recommended that Y Offset be as small as possible.
(4) DDR2 Keepout region to encompass entire DDR2 routing area
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

1.3.3 DDR2 Keep Out Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keep out region is defined for this purpose and is shown in Figure 3. The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are shown in Table 4.



Region should encompass all DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keep out region. Non-DDR2 signals may be routed in this region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.

Figure 3. Example DDR2 Keep Out Region

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1.3.4 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 5 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DSP and DDR2 interface. Additional bulk bypass capacitance may be needed for other circuitry.

Table 5. Bulk Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	DV_{DD18} Bulk Bypass Capacitor Count	2		Devices	See Note [(1)]
2	DV_{DD18} Bulk Bypass Total Capacitance	44		μF	
3	DDR Bulk Bypass Capacitor Count	1		Devices	See Note [(1)]
4	DDR Bulk Bypass Total Capacitance	22		μF	

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.

1.3.5 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, DSP/DDR power, and DSP/DDR ground connections. Table 6 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

1.3.6 Net Classes

Table 7 lists the clock net classes for the DDR2 interface. Table 8 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

Table 6. High-Speed Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	HS Bypass Capacitor Package Size		0402	10 Mils	See Note [(1)]
2	Distance from HS bypass capacitor to device being bypassed		250	Mils	
3	Number of connection vias for each HS bypass capacitor	2		Vias	See Note [(2)]
4	Trace length from bypass capacitor contact to connection via	1	30	Mils	
5	Number of connection vias for each DDR2 device power or ground balls	1		Vias	
6	Trace length from DDR2 device power ball to connection via		35	Mils	
7	DV_{DD18} HS Bypass Capacitor Count	8		Devices	See Note [(3)]
8	DV_{DD18} HS Bypass Capacitor Total Capacitance	0.8		μF	
9	DDR HS Bypass Capacitor Count	8		Devices	See Note [(3)]
10	DDR HS Bypass Capacitor Total Capacitance	0.8		μF	

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.

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Table 7. Clock Net Class Definitions

Clock Net Class	DSP Pin Names
CK	DDR_CLK/DDR_CLK
DQS0	DDR_DQS0
DQS1	DDR_DQS1

Table 8. Signal Net Class Definitions

Clock Net Class	Associated Clock Net Class	DSP Pin Names
ADDR_CTRL	CK	DDR_BA[2:0], DDR_A[12:0], DDR_CS, DDR_CAS, DDR_RAS, DDR_WE, DDR_CKE
DQ0	DQS0	DDR_D[7:0], DDR_DQM0
DQ1	DQS1	DDR_D[15:8], DDR_DQM1

1.3.7 DDR2 Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 9 shows the specifications for the series terminators.

Table 9. DDR2 Signal Terminations

No.	Parameter	Min	Typ	Max	Unit	Notes
1	CK Net Class	0		10	Ω	See Note [1]
2	ADDR_CTRL Net Class	0	22	Zo	Ω	See Notes [1], [2], [3]
3	Data Byte Net Classes (DQS0-DQS1, DQ0-DQ1)	0	22	Zo	Ω	See Notes [1], [2], [3], [4]

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.
(4) When no termination is used on data lines (0 Ωs), the DDR2 device must be programmed to operate in 60% strength mode.

1.3.8 VREF Routing

VREF is used as a reference by the input buffers of the DDR2 memories as well as the C6421's. VREF is intended to be 1/2 the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 1. Other methods of creating VREF are not recommended. Figure 4 shows the layout guidelines for VREF.

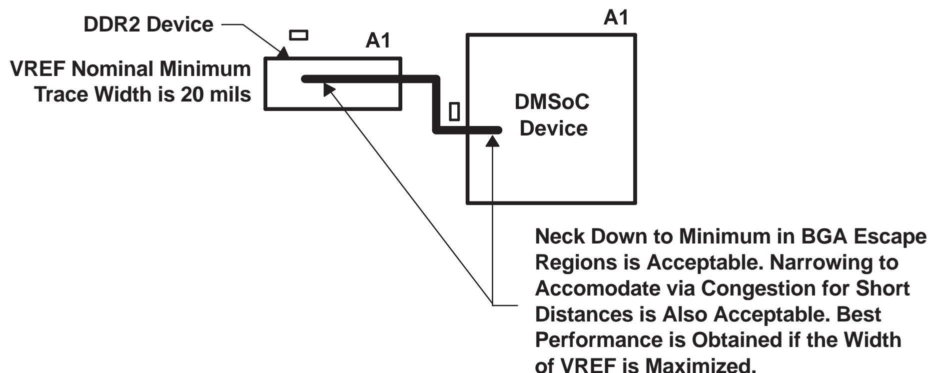

Figure 4. VREF Specification 16-Bit Interface

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1.3.9 DDR2 CK and ADDR_CTRL Routing

Figure 5 shows the topology of the routing for the CK and ADDR_CTRL net classes.

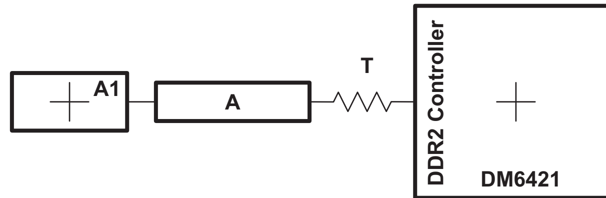

Figure 5. CK and ADDR_CTRL Routing and Topology

Table 10. CK and ADDR_CTRL Routing Specification [(1)]

No	Parameter	Min	Typ	Max	Unit	N otes
1	Center to center CK-$\overline{CK}$ spacing			2w		
2	Center to center CK to other DDR2 trace spacing	4w				See Notes [(2)], [(1)]
3	CK/ADDR_CTRL nominal trace length	CACLM-50	CACLM	CACLM+50	Mils	See Note [(3)]
4	ADDR_CTRL to CK Skew Length Mismatch			100	Mils	
5	ADDR_CTRL to ADDR_CTRL Skew Length Mismatch			100	Mils	
6	Center to center ADDR_CTRL to other DDR2 trace spacing	4w				See Note [(2)]
7	Center to center ADDR_CTRL to other ADDR_CTRL trace spacing	3w				See Note [(2)]

(1) Series terminator, if used, should be located closest to DSP.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 6 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

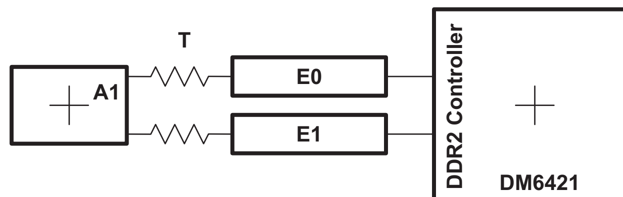

Figure 6. DQS and DQ Routing and Toplogy

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Table 11. DQS and DQ Routing Specification [1]

No.	Parameter	Min	Typ	Max	Unit	Notes
1	Center to center DQS-$\overline{DQS}$ spacing			2w		
2	DQS E Skew Length Mismatch			25	Mils	
3	Center to center DQS to other DDR2 trace spacing	4w				See Note [2]
4	DQS/DQ nominal trace length	DQLM-50	DQLM	DQLM+50	Mils	See Notes [1], [3]
5	DQ to DQS Skew Length Mismatch			100	Mils	See Note [3]
6	DQ to DQ Skew Length Mismatch			100	Mils	See Note [3]
7	Center to center DQ to other DDR2 trace spacing	4w				See Notes [2], [4]
8	Center to Center DQ to other DQ trace spacing	3w				See Note [2]
9	DQ/DQS E Skew Length Mismatch			100	Mils	See Note [3]

(1) Series terminator, if used, should be located closest to DDR.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) There is no need and it is not recommended to skew match across data bytes, ie from DQS0 and data byte 0 to DQS1 and data byte 1.
(4) DQ's from other DQS domains are considered *other DDR2 trace*.

2 References

- *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0)
- *TMS320C6421 Fixed-Point Digital Signal Processor Data Manual* (SPRS346)
- *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811)

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