Application Report
SPRAAT9A–February 2008–Revised October 2009

TMS320C6472/TMS320TCI6486 Serial RapidIO Implementation Guidelines

Thomas Johnson *Digital Signal Processing Solutions*

ABSTRACT

This application report contains implementation instructions for the Serial RapidIO® (SRIO) interface on the TMS320TCI6486/TMS320C6472 DSP device. The approach to specifying interface timing and physical requirements for the SRIO interface is quite different than previous approaches for other interfaces.

Serial RapidIO is an industry-standard, high-speed, switched-packet interconnect. Physical layer data transmission utilizes analog serializer/deserializers (SERDES) to feed low-output-swing differential CML buffers. Proper printed circuit board (PCB) design for this interface resembles analog or RF design and is very different than traditional parallel digital bus design.

Due to this analog nature of the SRIO, it is not possible to specify the interface in a traditional DSP digital-interface manner. Furthermore, it is undesirable to specify the interface in terms of the raw physical requirements laid out by the SRIO specification. Understanding the SRIO specification and producing a compliant PCB based on the explicit and implicit requirements there demands significant time, experience, and expensive tools.

For the TMS320TCI6486/TMS320C6472 SRIO interface, the approach is to reduce the specification to a set of easy-to-follow PCB routing rules. TI has performed the simulation and system design work to ensure SRIO interface requirements are met. This document describes the content of this SRIO implementation.

Contents

List of Tables

1 Prerequisites

The goal of the TCI6486/C6472 collateral is to make system implementation easier for the customer by providing the system solution. For this Serial RapidIO (SRIO) interface, it is not assumed that the system designer is familiar with SRIO, serializer-deserializer (SERDES) technology, or RF/microwave PCB design. However, it is still expected that the PCB design work be supervised by a knowledgeable high-speed digital PCB designer and an assumption is made that the PCB designer is using established high-speed design rules.

2 TMS320TCI6486/TMS320C6472 Supported Serial RapidIO Devices

Serial RapidIO is an industry-standard high-speed switched-packet interconnect. The Serial RapidIO specification allows a device to connect to any other device, so long as the two devices conform to a common physical-layer specification. TI DSPs support connecting to any Serial RapidIO device that complies with the Serial RapidIO specification revision 1.2 or later.

3 PCB Routing Rules

3.1 Example PCB Stackup

A stackup for a 16-layer board is shown in Table 1. This stackup was used on a development board for the TCI6486/C6472. It contains several signal routing layers since all of the peripheral interfaces were implemented. Similarly, this required all I/O power inputs to be supplied as well. The number of layers could be reduced by enlarging the board to spread out the DSPs, thus reducing routing congestion. However, for a relatively dense packing of DSPs in a DSP farm arrangement, a stackup similar to the one below is expected to be needed.

Table 1. Board Stackup

	Use	Description	Thickness
Layer 1	Signal	Pin escapes, non-critical routes	2.1
FR4			6.5
Layer 2	Power	Core power plane	1.4
FR4			3
Layer 3	GND	Solid ground plane	1.4
FR4			6.5
Layer 4	Signal	Critical routing	0.7
FR4			6.5
Layer 5	GND	Solid ground plane	1.4
FR4			6.5
Layer 6	Signal	Critical routing	0.7
FR4			6.5
Layer 7	Power	I/O power planes	1.4
FR4			4
Layer 8	Signal	Vertical signal routing	0.7
FR4			3
Layer 9	Signal	Horizontal signal routing	0.7
FR4			4
Layer 10	Power	I/O power planes	1.4
FR4			6.5
Layer 11	Signal	Critical routing	0.7
FR4			6.5
Layer 12	GND	Solid ground plane	1.4
FR4			6.5

Table 1. Board Stackup (continued)

	Use	Description	Thickness
Layer 13	Signal	Critical routing	0.7
FR4			6.5
Layer 14	GND	Solid ground plane	1.4
FR4			3
Layer 15	Power	Core power plane	1.4
FR4			6.5
Layer 16	Signal	Pin escape breakout, non-critical routes	2.1
		Total	**101.6**

3.2 General Trace/Space and Via Sizes

The key concern for Serial RapidIO signal traces is to achieve 100-Ω differential impedance. This differential impedance is impacted by trace width, trace spacing, distance between planes, and dielectric material. Verify with a proper PCB manufacturing tool that the trace geometry for all SRIO traces results in exactly 100-Ω differential impedance.

Of secondary concern is the insertion loss caused by the traces. Due to the skin effect, wider traces will have lower losses than narrower ones. Therefore, longer SRIO runs should use wider traces for lower loss. However, layers in the stackup that are set to 100-Ω differential impedance with wider traces may be less desirable for routing other signals. Table 2 shows recommendations for minimum trace width by SRIO signal run length.

Table 2. Minimum Trace Width

Signal Run Length, up to	Minimum Trace Width
10 in/25 cm	4 mil/0.1 mm
20 in/50 cm	6 mil/0.15 mm
30 in/75 cm	8 mil/0.2 mm

The PCB defined in the stackup (Table 1) was routed for most signals using 4-mil traces with 4-mil minimum trace spacing. 100-Ω differential impedance was achieved on layers 4, 6, 11, and 13 with 4-mil traces that have 6-mil differential spacing and on the top and bottom layers with 8-mil traces that have 10-mil differential spacing. BGA escape and general SRIO routing vias have 8-mil holes with 18-mil pads. Micro and/or blind/buried vias are neither required nor prohibited.

The PCB BGA pad requirements for the TCI6486/C6472 device are documented by the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811), available at www.ti.com. The TCI6486/C6472 device is a 0.8-mm ball pitch part and should follow the 0.8-mm guidelines. The PCB BGA pad requirements for the SRIO link partner device should follow its manufacturer's guidelines.

3.3 SERDES Interface Routing Requirements

The approach for specifying suitable SERDES routing breaks the physical connection down into three component pieces: receiver end, transmitter end, and interconnect. The receiver and transmitter ends are the pieces closest to the packages of the connected devices. The receiver end goes from the BGA pads to the AC coupling capacitors. The transmitter end is simply the BGA escape paths for the differential pairs. The interconnect joins the receiver and transmitter ends.

3.3.1 Receiver End

For the receiver end, it is strongly desired to route the trace from the BGA pad to the capacitor pad on the top layer. This avoids a via escape between the BGA pad and the capacitor. This style of connection is possible on Serial RapidIO port 1 but not on port 0. On the other side of the capacitor, it is recommended to via to another layer, preferably close to the bottom of the board to minimize the via stub. The trace widths and separation should be altered based on the board stackup to meet the 100-Ω differential impedance requirement. Traces may be necked down to escape the BGA, if necessary.

3.3.2 Transmitter End

The transmitter end should use standard via escapes to internal layers, preferably close to the bottom of the board to minimize the via stub. Internal layers are recommended for their superior shielding characteristics. The trace widths and separation should be selected based on the board stackup to meet the 100-Ω differential impedance requirement. Traces may be necked down to escape the BGA, if necessary.

3.3.3 Interconnect

The geometry of the traces to link the transmitter and receiver ends is determined by the placement in the target system. Therefore, it is not possible to specify an exact layout for the interconnect. Instead, the trace may be placed as required, so long as it meets the following requirements:

- Edge-coupled, matched-length (±10 mils) differential pair.
- No stubs.
- No more than 30 inches (75 cm) pin-to-pin, for 8-mil (0.2-mm) wide traces over FR4 material.
- 100-Ω differential impedance.
- The areas where desired differential-pair separation cannot be maintained (connections to devices or connectors) should be kept to an absolute minimum.
- Do not route across splits in the neighboring reference plane.
- No more than 3 sets of vias (not including via for BGA breakouts).
- Whenever possible, use the majority of the via length to transfer the signal to the internal routing layer in order to avoid via stubs (in other words, if DSP and its SRIO link partner are both on top of the PCB, internal routing should be close to the bottom).
- Other signals are separated by at least 2x the differential spacing.
- Internal layers are strongly preferred; avoid top and bottom layers.
- Internal routing traces must be adjacent to a reference plane (either ground or power; ground is strongly preferred) and within one signal plane of a ground reference plane.
- Avoid running long traces parallel to the FR4 fiberglass weave, as this may affect the propagation delays of the differential signals. Offset the pair with a 45 degree angle every few inches.
- If connectors are used, they must be of a suitable 100-Ω differential-impedance, high-speed type, and count as 1 in. of trace for each connector pair.

There is no requirement that the lengths of different differential pairs to be matched to each other.

3.3.4 Mid-Bus Probe (Optional)

A mid-bus probe can be used to observe traffic flowing down a link. Because the probe requires a special attachment point, it can degrade signal quality. The following rules must be observed to include a mid bus probe:

- Follow the probe manufacturer's guidelines for probe pads and layout.
- If the stubs can be kept under 250 mils (6.35 mm), then connecting the probe lands as stubs to the transmission line is acceptable.
- If the stubs cannot be kept under 250 mils (6.35 mm), then the probe lands should be connected in-line with the rest of the transmission line.

3.3.5 Connectors (Optional)

Any connectors used must be controlled impedance (50-Ω single-ended or 100-Ω differential) and suitable for microwave transmissions. Suitable connectors are typically categorized as backplane-type connectors. The connectors should have less than 1 dB insertion loss below 6 GHz. Some suggested connectors are:

- CN074 - AMC Connector
- Tyco Z-DOK
- Tyco Z-PAK HM Zd

3.3.6 Cabling (Optional)

Any cabling used must be controlled impedance (50-Ω single-ended or 100-Ω differential) and suitable for microwave transmissions. Recommended cable types are listed below:

- 50-Ω Coaxial - commonly used with SMA connectors, 4 cables required for 1x link; 16 for 4x link
  - RG142
  - RG316
  - RG178
- Infiniband - assembled cables available in 1x and 4x widths

3.4 Power Supply Requirements

The power supply and bypassing requirements for SERDES power planes are documented as part of the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* (SPRAAQ4).

It is best to use a plane segment (copper pour) to connect the power from the filters to the pins. However, traces at least 20 mils wide can also be used to access the inner BGA pads.

4 Device Settings

Some of the SERDES register values should be set based on parameters from the physical PCB. Others are not dependent on the PCB, but are set based on the SRIO electrical specification. The following sections describe the recommended settings for the receivers and transmitters. More information about these registers can be found in the *TMS320C6472/TMS320TCI648x DSP Serial RapidIO User's Guide* (SPRUE13).

4.1 Receive Channel Configuration

Table 3 lists the recommended settings for receiver channels that can be set in the SERDES receive channel configuration registers (SERDES_CFGRXn_CNTL).

Table 3. SERDES Receive Channel Configuration Register Settings

Bit	Field	Setting	Description
22:19	EQ	0001	Fully-adaptive equalization.
18:16	CDR	000	First order. Sufficient for SRIO clocking scheme (asynchronous with low frequency offset).
15:14	LOS	00	Disabled. Loss-of-signal detection not used in SRIO.
13:12	ALIGN	01	Comma Alignment. SRIO uses comma alignment during lane initialization.
10:8	TERM	001	Common point is 80% of V_{DDT}. This is the appropriate setting for AC coupled lines.
7	INVPAIR	0	Non-inverted - use when TXP connects to RXP and TXN connects to RXN.
		1	Inverted - use when TXP connects to RXN and TXN connects to RXP(1).
6:5	RATE	00	Full - use for 3.125-GHz and 2.5-GHz line rates.
		01	Half - use for 1.25-GHz line rate [see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* (SPRAAQ4)].
4:2	BUS-WIDTH	000	10-bit. SRIO uses 10-bit character groups.

(1) On inverted pairs, polarity inversion can be done at the receiver end or the transmitter end, but not both.

Table 3. SERDES Receive Channel Configuration Register Settings (continued)

Bit	Field	Setting	Description
0	ENRX	0	Disabled - for unused lanes.
		1	Enabled - for active lanes.

4.2 Transmit Channel Configuration

Table 4 lists the recommended settings for transmitter channels that can be set in the SERDES transmit channel configuration registers (SERDES_CFGTXn_CNTL).

Table 4. SERDES Transmit Channel Configuration Register Settings

Bit	Field	Setting	Description
16	ENFTP	0	Fixed phase. Do not care in 1x mode.
15:12	DE	1000	-4.16 dB. Use for lines up to 10 inches (25 cm).
		1001	-4.86 dB. Use for lines up to 14 inches (35 cm).
		1010	-5.61 dB. Use for lines up to 18 inches (45 cm).
		1011	-6.44 dB. Use for lines up to 22 inches (55 cm).
		1100	-7.35 dB. Use for lines up to 26 inches (65 cm).
		1101	-8.38 dB. Use for lines up to 30 inches (75 cm).
11:9	SWING	100	750 mV. Use for lines up to 10 inches (25 cm).
		101	1000 mV. Use for lines up to 20 inches (50 cm).
		111	1375 mV. Use for lines up to 30 inches (75 cm).
8	CM	1	Raised common mode. Helpful in preventing signal distortion at SWING amplitudes over 750 mV.
7	INVPAIR	0	Non-inverted - use when TXP connects to RXP and TXN connects to RXN.
		1	Inverted - use when TXP connects to RXN and TXN connects to RXP(1).
6:5	RATE	00	Full - use for 3.125-GHz and 2.5-GHz line rates.
		01	Half - use for 1.25-GHz line rate [see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* (SPRAAQ4)].
4:2	BUS WIDTH	000	10-bit. SRIO uses 10-bit character groups.
0	ENTX	0	Disabled - for unused lanes.
		1	Enabled - for active lanes.

(1) On inverted pairs, polarity inversion can be done at the receiver end or the transmitter end, but not both.

5 References

1. RapidIO specifications may be downloaded from the RapidIO Trade Association's web site, www.rapidio.org.
2. The *TMS320C6472/TMS320TCI648x DSP Serial RapidIO User's Guide* (SPRUE13) explains the functional operation of the SRIO peripheral.
3. The *TMS320C6472/TMS320TCI6486 Hardware Design Guide* (SPRAAQ4) contains information related to powering, clocking, and configuring the TMS320TCI6486/TMS320C6472, including the SRIO peripheral.
4. The *High-Speed DSP Systems Design Guide* (SPRU889) contains general guidance on many matters of high-performance DSP system design.
5. The *Flip-Chip Ball Grid Array Package Reference Guide* (SPRU811) provides guidance with respect to PCB design and Texas Instruments BGA packages. It contains PCB design rules, PCB assembly parameters, rework process, thermal management, troubleshooting tips plus other critical information.
6. *NEX-SRIO Users Manual* and *Probing Design Guide for the NEX-SRIO Serial RapidIO Logic Analyzer Probe* from Nexus Technology, Inc. are documents that describe the mid-bus probe and explain its use when monitoring the protocol operation of an SRIO link. More information can be found at www.nexustechnology.com.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265