Application Note

AM6442, AM6422, AM6412 and AM2434 Schematic Design and Review Checklist

ABSTRACT

This application note summarizes circuit design guidelines and recommendations to be followed by the board designers using any of the AM6442, AM6441, AM6422, AM6421, AM6412, AM6411, AM2434, AM2432, AM2431 processors. The guidelines include possible processor configurations and care about for interfacing different processor peripherals to attached (external) devices.

Additionally, links are provided for processor product page, collaterals, E2E FAQs and other commonly referenced documents that could help the designers optimize the efforts during board design.

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1 Introduction

This application note applies to all the processors listed below. Product related documentation is available on the product pages on TI.com. Click the processor link below for accessing the product page.

1.1 AM64x Processor Family

- AM6442
- AM6441
- AM6422
- AM6421
- AM6412
- AM6411

1.2 AM243x Processor Family

- AM2434
- AM2432
- AM2431

2 Related Collaterals

A number of documents relevant to the selected processor are provided on the product page on TI.com. Read through the documents before starting the design.

The link below summarizes the collaterals that can be referred when starting a custom board design.

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Collaterals to Get started.

2.1 Hardware Design Guide

It is recommended to read through the hardware design guide before starting custom board design.

Refer the *Hardware Design Guide for AM6442, AM6422, AM6412 and AM2434 Processors* to get an overview of the steps to be followed during custom board design.

3 Processor Selection

3.1 Data Sheet

Data sheet includes the pin description, pin to function mapping, recommended operating conditions and timing information for different processor peripherals.

For a quick overview of the processor architecture and selecting the processor variant, features, and speed grade, see the *Functional Block Diagram* and *Device Comparison* section of the device-specific data sheet.

3.2 Peripheral Instance Naming Convention

For naming the peripherals and instances, the device-specific TRM is generic, and the device-specific data sheet tends to be specific.

In the data sheet a suffix number is assigned even when there is only one instance, so any documents that reference the name will not need to change from processor to processor.

3.3 Processor Ordering and Quality

For information related to ordering and quality for the selected processor, see the links below:

AM6442-Ordering & quality

AM6441-Ordering & quality

AM6422-Ordering & quality

AM6421-Ordering & quality

AM6412-Ordering & quality

AM6411-Ordering & quality

AM2434-Ordering & quality

AM2432-Ordering & quality

AM2431-Ordering & quality

4 Power Architecture

To get an overview of the power solutions available, see the TI Power management web page.

In addition, WEBBENCH circuit designer tool provides a visual interface that delivers required power application.

4.1 Generating Supply Rails

The supply rails for the selected processor can be generated using discrete or integrated power architecture.

Use of discrete power architecture provides flexibility in design and component selection. Board designer has to take care of the device selection that can source the required load current, setting the output voltage, supply ramp, load transient response and supply sequencing.

Use of integrated power architecture (PMIC) simplifies processor specific power supply design.

The PMIC generates all the common supplies used to power the processor, allows supply power-up and power-down sequencing, supply ramp control and meeting all the processor specific power requirements.

Along with the PMIC, additional DC/DC converters and LDOs are used to generate additional on-board supplies based on use case.

Recommended devices and related collaterals for generating the on-board supplies using different power architectures are summarized below:

4.1.1 PMIC (Power Management IC)

For an integrated power architecture, recommended PMICs include TPS65219 or TPS65220 or LP8733xx. The space, performance and BOM optimized power architecture is designed to power the processor and the attached devices.

For additional information, refer below application notes:

Powering the AM64xx with the LP8733xx PMIC

Powering the AM64x with the TPS65220 or TPS65219 PMIC

Powering the AM243x With the TPS65219 PMIC

Using LP8733xx and TPS65218xx PMICs to Power AM64x and AM243x Sitara Processors.

4.1.1.1 Additional Reference

For more information, see the *Device Connection and Layout Fundamentals, Power Supply and Power Supply Designs* section of the device-specific data sheet and SK-AM64B (AM64B starter kit for AM64x sitara processors) schematic.

4.1.2 Discrete Power

Alternatively, a discrete power architecture could be used to generate the processor supply rails. Discrete power architecture is based on DC/DC converters and LDOs. The power sequence has to be implemented using the power good output and discrete logic.

For more information on the device selection and power architecture implementation, refer the *TMDS64EVM (AM64x evaluation module for Sitara processors)* schematic and below sections.

4.1.2.1 DC/DC Converter

The DC/DC Converters such as LM5140-Q1, TPS62823, TPS62097 or similar devices can be considered.

4.1.2.2 LDO

The LDOs such as TPS735, TLV70728, TLV75518 or similar devices can be considered.

4.2 Power

4.2.1 Load Switch

Load Switches can be used to turn on and off power to a specific peripheral or sub-system powered by the same supply level rail instead of using multiple DC/DC converters or LDOs to generate the supply. In some applications, there is a strict power-up/power-down sequence that must be followed. Load switches simplifies the implement power sequencing to meet the power-up/power-down requirements.

The load switch can be enabled by the PMIC or DC/DC converter to comply with the processor power sequencing requirements.

Load switches such as TPS22919, TPS22918, TPS22945 or similar devices can be considered.

4.2.2 eFuse

eFuses are integrated power path protection devices that are used to limit circuit currents, voltages to safe levels during fault conditions. eFuses offer many benefits to the system and can include protection features that are often difficult to implement with discrete components. To get an overview of the eFuses available, see the TI eFuses & hot swap controllers web page.

5 General Recommendations

Here are the recommendations and guidelines for board designers to be familiar while designing the custom board.

5.1 Processor Performance Evaluation Module (EVM)

Processor (hardware) performance evaluation modules/platforms (EVM) are not to be considered as a reference design. They are evaluation platforms and may not represent a proper or complete system implementation. In many cases, the EVMs are partially or completely designed and released for fabrication much before the processor design is complete. This is done so that a hardware platform is available when first silicon arrives. It is possible to learn new processor requirements during processor bring-up and bench validation. If so, these new requirements may not be accounted for in the hardware evaluation platform. Therefore, TI expects customers to carefully review and follow all requirements defined in the device-specific data sheet, silicon errata, and TRM when designing their system.

The hardware development platforms were not designed to be comprehensive of any system specific requirements, like radiated emissions, noise susceptibility, thermal management, and so forth.

5.2 EVM Versus Data Sheet

During evaluation or the board design, in case of any discrepancy between the device-specific EVMs and the data sheet, it is recommended to always follow the data sheet. Despite the best efforts by the designer, the EVMs may contain errors that still function but are not completely aligned with the data sheet specification.

5.2.1 Note About Component Selection

Selection of EVM components may not be the most optimized. Review the BOM and optimize the component selection based on the data sheet recommendations, application requirements and board circuit design.

Design calculations, design review and performing tests as required is recommended before finalizing the components value and ratings.

5.2.1.1 Series Resistor

The recommended value for the series resistors are simply a starting point for designers and should be verified on the board and adjusted accordingly (Step function that occurs on this pin is not near the mid-supply).

5.2.1.2 Parallel Termination

Provision for parallel pulls, pull polarity and pull values are based on the specific peripheral connectivity recommendations, recommendations for improved processor performance and relevant interface or standards requirements. EVM or SK implementation can be followed when standards or requirements for the interfaces are not available.

EVM or SK pull values can be used as a starting point and designers can choose the appropriate pull values based on the processor and attached device recommendations or specific board design implementation.

5.2.1.3 External ESD Protection

Providing provision for external ESD protection is recommended if any of the processor IOs are directly connected to an external connector, since internal ESD protection was not designed to handle the system level ESD requirements. To get an overview of the ESD protection ICs available, see the TI ESD & surge protection ICs web page.

5.2.2 Additional Information

Based on the project schedule and the design process followed, it is okay to reuse the EVM design files.

The link below summarizes the considerations designers have to be familiar when reusing TI EVM design files.

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - Reusing TI EVM design files.

5.3 Before You Begin The Design

5.3.1 Documentation

During the board design cycle, always use the latest version of the documentation, examples includes the device-specific data sheet, silicon errata, TRM and other design collaterals.

Tips for documentation search: Try searching the documentation for words such as: "recommended", "require", "do not", "note", "pin connectivity" and so forth. Important criteria for the processor typically contains one or more of these words. This is an easy way to make sure not missed anything important.

Tips to get updated information: On TI.com, processor product folder page, there is a "Notifications" button. Registering here enables automatic notification of processor documentation changes.

5.3.2 Processor Pinout Verification

- Verify the processor pin label correspond to the correct pin numbers listed in the *Pin Attributes* section of the device-specific data sheet.
- Verify the supply voltages connected to the processor power pins are within the recommended operating condition.
- All the pins of the processor (grouped into functions and having separate symbol blocks) are shown in the schematics to minimize tool related and functional errors.
- Most of the processor IOs are turned off by default. External pull resistors are recommended to hold inputs of any attached device in a valid logic state until software initializes the IOs. Use of pull resistor is attached device dependent.
- All Reserved pins of the processor, are recommended to be named as RSVD and left unconnected (do not connect signal traces/test points to these processor pads).
- For any processor pad (pin) that has a trace connected and not being used or not being actively driven, an external pull resistor is recommended.
- For board performance improvement, consider implementing external voltage, current or temperature monitoring.

5.3.3 IOSET

IOSETs are a collation of signals specific to an interface that are timed as a set. The processor is timing closed using IOSETs. Any interface that has IOSETs must select all interface signals from the same IOSET. Some interface signals may be shared over multiple IOSETs.

5.3.4 Note on PADCONFIG Register

Many of the processor pads support multiplexing of function. This means that their function can be independently chosen from multiple options. The selection of functions available on each pad is enumerated in *SIGNAL NAME* column in the *Pin Attributes* table of the device-specific data sheet.

The desired function is selected via the MUXMODE field of the associated pad configuration register. The PADCFG_CTRL0_CFG0_PADCONFIG0 to PADCFG_CTRL0_CFG0_PADCONFIG171 registers control the signal multiplexing of IO modules in the processor Main Domain and MCU_PADCFG_CTRL0_CFG0_PADCONFIG0 to MCU_PADCFG_CTRL0_CFG0_PADCONFIG32 registers control the signal multiplexing of IO modules in the processor MCU Domain.

The *Pad Configuration Ball Names* table in the *Pad Configuration Registers* section of the device-specific TRM summarizes the Bit Field Reset Values for all the PADCONFIG registers. Follow the notes added at the end of the table while configuring the PADCONFIG registers. The RXACTIVE bit must never be set without a valid logic state being sourced to the pin associated with the respective PADCONFIG register. This is important since a floating input may damage the processor.

5.3.5 Signal Isolation for Fail-Safe Operation

When the processor and the attached devices or an additional host are powered by different power sources, signal isolation is recommended since most of the processor IOs are not fail-safe. It is recommended to route the signals through a bus FET switch circuit designed to automatically isolate the two devices anytime the IO power is not valid for both devices. The bus FET switch and control logic are recommended to be powered from an always on power supply and only enabled by an AND function of power good signals from different power sources.

5.3.6 Reference to EVM or SK

For implementation (when specific recommendations are not available in the processor specific data sheet) examples and values, refer to the device-specific EVM or SK as applicable

5.3.7 Board Design - Layers Optimization

The main constraint in determining layer count is the number of layers required to implement the high speed DDR4/LPDDR4 interface. It may be possible to reduce the layer count in comparison to the EVM or the SK. Refer the *AM64x / AM243x DDR Board Design and Layout Guidelines* application note available on TI.com for further guidance and best practices in implementing the DDR4/LPDDR4 interface on custom design.

5.3.8 Termination of Unused Processor Pins

For specific connectivity requirements on certain unused processor pins or interfaces, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

It should be okay to leave any unused pin that does not have a special requirement mentioned in the *Pin Connectivity Requirements* section unconnected.

5.3.9 Naming of Peripheral Instances

A suffix number is assigned to a peripheral even when there is only one instance for reuse so that any documents that reference the name will not need to change from processor to processor.

The suffix starts with “0”. For the CPSW3G port names, port “0” is the internal (CPPI host) port of the switch.

5.3.10 High-Speed Interface Design Guidelines

For detailed recommendations on USB2.0, USB3.0 and PCIe signals connection and routing, refer the *High-Speed Interface Layout Guidelines*. Include appropriate constraints or routing requirements to be followed into the design.

For USB interface, a common-mode choke may be needed for improving the board performance when operating in harsh industrial environment. In addition, consider adding external ESD protection based on the application requirement.

5.3.11 Voltage and Thermal Manager (VTM) Module

The temperature monitors (sensors) are placed near the anticipated hot spots of the processor. You could read the on-die temp sensors in Linux and perform thermal management. Refer E2E thread.

5.3.12 Allowed GPIO Current Source or Sink

The DC current driven by the output buffers should remain less than the minimum IOH and IOL values defined to achieve the VOL max and VOH min values defined in the respective *Electrical Characteristics* table. We do not recommend going above the limits defined in the device-specific data sheet and we prefer the DC current to be significantly less that these limits because it can contribute to other problems.

For example, switching these high levels of current could create a lot of electrical noise that could couple to other circuits and require additional decoupling capacitors on the respective IO power rail.

5.3.13 Connection of Capacitor to LVCMOS Type IO (Input or Output)

LVCMOS type IOs when configured as inputs, have slew rate requirement. Connecting capacitors directly to the inputs is not recommended since the input will be driven to mid supply by the slow ramp causing functional or reliability concerns.

Follow the data sheet recommendations or perform simulations when connecting capacitors at the output of the LVCMOS IOs configured as output.

5.3.14 Processor Related Queries and Clarifications

For queries and clarifications related to processor selection and features, use the TI E2E forum. E2E can be used to ask new questions or refer to related questions that have been previously answered.

6 Processor Specific Recommendations

6.1 Common (Processor Start-Up) Connection

6.1.1 Power Supply

Follow the recommendations listed below:

- The power requirement for each supply rail varies based on the interfaces used and the operating environment.
- The current draw of processor supply rails can be estimated using the *PET (Power Estimation Tool)*. If the outputs from the selected power architecture powers the other on-board attached (peripheral) devices, the maximum current draw of these devices needs to be included.
- Verify if the output current ratings of the selected power architecture including PMIC, DC/DC converters and LDOs meet the maximum demand of processor and all devices that are attached. It is recommended to consider some additional margin for design variances.
- Verify if the recommended power supply sequence (Power-Up/Power-Down) is being followed. Proper power supply sequencing in correlation with resets and clocks is recommended. For the recommended power sequencing requirements, see the *Power Supply Sequencing* section of device-specific data sheet.

6.1.1.1 Supplies for Core and Peripherals

For proper operation, all power pins (balls) must be supplied with the supply voltages specified in the *Recommended Operating Conditions* section of the device-specific data sheet. Power pins that have specific connectivity requirements are specified in the *Pin Connectivity Requirements* section of the device-specific data sheet.

With the AM64x family of processors, core supply VDD_CORE can be operated at 0.75 V or 0.85 V. When VDD_CORE is operating at 0.75 V, VDD_CORE shall be ramped up prior to all 0.85 V supplies. When VDD_CORE is operating at 0.85 V, VDD_CORE and VDDR_CORE are recommended to be powered by the same source to ramp together.

For AM243x family of processors, VDD_CORE is specified to operate only at 0.85 V. VDD_CORE and VDDR_CORE are recommended to be powered by the same source to ramp together.

VDDS_OSC and VDDA_MCU supplies are recommended to be connected always.

Peripheral core supplies VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, VDDA_0P85_USB0 and VDDR_CORE are specified to operate only at 0.85 V.

Peripheral core supplies VDD_MMC0 and VDD_DLL_MMC0 are specified to operate at 0.85 V when MMC0 is used. It is recommended to connect VDD_MMC0 and VDD_DLL_MMC0 to the same power source as VDD_CORE when MMC0 is not used.

For more information, see the *Recommended Operating Conditions* and *Power Supply Sequencing* sections of the device-specific data sheet.

The processor includes multiple analog supply pins that provide power to sensitive analog circuitry like VDDA_MCU, VDDA_PLLx [x=0-2], VDDA_1P8_SERDES0, VDDA_1P8_USB0 and VDDA_ADC0. Filtered (ferrite) power supplies are recommended. For more information, see the [FAQ] AM625 / AM623 Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails. This is a generic FAQ and can be used for AM64x / AM243x processors.

6.1.1.1.1 Power Supply Ramp (Slew Rate) Requirement and Dynamic Voltage Scaling

All power supplies associated with the processor should allow for controlled supply ramp (supply slew rate). For more information, refer *Power Supply Slew Rate Requirement* section of the device-specific data sheet.

Dynamic voltage scaling for any supply rail is not supported.

6.1.1.2 Supply for IO Groups

The processor includes seven Dual-voltage IO domains (VDDSHVx [x = 0..5] and VDDSHV_MCU), where each domain provides power to a fixed set of IOs. Each IO domain can be configured for 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of IOs powered by the respective IO domain. All signals (attached devices) connected to these IO domains must be powered from the same power source that is being used to power the respective processor Dual-voltage IO domains (VDDSHVx supply rail). Most of the IO buffers are not fail-safe. For information on fail-safe IOs, see the device-specific data sheet.

The pins designated as CAP_VDDSx [x=0-5], CAP_VDDS_MCU and CAP_VDDSHV_MMC1 are provided for connecting external capacitors to internal regulators.

A 1-µF (recommended tolerance is ± 20%) capacitor is recommended to be connected between the pins and VSS for CAP_VDDSx [x=0-5] and CAP_VDDS_MCU. The expected output voltage level at these pins are 1.8 V + 10% (1.98 V max). Choose the capacitor voltage rating accordingly and use an optimal capacitor package.

A 3.3-µF (recommended tolerance is ± 20%) capacitor is recommended to be connected between the pin and VSS for CAP_VDDSHV_MMC1.

Verify if the selected capacitor has ESR less than 0.8 Ω. Ensure board trace connection loop inductance is less than 1.5-nH.

Note

A valid supply voltage for the VDDSHVx supplies must be present before any input is applied to the associated peripherals or IOs.

VDDSHVx supplies and the associated CAP_VDDSx capacitors must be connected irrespective of the usage of the peripherals or IOs.

6.1.1.3 Supply for VPP (eFuse ROM Programming)

It is important for the processor VPP (eFuse ROM programming supply) to remain within the *Recommended Operating Condition (ROC)* range during eFuse programming. An LDO powered from a higher voltage supply (2.5 V or 3.3 V) is recommended for the LDO to be able to compensate for the voltage drop through its series pass transistor and maintain the correct operating voltage during high current transients. Local bulk capacitors are likely needed near the processor VPP pin to support the LDO transient response.

Using a FET as a switch or Load switch to source the VPP pin from a fixed 1.8 V supply can be problematic due to the high current transient. The VPP implementation is recommended to be characterized to ensure the processor VPP pin supply never drops below the min ROC value.

For more information, see the [FAQ] AM625/AM623 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application. This is a generic FAQ and can be used for AM64x / AM243x processors.

6.1.1.4 Additional Information

Placement of 0 Ω resistors (shunt) or a jumper in line with the core and other supply rails are recommended for initial PCB prototype builds. This helps during board bring-up and debug to isolate the supply or current measurement. Current measurement is the purpose of these resistors in the EVM.

Verify the effect of adding this provision on the board performance.

6.1.2 Capacitors for Supply Rails

Ensure PDN analysis has been performed, and the required number of decoupling and bulk capacitors are provided for all the power supply rails including the Dual-voltage IO supply rails.

Place the decoupling capacitors as close as possible to the supply pins. Larger bulk capacitors can be placed further away.

Use low ESL capacitors and mount them with shortest possible traces to keep the mounting inductance low. For more information, refer the *Sitara Processor Power Distribution Networks: Implementation and Analysis*.

The bulk and decoupling capacitors values from the EVM can be used as a reference when PDN analysis is not available. For filtered (ferrite) power supplies implementation, follow the device-specific EVM.

Feedthrough (3-terminal) capacitors can be considered (used on the SK-AM64B board) to optimize the number of capacitors used, minimizes the loop inductance and improve processor performance mainly the DDR performance.

6.1.2.1 Additional Information

When processor peripherals including Analog-to-Digital Converter (ADC0), DDR Subsystem (DDRSS0), MMC0, SERDES0 and USB0 are not used, the peripheral supplies have specific connectivity requirements. For more information, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

6.1.3 Processor Clock

6.1.3.1 Clock Inputs

6.1.3.1.1 High Frequency Oscillator (MCU_OSC0_XI/ MCU_OSC0_XO)

A 25 MHz clock source is required to be connected to the high frequency oscillator (MCU_OSC0) for proper operation of the processor.

Select a crystal or 1.8 V LVCMOS square-wave digital clock source. Discrete components used to implement the oscillator circuit are recommended to be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins. For the crystal, follow the *MCU_OSC0 Crystal Circuit Requirements* table of the device-specific data sheet when choosing the load capacitors.

When using 1.8 V LVCMOS square-wave digital clock source terminate the processor XO pin as per the device-specific data sheet recommendation.

For information on clock selection, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Queries regarding Crystal selection.

6.1.3.1.2 External Clock Input to Main Domain (EXT_REFCLK1)

EXT_REFCLK1 clock pin is routed to clock muxes as one of the selectable input clock source to the Timer modules (DMTIMER/WDT), DMTIMER in Security Subsystem (SMS), MCAN and CPTS (Time Stamping Module). If an application needs a specific clock frequency to be fed to these modules then they have an option to use the EXT_REFCLK1 (for example: time synchronization or for clock quality reasons).

6.1.3.1.3 Additional Information

Refer section *9.3 Clock Routing Guidelines* of *AM62Ax Sitara™ Processors Data Sheet*. The routing guidelines will be updated in the next revision of the device-specific data sheet.

6.1.3.2 Clock Output

IO pin named CLKOUT0 can be configured as clock output. The clock output can be used as clock source for the attached devices (Ex: Ethernet PHY).

It is possible to configure PADCONFIG53 and PADCONFIG157 for MUX MODE 5 at the same time, which will source CLKOUT0 to pins U13 and A19 at the same time. Each AM64x pin has its own IO buffer and the signal multiplexing is done on the processor side of the IO buffer. Therefore, should not encounter any signal integrity issues due to sourcing CLKOUT0 to both pins at the same time.

6.1.4 Processor Reset

6.1.4.1 Reset Inputs

MCU_PORz is the MCU Domain cold reset external input to the processor. It is recommended to keep the MCU_PORz pulled low during the supply ramp and oscillator start-up. Follow the recommended MCU_PORz reset timing requirement in the *Power-Up Sequencing* diagram of the device-specific data sheet.

For MCU_PORz (fail-safe), a 3.3 V input can be applied, but the input thresholds are still a function of the 1.8 V IO supply voltage (VDDS_OSC).

Terminate external warm reset inputs MCU_RESETz and RESET_REQz as per the *Pin Connectivity Requirements* section of the device-specific data sheet. Warm reset inputs (LVCMOS type IOs) have input slew rate requirements. Connecting a capacitor directly at the input is not recommended due to the slow input ramp. A schmitt trigger based debouncing logic is recommended. Refer device-specific EVM schematics for implementing the debouncing logic.

6.1.4.2 Reset Status Outputs

PORz_OUT is the Main Domain POR status output, RESETSTATz is the Main Domain warm reset status output and MCU_RESETSTATz is the MCU Domain warm reset status output.

RESETSTATz can be used to reset on-board memories or peripherals with reset functionality (eMMC, OSPI, Boot mode buffers, EPHY) or SD Card power switch. The PORz_OUT can also be used to latch the hardware strap configurations during power-up including Ethernet PHY pin-strap configurations.

Pulldown resistors are recommended for PORz_OUT and RESETSTATz outputs to assert the reset for the attached devices during power-up.

Reset status outputs when not used can be left unconnected. It is recommended to connect a test point for testing or future enhancements.

6.1.4.3 Additional Information

The inputs that are used to configure the processor boot (BOOTMODExx inputs) must be held in a known state to select the appropriate boot mode configuration as defined in the device-specific TRM, until the boot mode configuration is latched during the rising edge of the PORz_OUT.

6.1.5 Configuration of Boot Modes (for Processor)

Boot mode inputs do not have internal pullup or pulldown resistors that are active during processor power-up or reset. It is recommended to connect external pullup or pulldown resistors to set the required boot mode.

When dip switches are used, it is recommended to use a resistor divider ratio of 470 Ω (pullup) and 47 kΩ (pulldown) for improved noise performance.

When dip switches are not used, it is recommended to use a standard resistor (same value for pullup or pulldown) value Ex: 10 kΩ or similar since either a pullup or pulldown resistor is used.

It is recommended to terminate (pullup or pulldown) boot mode pins marked as Reserved or not used.

It is recommended to add provision for pullup and pulldown resistors for all the boot mode pins that have configuration capability for debugging, design flexibility and future enhancement. Populate either pullup or pulldown for each boot mode pins. Direct connection of boot mode pins to ground or power supply is not recommended or allowed since these IOs have alternate configuration and could intentionally or unintentionally be configured as output.

Based on the application requirement, a buffer that is only driven when reset is active (low) can be used to present the boot configuration to the processor.

If the processor IOs are configured as an output during normal operation, a current limiting series resistor (~1 kΩ) is recommended at the output of the buffers. See the device-specific EVM for implementation.

6.1.5.1 Processor Boot Mode Inputs Isolation Buffers Use Case and Optimization

In the EVM, the boot mode pins Bootmode [15:00] are asserted through two buffers (isolation buffers). The buffers ensure that SYSBOOT pulls (boot mode configured using resistors) are controlling the level of the signals when the boot mode signals are being latched (around the PORz_OUT rising edge) by the processor. Since boot mode signals are often used for other functions after processor power-up and are connected to other devices, boot mode configuration resistors need to be isolated from other connected peripherals so that those peripherals do not conflict with the intended boot mode configuration (signal levels).

The buffers are enabled only when PORz_OUT is driven low by the processor. After PORz_OUT goes high, the buffer outputs are Hi-Z so the signals are not pulled up or down by the boot mode resistors.

For optimizing the design and BOM, these buffers can be optimized or removed depending on the use case. The boot mode pull resistor values can be selected so that they do not affect the operation of attach devices.

6.1.5.2 Bootmode Selection

For configuring the bootmode, see the *ROM Code Boot Modes* table in the *Initialization* chapter of the device-specific TRM.

6.1.5.2.1 Notes for USB Boot Mode

USB0 interface supports boot. When the USB0 is configured for DFU boot mode, 3.3 V supply (permanent or switched) is not recommended to be connected to the USB0_VBUS pin. No permanent supply (equivalent to the divider value) is allowed to be connected to the USB0_VBUS.

A 5 V supply from the host (switched) connected through the USB connector is recommended to be connected to the processor through the resistor voltage divider as per the device-specific data sheet recommendations. The Zener diode could be removed and a 20 kΩ resistor could be substituted for the 16.5 kΩ and 3.5 kΩ resistors if the board will never apply a VBUS potential greater than 5.5 V and the supply is on-board.

Note

USB0_VBUS is fail-safe input. The fail-safe input is valid only if the VBUS supply is connected through recommended VBUS supply divider circuit.

6.1.5.3 Additional Information

When the boot mode configuration to the buffer is being driven from external inputs, the boot mode configuration inputs are recommended to be stable during the processor cold reset.

When using Ethernet Boot (CPSW3G, Take note of i2331 CPSW: Device lockup when reading CPSW register recommendations) and RGMII interface, select a EPHY with capability to enable RGMII_ID mode on the EPHY RX data path and disables RGMII_ID mode on the TX data path by default (the processor implements RGMII_ID on the TX channel). The processor ROM is EPHY agnostic and will not programmatically enable/disable RGMII_ID mode on attached EPHYs. This is accomplished via pin strapping on the EPHY.

6.2 Board Debug Using JTAG and EMU

JTAG not used

For terminating the JTAG and EMU signals, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

During board design, TI recommends provisioning at least a minimal JTAG port connected to test points or a header footprint to support early prototype debugging. JTAG components can be DNI in the production version of the board, if desired. Also provide provision to add recommended terminations as per *Pin Connectivity Requirements* section and external ESD protection.

JTAG and EMU used

Terminate TDI, TCK, TMS, TRSTn, EMU0 and EMU1 signals as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

It is recommended to connect to a series resistor (22 Ω) on the TDO (close to processor pin) signal. External ESD protection is recommended for all JTAG and EMU signals when the signals are connected to external connector.

6.2.1 Additional Information

Buffering of clock and signals are recommended whenever the JTAG interface connects to more than one device. buffering of clock is strongly recommended even for single device implementations. For implementation, see the device-specific EVM.

If trace operation is required, connect TRC_x signals directly to the emulation connector. All TRC_x signals are pin-muxed with other signals. Either trace functionality or GPMC interface can be used. Connections (Board Routes) for TRC_x signals used for trace functionality must be short and skew matched. The trace signals are on VDDSHV3 domain, and can be at a different supply voltage from the other JTAG signals. For additional recommendations on TRC/EMU design and layout, see the *Emulation and Trace Headers Technical Reference Manual*. A summary of this information is available at *XDS Target Connection Guide*.

If boundary scan is required, connect EMU0 and EMU1 pins directly to the JTAG connector.

For proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*.

7 Processor Peripherals

7.1 Power Supply Connections for IO Groups

Each Dual-voltage IO domain (VDDSHVx [x=0-5] and VDDSHV_MCU) provides power supply to a fixed set of IOs (peripherals). 3.3 V or 1.8 V supply voltage can be connected to each of the Dual-voltage IO domains. For all the Dual-voltage IO domains except VDDSHV5, it is recommended to connect the required supply voltage during power-up.

VDDSHV5 has been designed to support power-up, power-down, or dynamic supply voltage change without any dependency on other supplies. This capability is required to support UHS-I SD Cards.

7.2 Memory Interface (DDR4, LPDDR4, MMCSD (eMMC/SD/SDIO), OSPI/QSPI and GPMC)

7.2.1 DDR Subsystem (DDRSS)

The processor supports DDR4 or LPDDR4 interface.

7.2.1.1 Double Data Rate 4 (DDR4)

For implementation guidelines and routing topology, refer the *AM64x / AM243x DDR Board Design and Layout Guidelines*.

7.2.1.1.1 Interface Configuration

The allowed device configurations are 1 X 16-bit or 2 X 8-bit.

1 X 8-bit device configuration is not a valid configuration.

7.2.1.1.2 Routing Topology and Terminations

When a single device is used (1 X 16-bit), consider following Point-to-Point routing topology.

Summary of point-to-point topology implementation:

- For differential clock (DDR0_CK0, DDR0_CK0_n) signals, differential termination (2 X R in series (value = Zo) and a filter capacitor connected to the center of two resistors and VDDS_DDR (DDR PHY IO supply)) is recommended.

- VREFCA (VDDS_DDR/2, reference voltage) is used for command and address inputs of the attached device.

  VREFCA can be generated using a resistor divider (2 resistors (recommended value is 1 kΩ, 1%) connected in series to VDDS_DDR and VSS) with filter capacitor (recommended value is 0.1uF) connected across both the resistors and additional decoupling capacitor connected to the VREFCA pin close to the device.

Alternatively, adding VTT terminations for a single device on the address and control signals, and using an LDO to generate the VTT supply is an acceptable approach. Ensure the LDO used support the VTT termination application.

When two devices (2 X 8-bit) are used, it is recommended to follow the Fly-by routing topology.

Summary of Fly-by routing topology implementation:

- External terminations (VTT) for address, control and clock signals are recommended.
- An LDO with capability to Sink/Source the current is recommended to generate the VTT supply.
- The LDO generates the reference voltage (VDDS_DDR/2). Add decoupling capacitors for the reference voltage.

7.2.1.1.3 Resistors for Control and Calibration

Provide pulldown resistors for DDR0_RESET0_n (DDR_RESET#), DDR0_CKE0 (DDR_CKE (optional)) and pullup resistor for DDR0_ALERT_n (DDR_ALERTn) close to device pins.

Provide pulldown resistor for DDR4 device TEN (test enable) close to device pin.

Provide resistors for DDR0_CAL0 (close to processor pin) and ZQn (n=0..1, close to device pin/s). Refer device-specific data sheet and DDR design guide for recommended resistor value and tolerance.

7.2.1.1.4 Capacitors for the Power Supply Rails

Provide adequate bulk and decoupling capacitors for the DDR supply rails on the processor side as well as the DDR4 device side. For more information, see the device-specific EVM.

7.2.1.1.5 Data Bit or Byte Swapping

During the design in case bit swapping is required, bit swaps within a data byte, and swapping of byte 0/1 are supported. Address bit swapping is not supported. The DM and DQS bits must not be swapped.

For more information, see the *Bit Swapping* section of *AM64x / AM243x DDR Board Design and Layout Guidelines*.

It is recommended to update the schematics to include the bit swapping done during layout.

7.2.1.2 Low-Power Double Data Rate 4 (LPDDR4)

For implementation guidelines and routing topology, refer the *AM64x / AM243x DDR Board Design and Layout Guidelines*.

7.2.1.2.1 Interface Configuration

The allowed device configuration is 1 X 16-bit. For more information, see the *LPDDR4 Device Implementations Supported* section of *AM64x / AM243x DDR Board Design and Layout Guidelines*.

Refer *Board Design Simulations* chapter of the *AM62A3 / AM62A7 DDR Board Design and Layout Guidelines* and *AM625 / AM623 DDR Board Design and Layout Guidelines* application notes.

7.2.1.2.2 Routing Topology and Terminations

Follow point-to-point routing topology for clock (CK), address, control (ADDR_CTRL) and data signals.

There is no termination required on the board of the address/control signals for LPDDR4. All termination is handled internally (on-die). Thus, VTT does not apply for LPDDR4.

7.2.1.2.3 Resistors for Control and Calibration

Provide pulldown resistor for DDR0_RESET0_n (LPDDR4_RESET_N) close to device pin.

Provide resistors for DDR0_CAL0 (close to processor pin), ODT_CA_A..B (close to device pin/s) and ZQn (n=0..1, close to device pin/s). For recommended resistor value and tolerance, see the device-specific data sheet and DDR design guide.

7.2.1.2.4 Capacitors for the Power Supply Rails

Provide adequate bulk and decoupling capacitors for the DDR supply rails on the processor side as well as the LPDDR4 device side. For more information, see the device-specific SK.

7.2.1.2.5 Data Bit or Byte Swapping

During the design in case bit swapping is required, bit swaps within a data byte, and swapping of byte 0/1 are supported. Address bit swapping is not supported.

It is recommended to update the schematics to include the bit swapping done during layout.

7.2.2 Multi-Media Card/Secure Digital (MMCSD)

The processor supports two MMCSD instances. The MMCSD Host Controller provides an interface to 1 X eMMC (8-bit) and 1 X SD/SDIO (4-bit) instances.

7.2.2.1 MMC0 - eMMC (Embedded Multi-Media Card) Interface

For more information, see the *MMC0 - eMMC Interface* section of the device-specific data sheet.

7.2.2.1.1 MMC0 Used

7.2.2.1.1.1 IO Power Supply

The MMC0 interface of the processor is powered by the VDD_MMC0 (0.85 V), VDD_DLL_MMC0 (0.85 V) and VDDS_MMC0 (1.8 V) supplies.

It is recommended to connect the same supply rail to VDDS_MMC0 and IO supply rail of the attached device (eMMC).

VDD (core voltage) for the eMMC device can be powered from an independent supply rail.

7.2.2.1.1.2 eMMC Reset

It is recommended to implement the eMMC device reset using a dual input AND gate logic. One of the AND gate input is the processor general purpose input/output (GPIO) pin and has provision for pullup. The other input of the AND gate can be processor Main Domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO levels of the attached device matches the processor IO voltage level. A level translator is recommended to match the IO voltage levels.

7.2.2.1.1.3 Signals Termination

Provide the following:

- Provision for a series resistor (0 Ω) for MMC1_CLK (close to processor pin).
- Provide resistor (pulldown) for MMC0_CALPAD (close to processor pin). Refer device-specific data sheet for resistor value and tolerance.

Note

External pull resistors are optional (pullups enabled internally by the eMMC device for DAT0:7, CMD and pulldown enabled internally for CLK, DS).

7.2.2.1.1.4 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors have been provided for the processor supply rails and the attached device (Core and IO supplies).

Follow the device-specific EVM implementation whenever recommendations are not available.

7.2.2.1.2 MMC0 Not Used

MMC0 interface signals do not have alternate function. MMC0 when not used has specific termination requirements for interface and supplies.

For terminating the interface signals, core, analog and IO supplies, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

7.2.2.1.3 Additional Information

Note

There could be implementation difference in the eMMC Controller and PHY IPs used on different processors families. Pay attention on the interface including the terminations recommended when migrating to a different processor family.

It is recommended to review the device-specific data sheet, TRM, and following the termination recommendations of the device-specific processor family and attached device.

EVM implementation can be followed as required.

7.2.2.2 MMC1 – Secure Digital (SD) Card Interface

For more information, see the *MMC1 - SD/SDIO Interface* section of the device-specific data sheet.

7.2.2.2.1 IO Power Supply

The MMC1 IO interface (CMD, CLK and Data) of the processor is powered by VDDSHV5 (Dual-voltage IO) supply rail (IO supply for IO group 5).

VDDSHV5 supports power-up, power-down, or dynamic supply voltage change without any dependency on other supplies.

The processor includes an integrated SDIO_LDO to power VDDSHV5 supply when configured for SD Card interface. The output of the power switch described in the reset section below is connects as input to the SDIO_LDO (VDDA_3P3_SDIO). The output of SDIO_LDO is 3.3 V during power-up and allows changing to 1.8 V when software is ready to change the supply voltage. The output of the SDIO_LDO is controlled by the V1P8_SIGNAL_ENA bit and defaults to 3.3 V output.

Ensure the recommended capacitor is provided at the output of SDIO_LDO pin (CAP_VDDSHV_MMC1).

The SD Card Detect (CD) and Write Protect (WP) pins are connected to the VDDSHV0 (Dual-voltage IO) supply rail (IO supply for IO group 0).

It is recommended to connect the same supply rail to VDDSHV0 and inputs MMC1_SDCD, MMC1_SDWP from SD Card.

Note

If SDIO_LDO is not used to power VDDSHV5, see the *Pin Connectivity Requirements* section of the device-specific data sheet to terminate VDDA_3P3_SDIO and CAP_VDDSHV_MMC1 pins.

7.2.2.2.2 SD Card Reset and Boot

It is recommended to provision for a software enabled (controlled) power switch that sources the SD Card power supply (VDD). A fixed 3.3 V IO supply (IO supply connected to the processor) is connected as the input to the power switch.

The power switch allows power cycling of the SD Card (since this is the only way to reset the SD Card) and place the SD Card back into its default state.

It is recommended to implement the SD Card power switch enable logic using a three input AND gate logic. The input to the AND gate includes PORz_OUT (Main Domain POR status output), RESETSTATz (Main Domain warm reset status output) and processor GPIO. It is recommended to terminate the AND gate input connected to the processor GPIO using a pullup resistor connected to the specific GPIO IO domain supply voltage. Optionally provide provision to isolate the GPIO input to the AND gate for testing or debug.

For implementation details, see the device-specific EVM and SK.

If MMC1 (SD Card) is configured as a boot device ensure that the external power switch sourcing the SD Card power supply defaults to ON (powered state) to ensure the SD Card is powered during boot.

7.2.2.2.3 Signals Termination

Provide the following:

- Provision for a series resistor (0 Ω) for MMC1_CLK (close to processor pin) and external pulldown resistor for MMC1_CLK signal (close to device or SD Card).
- Provide external pullup resistors for the data lines (DAT0:3) and CMD signal connected to the VDDSHV5 (Dual-voltage IO) supply rail close to the SD Card socket.
- Provide external pullup resistors for the CD and WP signals connected to the VDDSHV0 (Dual-voltage IO) supply rail close to the SD Card socket.

7.2.2.2.4 ESD Protection

External ESD protection is recommended for data, clock, and control signals (Internal ESD protection was not designed to handle the system level ESD requirements).

7.2.2.2.5 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV5 (Dual-voltage IO) supply rail and the attached device.

Follow the device-specific EVM and SK implementation whenever recommendations are not available.

Note

Follow the device-specific recommendations for data and control interface termination. It is recommended to place the series resistor for the clock output close to processor pin.

7.2.2.3 Additional Information

For MMC1_CLK PADCONFIG implementation details, see the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the device-specific data sheet.

7.2.3 Octal Serial Peripheral Interface (OSPI) or Quad Serial Peripheral Interface (QSPI)

For more information, see the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the device-specific data sheet.

7.2.3.1 IO Power Supply

The OSPI / QSPI IO interface of the processor is powered by the VDDSHV4 (Dual-voltage IO) supply rail (IO supply for IO group 4).

It is recommended to connect the same supply rail to VDDSHV4 and IO supply rail of the attached device.

VDD (core voltage) for the attached device can be powered from an independent supply rail.

7.2.3.2 OSPI / QSPI Reset

It is recommended to implement the OSPI / QSPI device reset using a dual input AND gate logic. One of the AND gate input is the processor general purpose input/output (GPIO) pin and has provision for pullup. The other input of the AND gate can be processor Main Domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO levels of the attached device matches the processor IO voltage level. A level translator is recommended to match the IO voltage levels.

7.2.3.3 Signals Termination

Provide the following:

- Provision for a series resistor (22 Ω) for OSPI0_CLK (close to processor pin) and external parallel resistor for OSPI0_CLK (pulldown), CS pin (pullup) and INT# pin (pullup) close to the device.

- Provide provision for external pullup resistors for the data lines (DAT0:7) connected to the peripheral specific Dual-voltage IO supply rail close to the processor. Depending on the terminations available internal to the attach device, populate the terminations.

7.2.3.4 Loopback Clock

Verify the required loopback clock configuration. Different configuration of clock loopback can be made using OSPI0_LBCLKO (OSPI Loopback Clock Output) and OSPI0_DQS (OSPI Data Strobe or Loopback Clock Input). For the following loopback configurations, see the device-specific data sheet:

- *No Loopback, Internal PHY Loopback, and Internal Pad Loopback*

External Board Level Loopback

Processor DQS or Loopback Clock is used along with the DS data strobe of OSPI device

If DS (Read Data Strobe) pin is available on the device, connect the DS pin of the device to the OSPI0_DQS pin of the processor. It is recommended to leave the OSPI0_LBCLKO pin floating.

If DS is available or not used, to configure the external loopback, connect the OSPI0_LBCLKO output pin of the processor to the OSPI0_DQS input pin of the processor.

If External Loopback is not used, it is recommended to leave the OSPI0_LBCLKO and OSPI0_DQS pins floating.

Note

D0 and D1 of the processor OSPI interface pins must be connected to D0 and D1 of the QSPI / OSPI memory device pins to support legacy x1 commands. Data bit swapping is not allowed.

7.2.3.5 Interface to Multiple Devices

It is recommended to connect the OSPI (processor) to a single memory device. In case the OSPI is interfaced to multiple memory devices, the interface would create a split data bus which could severely degrade signal integrity at high speeds. For accessing OSPI at high speeds, a point-to-point data bus is recommended.

7.2.3.6 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV4 (Dual-voltage IO) supply rail and the attached device (Core and IO supplies).

Follow the device-specific EVM and SK implementation whenever recommendations are not available.

7.2.4 General-Purpose Memory Controller (GPMC)

7.2.4.1 IO Power Supply

The GPMC IO interface of the processor is powered by the VDDSHV3 (Dual-voltage IO) supply rail (IO supply for IO group 3).

It is recommended to connect the same supply rail to VDDSHV3 and IO supply rail of the attached device.

VDD (core voltage) for the attached device can be powered from an independent supply rail.

7.2.4.2 GPMC Interface

Verify the number of devices connected to the GPMC interface.

It is recommended to connect the processor GPMC interface to a single device in synchronous mode. Using multiple devices (i.e., using multiple CSn) would require splitting the GPMC clock (and other interface signals) on board, which would cause signal integrity issues.

A detailed timing analysis is recommended when interfacing multiple devices (not recommended) in asynchronous mode. When interfacing multiple devices in asynchronous mode, the control signals would have to be routed to multiple devices. The split routing and loading issues will have an affect on performance.

7.2.4.3 Memory Reset

When using NAND / NOR flash with GPMC, many of the memories interfaced over GPMC may not have the reset signal.

It is optional to use the reset signal. In case reset pin is available, review the reset requirements and connect the reset pin to the relevant reset source.

7.2.4.4 Signals Termination

The active high ready / active low busy (R/B#) output from the NAND flash is open drain and is connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). It is recommended to provide pullup resistor (recommended value is 4.7 kΩ) connected to the peripheral specific Dual-voltage IO supply rail. Place the pullup resistor close to the device pin.

It is recommended to provision for external pullup resistors on GPMC0_CSn0..3 (depending on the configuration) to hold the signal high when processor is held in reset, or after reset, before software has configured the PADCONFIG registers to enable the Tx buffer.

Provide series resistor (22 Ω) (close to processor pin) for GPMC0_CLK.

7.2.4.5 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV3 (Dual-voltage IO) supply rail and the attached device (Core and IO voltage).

Follow the device-specific EVM and SK implementation whenever recommendations are not available.

7.3 External Communication Interface (Ethernet (CPSW3G and PRU_ICSSG), USB2.0, USB3.0 (SERDES), PCIe (SERDES), UART and CAN)

7.3.1 Ethernet Interface (CPSW3G and PRU_ICSSG)

The processor supports a total of six Ethernet interfaces.

The processor supports up to five concurrent external Ethernet interfaces (EPHY ports). Pinmuxing overlaps one of the CPSW3G and PRU_ICSSG1 (PRG1_PRU1).

CPSW3G can be interfaced to the external EPHY using RGMII or RMII. One or two RGMII interfaces can be used. When One of the two external CPSW3G interfaces are used to interface to the EPHY using RMII interfaced the EPHY can be configured as controller (master) or device (slave). When both the CPSW3G external interfaces are used to interface to the EPHY using RMII interface it is recommended to configure the EPHY as device.

For more information, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - Ethernet.

7.3.1.1 IO Power Supply

Table 7-1 shows that the IO of the processor supporting media independent interfaces are powered by the Dual-voltage IO rails.

Table 7-1. IO Power Supply Rail Mapping for Interface Instances

Peripheral Instance	Media Independent Interface Type	Interface Instance	Dual-Voltage IO Supply
CPSW3G	RGMII	RGMII1	VDDSHV1 and VDDSHV2
		RGMII2	VDDSHV2
	RMII	RMII1 with IOSET1	VDDSHV2
		RMII1 with IOSET2	VDDSHV1
		RMII2	VDDSHV1
PRU_ICSSG0	RGMII	RGMII1	VDDSHV1
		RGMII2	VDDSHV1
	MII	MII1	VDDSHV1
		MII2	VDDSHV1
PRU_ICSSG1	RGMII	RGMII1	VDDSHV2
		RGMII2	VDDSHV2
	MII	MII1	VDDSHV2
		MII2	VDDSHV2

It is recommended to connect the same supply rail to VDDSHV1 and VDDHSV2 (Dual-voltage IO) supplies and IO supply rail of the attached device.

VDD (core voltage) for the attached device can be powered from an independent supply rail.

7.3.1.2 Media Independent Interface (MAC side)

7.3.1.2.1 Common Platform Ethernet Switch 3-Port Gigabit (CPSW3G)

For pin mapping information related to RGMII interface, refer *Signal Descriptions, CPSW3G, MAIN Domain, RGMII1 Signal Descriptions and RGMII2 Signal Descriptions* sections of the device-specific data sheet.

For pin mapping information related to RMII interface, refer *Signal Descriptions, CPSW3G, MAIN Domain, RMII1 and RMII2 Signal Descriptions* section of the device-specific data sheet.

Note

CPSW3G MDIO0, CPSW3G RMII1, CPSW3G RMII2, and CPSW3G RGMII1 have one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for these interfaces can be found in the tables of the *CPSW3G IOSETs* section of device-specific data sheet.

Based on the interface required, for information on valid IOSETs, valid pin combinations of each CPSW3G MDIO0 IOSET, CPSW3G RMII1 and RMII2 IOSET, and CPSW3G RGMII1 IOSET, refer *Timing and Switching Characteristics, Peripherals, CPSW3G IOSETs* section of the device-specific data sheet.

RMII_REF_CLK is common to both RMII1 and RMII2. For proper operation, all pin multiplexed signal assignments must use the same IOSET. Both RMII ports share a single RMII_REF_CLK. This clock can be the input to PRG1_PRU0_GPO10 pin for IOSET1 or the input to PRG1_PRU0_GPO10 pin for IOSET2. All RMII signals must be configured to pins associated with IOSET1 or IOSET2. It is not allowed to split the clock assignment between IOSETs (connecting clock to one of the IOSET and interface signals to the other IOSET). The clock path for each IOSET is timing closed relative to the signals associated with its respective IOSET. The delay difference between the two clock paths are not relative.

7.3.1.2.2 Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)

For pin mapping information related to RGMII interface, refer *Signal Descriptions, PRU_ICSSG, MAIN Domain* section of the device-specific data sheet.

For pin mapping information related to MII interface (alternate function), use SysConfig-PinMux tool or device-specific TRM.

Pin mapping information for the processor pins provided in the device-specific data sheet for the available primary functions. In case configurable alternate functions are available for any of these pins, the relevant information can be derived using the SysConfig-PinMux tool or by referring to the device-specific TRM.

7.3.1.2.3 Additional Information

PRU_ICSSG pins can be multiplexed at the processor level using the PADCONFIGx registers and also at the PRU_ICSSG IP level. Take care of the schematic connections for the required interface, in particular review the differences between the RGMII connections and the MII connections for the transmit pins including the clock.

Some industrial protocols require the use of 10/100-Mbit EPHY using the MII interface. Verify with the EPHY manufacturer (as required) to determine if the MII interface required by the industrial protocol is supported.

Note

The PRU_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the *PRU_ICSSG* chapter in the device-specific TRM.

7.3.1.3 Usage of SysConfig-PinMux Tool

To configure the required Ethernet interfaces, it is recommended to use the SysConfig-PinMux tool . SysConfig-PinMux tool will provide details of possible IO configurations and IO conflicts.

7.3.1.4 EPHY Reset

It is recommended to implement the EPHY reset using three input AND gate logic. One of the AND gate input is controlled by processor general purpose input/output (GPIO) pin. It is recommended to connect a pullup to the AND gate input (connected to the processor GPIO) connected to the specific GPIO IO domain supply voltage. The other inputs to the AND gate can be the Main Domain POR status output (PORz_OUT) and Main Domain warm reset status output (RESETSTATz) Signal. An isolation resistor is recommended before connecting the processor GPIO input for testing.

If a dual input AND gate is used, PORz_OUT or RESETSTATz can be connected as one of the inputs along with the processor GPIO input as the second input based on the use case. When more than one EPHY is used, it is recommended to provide provision to reset the EPHYs individually.

A pullup or pull down at the output of the ANDing logic is recommended based on the EPHY reset pin configuration. The board designer needs to make sure the EPHYs are held in reset for a specified minimum reset hold time after the respective clocks are valid.

7.3.1.5 Ethernet PHY Pin Strapping

Many of the TI EPHYs configure their outputs as inputs during reset, and captures configuration (Pin strapping is done through resistors) information on these inputs when the processor is released from reset. It may be necessary to apply appropriate pullup or pulldown resistors on these inputs (IOs) which also connect to processor IOs. TI EPHYs used on the EVM or SK use a combination of pullup and pulldown resistors allowing multiple configuration modes to be configured using each pin. By default, the processor input buffers and internal pullup or pulldown resistors are disabled, which minimizes any concern of a mid-supply potential being applied to the processor input buffer by the EPHY. The EPHYs are required to be configured to normal state from reset state to ensure the EPHY is driving a valid logic state before enabling any of the associated processor input buffers.

7.3.1.6 Ethernet PHY (and MAC) Operation and Media Independent Interface (MII) Clock

Verify the clock input option used for Ethernet PHY and MAC based on the interface.

7.3.1.6.1 Crystal

If a crystal is used as the clock source for the Ethernet PHY, it is recommended to match crystal (clock) specifications with the processor crystal (clock) specifications to ensure optimized performance.

7.3.1.6.2 Oscillator

When an external clock (LVCMOS) oscillator is used as the clock source for the EPHY, a single oscillator is recommended for the processor and the EPHY. It is recommended to use two-output phase aligned buffer for processor and the EPHY. Be sure to terminate XO of the processor as per the device-specific data sheet recommendations. Refer EVM and SK.

Additionally, verify if the crystal XO of the EPHY has termination recommendations.

7.3.1.6.3 Processor Clock Output (CLKOUT0)

Alternative approach for clocking the Ethernet PHY is to use the processor clock output (CLKOUT0). Clock output is buffered internally and is intended for a point-point clock topology. A series resistor is recommended at the source.

RGMII EPHYs require a 25 MHz clock input that is not synchronous to any other signals. So, this signal will not have any timing requirements, but it is important the EPHY does not receive any non-monotonic transitions on its clock input.

RMII EPHY clocking option changes with the controller (master) and device (slave) configuration.

When configured as controller, most RMII EPHYs require a 25 MHz input clock that is not synchronous to any other signals, the 25 MHz clock signal will not have any timing requirements, but it is important to make sure the EPHY does not receive any non-monotonic transitions on its clock input.

The RMII EPHY provides the 50 MHz clock the MAC. For this use case, the 50 MHz data transfer clock is delayed to the MAC relative to the EPHY. This shifts clock to data timing relationship which may erode the timing margin. This could be problematic for some designs if this delay is too large.

When configured as device, the MAC and the EPHY uses a 50 MHz clock that is synchronous to both transmit and receive data. The 50 MHz clock is defined in the RMII specification as a common data transfer clock signal that is used by both the MAC and the EPHY, where transitions are expected to arrive simultaneously at the MAC and EPHY device pins. This provides better timing margin for both transmit and receive data transfers. It is also important that the MAC and EPHY do not receive any non-monotonic transitions on their clock inputs. To ensure this doesn't happen, it is highly recommended this clock signal is routed through a two-output phase aligned buffer. Recommend using equal length signal traces that are ½ the length of the data signals for connecting the clock buffer outputs, where one clock output connects to the MAC and the other connects to the EPHY.

For RMII interface, the recommended configuration is the *RMII Interface Typical Application (External Clock Source)* explained in the device-specific TRM. If *RMII Interface Typical Application (Internal Clock Source)* configuration explained in the device-specific TRM is used the performance has to be validated on a system level. Provision for an external clock for initial performance testing and comparison is recommended. The Ethernet performance (RGMII) has been validated on the processor and the EPHY with 25 MHz clock.

The CLKOUT0 signal function can be used to source a 25 MHz or a 50 MHz clock to the EPHY. However, this would require the software to configure the clock output. This configuration cannot be used if the board design needs to support Ethernet boot. This clock is likely to glitch anytime the configuration is changed.

The board designer needs to make sure the EPHYs are held in reset for a specified minimum reset hold time after the respective clocks are valid.

TI does not define performance of the processor clock outputs because clock performance is influenced by many variables unique to each system implementation. The board designer will have to validate timing of all peripherals by using their actual PCB delays, min/max output delay characteristics, and min setup/hold requirements of each device to confirm there is enough timing margin.

7.3.1.7 MAC (Data, Control and Clock) Interface Signals Termination

Series resistors (22 Ω) are recommended for the Ethernet MAC interface signals. Use smallest possible package (0402 or smaller) and place as close to the source. To start with place series resistor (22 Ω) for the TX signals near to the processor pins. For the RX signals the EPHYs internal series resistors can be used. Providing provision for external series resistors (0 Ω) are recommended on the RX signals.

The interrupt output of the Ethernet PHY can be connected to the processor EXTINTn (interrupt) pin. A pullup resistor is recommended for the EXTINTn input close to the processor. When a PCB trace is connected and not being driven actively by an external input, it is recommended to connect the external pullup resistor. This is a fail-safe input.

7.3.1.8 MAC (Media Access Controller) to MAC Interface

For applications requiring EPHY-less (MAC-to-MAC) connection, using the RGMII interface is recommended (check with TI if this is officially supported) since the clocks are source synchronous.

7.3.1.9 Management Data Input/Output (MDIO) Interface

If CPSW3G, PRU_ICSSG0 and PRU_ICSSG1 are used in the design, see the MDIO interface configuration.

Table 7-2. CPSW3G MDIO

IOSET	Signal Name	Ball Name	Dual-Voltage IO Supply
IOSET1	MDIO0_MDIO	PRG0_PRU1_GPO18	VDDSHV1
	MDIO0_MDC	PRG0_PRU1_GPO19	VDDSHV1
IOSET2	MDIO0_MDIO	PRG1_MDIO0_MDIO	VDDSHV2
	MDIO0_MDC	PRG1_MDIO0_MDC	VDDSHV2

Table 7-3. PRU_ICSSG INSTANCE MDIO

Peripheral Instance	Ball Name/Signal Name	Dual-Voltage IO Supply
PRU_ICSSG0	PRG0_MDIO0_MDIO	VDDSHV1
	PRG0_MDIO0_MDC	VDDSHV1
PRU_ICSSG1	PRG1_MDIO0_MDIO	VDDSHV2
	PRG1_MDIO0_MDC	VDDSHV2

Using the same MDIO to control both CPSW3G and PRU_ICSSG Ethernet is NOT recommended or currently not supported in hardware.

It is recommended to provide external pullup resistor for the MDIO signals (MDIO0_MDIO, PRG0_MDIO0_MDIO, PRG1_MDIO0_MDIO). Place the pullup resistor close to the device pin.

Before configuring the MDIO interface, see the advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)* of the device-specific silicon errata.

7.3.1.9.1 MDIO Interface Mode

Before using the MDIO interface, see the advisory i2329 MDIO: MDIO interface corruption (CPSW and PRU_ICSS) of the device-specific silicon errata.

If the selected processor and the silicon revision being used is affected by the silicon errata, there is a work around implemented by the driver. The driver reads the device JTAG ID and configures the MDIO to use manual (bit bang) mode.

Refer section *Peripherals, High-speed Serial Interfaces, Gigabit Ethernet Switch (CPSW3G), CPSW0 Functional Description, MDIO Interrupts* for information related to MDIO modes and *Introduction, Device Identification* for JTAG ID of the device-specific TRM

7.3.1.10 Ethernet Medium Dependent Interface (MDI) Including Magnetics

In case the EPHY and MDI interface including the magnetics and the RJ45 connector are implemented on the processor board, follow the EVM and SK for MDI interface, magnetics recommendation, external ESD protection and connection of RJ45 connector shield.

7.3.1.11 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV1 and VDDSHV2 (Dual-voltage IO) supply rails and the attached device (core and IO supplies).

Follow the device-specific EVM and SK implementation whenever recommendations are not available.

7.3.2 Universal Serial Bus (USB2.0)

The processor provides 1 X USB2.0 interface that can be configured as host or device or DRD (Dual-Role Device).

USB0_VBUS is recommended to be connected in accordance with the *USB Design Guidelines* section of the device-specific data sheet. The supply voltage range for the USB0_VBUS pin is defined in the *Recommended Operating Conditions* table of the device-specific data sheet.

7.3.2.1 USB Used

It is recommended to connect the USB analog supplies VDDA_0P85_USB0, VDDA_1P8_USB0 and VDDA_3P3_USB0 to the recommended power supply rails in the device-specific data sheet.

Connect USB0_DM and USB0_DP signals directly (without any series resistors or capacitors). Route these signals with traces that does not include any stubs or test points.

Provide resistor (pulldown) for USB0_RCALIB (close to processor pin). Refer device-specific data sheet for resistor value and tolerance.

7.3.2.1.1 USB Host Interface

It is recommended to provide a power switch to control the VBUS supply to externally connected device and protect power switch input supply from being overloaded.

The Power switch output connects to the USB type A connector. It is recommended to connect a capacitor (>120-µF) to the VBUS supply close to the connector.

The USB0_DRVVBUS signal with an internal pulldown is used to enable the VBUS power switch. An external pulldown near to the power switch enable (EN) pin is recommended. Connection of USB0_VBUS (VBUS supply input including Voltage Divider / Clamp) is optional.

If the power switch used has an OC (over current) indication output, pullup the OC indication output and connect to a processor IO (input).

It is recommended to connect USB0_ID pin to VSS through a 0 Ω resistor.

7.3.2.1.2 USB Device Interface

The VBUS power is sourced by an external host. USB standard for device operation recommends connecting < 10 µF capacitor to the VBUS close to the USB type B connector.

Follow the *USB VBUS Design Guidelines* section of the device-specific data sheet to scale the USB VBUS voltage (supply near the USB interface connector) before connecting to USB0_VBUS pin.

Based on the use case, the zener diode can be removed if one is absolutely sure that the board will never experience a VBUS signal potential greater than 5.5 V (sourced on-board).

It is recommended to leave the USB0_ID pin floating.

7.3.2.1.3 USB Dual-Role Device Interface

Connect USB0_ID pin directly to the corresponding ID pin on a USB Micro-AB connector. Depending on the cable attached, the USB0_ID pin will be terminated and the processor will be configured as host or device.

Note

Full compliant USB On-The-Go (OTG) feature is not supported.

7.3.2.1.4 USB Type-C

If the board design uses USB Type-C connector, the USB0_ID signal is not required to be connected. The DRD mode switching is controlled by the USB Type-C companion device.

DRP (Dual role port) requires a controller, primarily to switch power based on the negotiated role. In a Device Mode only, USB2.0 only, Type-C implementations where the device is not powered by the Type-C connector, no Type-C controller is required.

- The CC pins at the connector should be independently grounded via 5.1K (recommended tolerance is ±20%) resistors.
- The USB DP and USB DM connector pins should be shorted on the PCB (DM=B7:A7, DP=B6:A6). This allows for USB2.0 connectivity regardless of cable orientation. Try to keep resulting stubs as short as possible.

Also ensure you follow the USB0_VBUS input scaling recommendations. See the section *USB VBUS Design Guidelines* of the device-specific data sheet for details.

The AM62 SK USB0 interface design can be used as a reference for implementation of USB Type-C interface.

7.3.2.2 USB Not Used

USB0 when not used has specific terminating requirements for interface and supplies.

For terminating the interface signals, analog supply pins, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

It is recommended to connect the processor USB analog supplies to VSS through separate 0 Ω resistors.

In case USB0 is required for future expansion, connect the signals (USB0_DM, USB0_DP, USB0_RCALIB and USB0_VBUS) with the shortest possible traces and terminate at test points or connectors. Additionally, provision to connect the USB supplies has to be provided.

7.3.2.3 Additional Information

Connect USB0_DM and USB0_DP signals directly from the processor to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed. Ground the connector ID to enable host mode. As each hub has different implementation requirements, it is recommended to follow the hub manufacturer recommendations.

For more information on USB2.0 interface, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – USB2.0 interface.

7.3.3 Serializer/Deserializer (SERDES)

USB3.0 or PCIe interface (data transaction) are implemented through the SERDES pins. The USB3.0 subsystem or PCIe subsystem does not have any direct external interface pins.

Note

The use of USB3.0 and PCIe interface are mutually exclusive (USB3.0 or PCIe). USB3.0 and PCIe cannot be used at the same time.

For more information, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - SERDES - SERDES0 interface.

7.3.3.1 SERDES0 Used

It is recommended to connect the analog and IO supplies VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C and VDDA_1P8_SERDES0 to the recommended power supply rails in the device-specific data sheet.

Provide resistor (pulldown) for SERDES0_REXT (close to processor pin). Refer device-specific data sheet for resistor value and tolerance.

7.3.3.1.1 USB3SS0 - USB3.0 Super Speed Interface Configuration

USB3.0 interface includes SuperSpeed (SS) USB 3.0 Dual-Role Device (DRD) subsystem with on-chip SS (USB3.0) PHY and HS/FS/LS (USB2.0) PHY.

SERDES0 PHY Differential Transmit Data (TX0) and Differential Receive Data (RX0) signals are configured for USB3.0 functionality. SERDES0_TX0_P and SERDES0_TX0_N are configured as USB0_SSTXP and USB0_SSTXN. SERDES0_RX0_P and SERDES0_RX0_N are configured as USB0_SSRXP and USB0_SSRXN.

7.3.3.1.1.1 Signal Interface

7.3.3.1.1.1.1 USB3.0 Super Speed Interface

AC-coupling capacitors are recommended for USB3.0 transmit and receive signals. Place the capacitors closer to the transmitter.

If an on-board USB3.0 connector is used, connect the receive signals from the processor directly to the connector. The AC-coupling capacitors for the receive signals are expected to be available on the device connected to the USB3.0 connector.

7.3.3.1.1.1.1.1 USB3.0 Super Speed Interface Operating Mode Configuration

The processor USB0_ID pin is not USB2.0 specific. The same pin is used to determine the operating mode for USB3.0. The USB0_ID pin is connected directly to VSS through a 0 Ω resistor if operating as a host (Type-A connector used) and open-circuit when operating as a device (Type-B connector used). It is recommended to route the USB0_ID signal from the processor to the Micro USB Type-AB connector, for Dual-Role configuration.

7.3.3.1.1.2 Unused SERDES Clock Termination

For terminating the unused SERDES0_REFCLK0P and SERDES0_REFCLK0N pins, see the *Pin Connectivity Requirements* table recommendations of the device-specific data sheet. Optionally, place 50 Ω resistor at the clock output terminals (P and N) with respect to ground near to the processor and provision for a test point for internal board level testing.

7.3.3.1.1.3 Additional Information

USB3.0 interface includes signals related to USB3.0 and USB2.0 signals for backward compatibility. Refer above section Universal Serial Bus (USB2.0) for information related to USB2.0 signals and connection.

Connect the USB3.0 signals (differential transmit and receive) and USB2.0 signals (USB0_DP and USB0_DM) to the USB3.0 (same) connector. Splitting USB3.0 and USB2.0 signals to different connectors is not allowed (permitted) in the USB3.0 specification.

7.3.3.1.2 Peripheral Component Interconnect Express (PCIe) Interface Configuration

SERDES0 PHY Differential Transmit Data (TX0) and Differential Receive Data (RX0) signals are configured for PCIe functionality. SERDES0_TX0_P and SERDES0_TX0_N signals are configured as PCIE0_TX0_P and PCIE0_TX0_N. SERDES0_RX0_P and SERDES0_RX0_N signals are configured as PCIE0_RX0_P and PCIE0_RX0_N.

7.3.3.1.2.1 Clock Configuration for PCIe Operating Modes

PCIe interface implements a common clock architecture. The clock could be sourced by the processor or the add-on card based on the configured functionality. A common external clock can be used as alternate clocking option.

7.3.3.1.2.2 Signal Interface Termination

AC-coupling capacitors are recommended for PCIe transmit and receive signals. Place the capacitors closer to the transmitter.

If an on-board PCIe connector is used, connect the receive signals from the processor directly to the connector. The AC-coupling capacitors for the receive signals are expected to be available on the device connected to the PCIe connector.

7.3.3.1.2.3 PCIe Clock (REFCLK) Source

The following clocking options can be considered for sourcing the PCIe interface (common clocking architecture) clock

- **Clock generator**

  The clock generator outputs can be connected to the processor and the add-on card (on-board PCIe connector) as a common clock. Follow the clock generator recommendations for terminating the clock outputs.
- **Clock output from the processor**

  The processor clock output can be connected as the clock input to the add-on card. Place 50 Ω resistor at the clock output terminals (P and N) with respect to ground closer to the processor.

  Note

  For allowed configuration, refer advisory i2236 in the device-specific silicon errata.

- **External clock input to the processor (Clock output from an add-on card)**

  The external clock from the add-on card is connected as the clock input to the processor. If the clock from the add-on card is in no Re-biasing mode place a 0 Ω series resistors and if the clock from the add-on card is in Re-biasing mode place a 0.1uF capacitor (AC-coupling) 0402 package. Place the capacitors closer to the receiver.

7.3.3.1.2.4 Hardware Reset (Fundamental Reset)

The following options are available to reset the PCIe card.

- **Resetting the add-on card**

  It is recommended to implement the reset for the attached PCIe device (add-on card) using an AND gate logic. One of the AND gate input is the processor general purpose input/output (GPIO) pin and has provision for pulldown. The other input of the AND gate is the processor Main Domain warm reset status output (RESETSTATz) signal.
- **Resetting the processor**

  It is recommended to connect the reset output from the add-on card (PCIe connector) as one of the inputs to the ANDing logic used to generate the processor MCU Domain cold reset (MCU_PORz).

For implementation, refer the device-specific EVM.

7.3.3.1.2.5 PCIe Clock Request (PCIE0_CLKREQn) Signal

Connection of the PCIE0_CLKREQn (Clock Power Down signal) pin between the processor and the PCIe (add-on card) connector is optional and application dependent. This connection is required to enable low power mode.

The PCIE0_CLKREQn functionality has not been currently implemented on the device-specific EVM. Adding PCIE0_CLKREQn support needs further analysis and addition of glue logic.

7.3.3.1.2.6 Connecting PCIe Interface Signals

Refer device-specific EVM for connecting and configuring the other applicable PCIe signals for implementing different operating modes of PCIe interface.

7.3.3.2 SERDES0 Not Used

SERDES0 when not used has specific termination requirements for interface signals and supplies.

For terminating the interface signals, analog and IO supplies, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

When the processor analog and IO supply pins are required to be connected to VSS. It is recommended to connect to VSS through separate 0 Ω resistors.

When the boundary scan function is required, decoupling capacitors are recommended on the supply pins. Bulk capacitors and ferrites are not required.

When boundary scan function is not required, decoupling capacitors, bulk capacitors and ferrites are not required.

7.3.4 Universal Asynchronous Receiver/Transmitter (UART)

Verify the UART interface application requirements (external interface or debug) and configuration (2-wire or 4-wire with flow control). For the number of instances supported, see the device-specific data sheet.

When an external transceiver is used, make sure the external interface signal levels matches the Dual-voltage IO supply voltage level.

Consider provisioning for series resistors on the interface signals (close to the source) for debug or isolation. It is recommended to add pullup resistor on the UART Receive pins (UART0..6_RXD, MCU_UART0..1_RXD).

External ESD protection is recommended in case the interface signals from the processor are directly connected to an external connector.

UART interface is frequently hooked up incorrectly. Make sure signals are connected as follows:

- TX ---> RX
- RX ---> TX

If additional interface signals are used, verify the connections.

7.3.5 Controller Area Network (CAN)

For the number of instances supported, see the device-specific data sheet. The CAN interface to the processor includes external CAN transceiver.

When an external transceiver is used, make sure the external interface signal levels matches the Dual-voltage IO supply voltage level.

Ensure the required terminations at the CAN transceiver are provided and the signal are connected as expected.

Consider provisioning for series resistors on the interface signals (close to the source) for debug or isolation.

7.4 On-Board Synchronous Communication Interface (MCSPI and I2C)

7.4.1 Multichannel Serial Peripheral Interface (MCSPI)

Verify if series resistors (22 Ω) are provided for clock outputs SPI0..4_CLK (MCSPI 0..4) and MCU_SPI0..1_CLK (MCU_MCSPI 0..1) close to processor pins.

Verify if external parallel pulls are provided for Chip Select signals SPI0..4_CS0..3 (MCSPI 0..4) & MCU_SPI0..1_CS0..3 (MCSPI 0..1) close to the device pins. Pulls for data outputs are use case dependent and needs to be verified when selecting the attach device.

7.4.2 Inter-Integrated Circuit (I2C)

Verify if the application requires a fully compliant I2C interface. The I2C0 and MCU_I2C0 are true open-drain output type buffers and fully compliant to the I2C specifications. These can support 3.4-Mbps I2C operations (when the IO buffers (interface) are operating at 1.8 V).

I2C interfaces with open-drain output type buffers have termination requirements. It is recommended to terminate the open-drain output type buffers I2C interfaces irrespective of the IO configuration, see the *Pin Connectivity Requirements* section of the device-specific data sheet. A pullup of 4.7 kΩ or less is recommended.

When these open-drain output type buffers I2C interfaces are pulled to 3.3 V supply, these IOs have slew rate limit. An RC is recommended to limit the slew rate on the I2C signals.

For more information, see the Terminations (Pullups) section of this checklist document.

Verify if the application requires additional I2C interfaces.

I2C1..3 and MCU_I2C1 use LVCMOS to emulate an open-drain buffer and not fully compliant with the I2C specification, in particular falling edges are fast (< 2 ns). Any devices connected to these ports must be able to function properly with the faster fall time. These support 100-kHz and 400-kHz operation. Pullup resistors are recommended for these I2C signals. Location of the pullup is not critical but connection is important. It is recommended to connect the pullups with the shortest possible stub.

For more information, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – I2C interface.

If planning to use TI provided software, be sure to connect I2C0 to the PMIC, as this is the I2C interface used for PMIC control.

Note

I2C0 and MCU_I2C0 open drain output type buffer I2C interface signals are fail-safe IOs.

7.5 Analog to Digital Converter (ADC)

7.5.1 ADC0 Used

It is recommended to connect the ADC0 analog supply VDDA_ADC0 to the recommended power supply rails in the device-specific data sheet.

Follow the notes added at the end of the *Signal Descriptions, ADC, MAIN Domain* table of the device-specific data sheet before using ADC0.

Refer section *Peripherals, Analog-to-Digital Converter (ADC), Change Summary of AM64x / AM243x SR2.0 ADC Errata* of *Hardware Design Guide for AM6442, AM6422, AM6412 and AM2434 Processors* application note.

Note

ADC IOs are not fail-safe. Applying a voltage to any of the ADC inputs without powering the processor is not recommended or allowed. The ADC input applied (based on the input level) could cause residual voltage on the supply rail resulting in board start-up issues. Refer *Absolute Maximum Rating* table of device-specific data sheet. In case supplies that are available before the processor supply ramps are required to be monitored, it is recommended to connected these inputs to the ADC through a switch. The switch can be controlled by processor GPIO or power good signal from any of the supply source including PMIC.

7.5.2 ADC0 Not Used

When entire ADC0 is not used, there are specific termination requirements for the inputs and supply rail. When any of the ADC inputs are not used, there are specific termination requirements for the unused inputs.

For terminating the ADC inputs, analog supply pin, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

It is recommended to connect the ADC inputs and processor analog supply pin to VSS through separate 0 Ω resistors. This is for future expansion or enhancement and is optional.

7.6 GPIO and Hardware Diagnostics

7.6.1 General Purpose Input/Output (GPIO)

7.6.1.1 Termination and External Buffering

Consider adding series resistor (22 Ω) to limit the current. Externally buffer the GPIO outputs when higher (above the data sheet specified value) current sourcing is required.

7.6.1.2 GPIO Multiplexed With MMC Interface

In case the IO with MMC function are required to be used for GPIO function, the MMC entries in the device tree can be removed for the IOs to function as GPIOs. Alternatively, iomux_enable bit can be set to 1.

7.6.1.3 Additional Information

Signals on unused interfaces can typically be left unconnected, unless otherwise stated. Many of the IOs have a *Pad Configuration Register* that provides control over the input capabilities of the IO (RXENABLE field in each conf_<module>_<pin> register). For more details, see the *Control Module* chapter of the device-specific TRM. Software can disable the IO receive buffers (that is, RXENABLE=0) that are not connected in the design as soon as possible during initialization. Software needs to be ensured that it does not accidentally enable the receiver of an IO (by setting the RXENABLE bit) when the associated pin is floating.

Note

For specific guidance on configuring certain unused pins, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

Note

For specific guidance configuring the IOs, see the *Pad Configuration Registers* chapter of the device-specific TRM.

7.6.2 Internal Hardware Diagnostics

7.6.2.1 Monitoring of On-Board Supply Voltages Using Processor

7.6.2.1.1 Voltage Monitor Pins When Used

It is recommended to connect the main voltage powering the board (3.3 V or 5 V or greater) to the VMON_VSYS pin through an external resistor voltage divider (0.45 V ± 3 %) for early supply failure indication. Consider implementing a noise filter (capacitor) across the voltage divider output connected to the processor input as described in the *System Power Supply Monitor Design Guidelines* section of the device-specific data sheet.

Connect VMON_1P8_SOC, VMON_1P8_MCU, VMON_3P3_SOC and VMON_3P3_MCU pins directly to their respective supplies. Refer *Recommended Operating Conditions* section of the device-specific data sheet for the allowed supply voltage range.

Note

VMON_VSYS, VMON_1P8_MCU, VMON_1P8_SOC, VMON_3P3_MCU and VMON_3P3_SOC are fail-safe inputs.

For VMON_VSYS, fail-safe condition is valid when the recommendations in section *System Power Supply Monitor Design Guidelines* of device-specific data sheet are followed.

For the other VMON pins, the fail-safe condition is valid when the supply voltage connected is within the *Recommended Operating Conditions* or *Absolute Maximum Ratings* of device-specific data sheet.

7.6.2.1.2 Voltage Monitor Pins Not Used

TI recommends using VMON_VSYS for early supply failure indication. When not used, connect VMON_VSYS, VMON_3P3_SOC and VMON_3P3_MCU pins to VSS through separate 0 Ω resistors and add test point for future expansion.

It is recommended to connect the VMON_1P8_SOC and VMON_1P8_MCU pins to respective supplies. Grounding these signals would short internal 1.8 V supplies and is not allowed.

7.6.2.2 Internal Temperature Monitoring

The Voltage and Thermal Manager (VTM) module on the processor supports voltage and thermal management of the processor by providing control of on-chip temperature sensors.

The processor supports a single VTM module, VTM0, which is located in the Main Domain. VTM0 has two associated temperature monitors, ITemp_Sensor_Main_0, and ITemp_Sensor_Main_1, each of which are located near hot-spots in the processor die.

TI does not spec or guarantee any accuracy for the VTM module with regard to temperature measurements. A ± 7°C accuracy is provided to give an indication and we have performed internal characterization to confirm the measurements are within specified range.

7.6.2.3 Termination of Error Signal Output (MCU_SAFETY_ERRORn)

It is recommended to always terminate the MCU_SAFETY_ERRORn signal as per the *Pin Connectivity Requirements* section of the device-specific data sheet for testing or using the signal for other board level applications.

7.6.2.4 High Frequency Oscillator (MCU_OSC0) Clock Loss Detection

The processor supports HFOSC0 clock loss detection circuitry to detect HFOSC0_CLK malfunction (stops). Dedicated hardware logic monitors HFOSC0 clock using CLK_12M_RC clock. When HFOSC0_CLK stops toggling for 9 CLK_12M_RC clock periods, a HFOSC0 clock stop loss condition is detected. If CTRLMMR_MCU_PLL_CLKSEL [8] CLKLOSS_SWTCH_EN is set, the reference clock is switched from HFOSC0_CLKOUT to CLK_12M_RC to allow the processor to operate with a slower clock.

During clock-loss condition, the processor reports the error to the external device through MCU_SAFETY_ERRORn pin by driving the pin Low. The recovery mechanism implementation is up to the external system (such as a PMIC to take action).

For example, doing a full system power cycle to see if the system recovers. If the board does not recover then the processor has to indicate the user to take alternative action such as to check system clocks, external crystal or supply rails.

7.7 Verifying Board Level Design Issues

7.7.1 Processor Pin Configuration Using Pinmux Tool

Recommend verifying All peripheral and IO configuration using the TI *SysConfig-PinMux* tool to ensure valid IOSETs have been configured.

For more information, see the PinmuxConfigSummary.csv file provided by the SysConfig-PinMux tool.

7.7.2 Schematics Configurations

Verify if all the circuit options provided for alternate functionality or testing that are not required for the normal functioning of the board or could result is circuit malfunction are marked as DNI.

7.7.3 Terminations

Terminating a signal to the wrong IO supply rail can cause leakage between the IO rails of the processor. Each signal has an associated IO supply rail (Ex: VDDSHVx [x=0-5]). For more information, see the *Pin Attributes* table of the device-specific data sheet.

For example, if you want to pullup SPI0_CS1 signal in any mux mode (UART6_RXD, I2C2_SCL, GPIO1_43 and so forth), pull up the signal supply rail connected to VDDSHV0.

7.7.4 Peripheral (Sub System) Clock Outputs

For any of the processor peripheral that has a clock output, configure the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx / CTRLMMR_PADCONFIGy registers. This bit configuration is required for the clock output to work properly.

7.7.5 General Debug

7.7.5.1 Clock Output for Board Bring-Up, Test or Debug

The below clock outputs are available on the processor for test and debug purposes only.

- OBSCLK0, MCU_OBSCLK0 (recommended): Observation clock outputs

  OBSCLK0, MCU_OBSCLK0 are observation clock outputs for test and debug purposes only. OBSCLK pins can be used to select one of the several different clocks as output. We do not expect this signal to be used as a clock source for any external device. As stated in the data sheet, this signal is provided for test and debug purposes only.

- SYSCLKOUT0 (optional): SYSCLK0 is divided by 4 and then sent out of the processor as a LVCMOS clock signal (SYSCLKOUT0)
- MCU_SYSCLKOUT0 (optional): MCU_SYSCLK0 is divided by 4 and then sent out of the processor as a LVCMOS clock signal (MCU_SYSCLKOUT0)

If the processor pins designated OBSCLK0, MCU_OBSCLK0, SYSCLKOUT0, MCU_SYSCLKOUT0 are not used, provide a test point for test/debug. Consider adding a parallel pull.

In case these pins are used, a test point can be inserted on the trace and provision to isolated these signals from the attached devices can be provided for test/debug.

System clock pins (MCU_SYSCLKOUT0 and SYSCLKOUT0) are hardwired to dedicated clock resources.

7.7.5.2 Additional Information

It is recommended to provide test points for MCU_RESETSTATz, RESETSTATz and PORz_OUT for testing or debug when not used.

For attached devices (DC/DC Converter or LDO or Sensor) that have an alert output, over current indication or PG (power good) output that is not used, provide a pullup and test point for testing or future enhancements.

8 Layout Notes (to be Added on the Schematic)

Recommend adding design notes as required for the processor peripherals (Example: USB, Ethernet, PCIe, eMMC, SD Card, and other peripherals) and attach device including Board Boot mode configurations, placement of terminations, placement of decoupling and bulk capacitors.

Mark all differential signals, critical signals and if required specify the target impedance. See examples below:

- DDR target impedance is 40 Ω (single-ended) and 80 Ω (differential) for the DDR signals.
- The differential impedance for the USB data lines must be within the specified tolerance for a nominal value of 90 Ω.
- The differential impedance for the SuperSpeed, PCI-Express (PCIe) signal lines (TX and RX) must be within the specified tolerance for a nominal value of 95 Ω.
- The differential impedance for the Ethernet MDI signals must be within the specified tolerance for a nominal value of 100 Ω.

9 Board Design Simulation

The baseline drive impedance and ODT settings are derived from the Signal Integrity SI simulations performed on the EVM and SK.

It is recommended to perform simulation for the design as the values could be different based on board design.

To get an overview of the basic system-level board extraction, simulation, and analysis methodologies for high speed LPDDR4 interfaces, refer *LPDDR4 Board Design Simulations* chapter of the *AM62Ax DDR Board Design and Layout Guidelines* application note.

The drive strength is adjustable using the DDR Register Configuration Tool on SysConfig.

For more information, see the [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration. This is a generic FAQ and can be used for AM64x / AM243x processors.

10 Additional References

Additional references includes FAQs and schematic checklist for some of the processor attach devices that can be used during design and review.

For PMIC design review, see the TPS65219 Schematic, Layout Checklist.

Based on customer queries and learning, FAQs are created to support customers during their board design. Refer below list of FAQs created that could be referred during board design along with other collaterals including the Hardware design guide and the Schematics checklist.

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - FAQs related to Processor peripherals to support board design

Refer to the following list of FAQs that are referred to during design that includes software related FAQs.

[FAQ] PROCESSOR-SDK-AM64X: AM64x Frequently Asked Questions List

11 Summary

This schematic checklist is provided as a guide for use during the schematic design. The recommendations provided in this document could help simplify the design, reduce debug time and could possibly minimize future re-spins of the board.

12 References

12.1 AM64x

- Texas Instruments: *AM64x Sitara™ Processors Data Sheet*
- Texas Instruments: *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*
- Texas Instruments: *TMDS64EVM (AM64x evaluation module for Sitara processors)*
- Texas Instruments: *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)*
- Texas Instruments: *TMDS64DC01EVM (AM64x IO-link and high-speed breakout card)*
- Texas Instruments: *Powering the AM64x with the TPS65220 or TPS65219 PMIC*
- Texas Instruments: *Powering the AM64xx with the LP8733xx PMIC*

12.2 AM243x

- Texas Instruments: *AM243x Sitara™ Microcontrollers Data Sheet*
- Texas Instruments: *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)*
- Texas Instruments: *LP-AM243 (AM243x general purpose LaunchPad™ development kit for Arm®-based MCU)*
- Texas Instruments: *TMDS243DC01EVM (AM243x and AM64x evaluation module breakout board for high-speed expansion)*
- Texas Instruments: *Powering the AM243x With the TPS65219 PMIC*

12.3 Common

- Texas Instruments: *AM64x / AM243x Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM64x / AM243x Processor Silicon Errata*
- Texas Instruments: *AM64x / AM243x Power Estimation Tool*
- Texas Instruments: *Hardware Design Guide for AM6442, AM6422, AM6412 and AM2434 Processors*
- Texas Instruments: *AM64x and AM243x BGA Escape Routing*
- Texas Instruments: *AM64x / AM243x DDR Board Design and Layout Guidelines*
- Texas Instruments: *AM62A3 / AM62A7 DDR Board Design and Layout Guidelines*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors Application Report*
- Texas Instruments: *PRU-ICSS Feature Comparison*
- Texas Instruments: *Industrial Communication Protocols Supported on Sitara™ Processors and MCUs*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *Jacinto 7 High-Speed Interface Layout Guidelines*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*

A Terminology

ADC – Analog-to-Digital Converter

BOM – Bill of Materials

CAN – Controller Area Network

CKE – Clock Enable

CPPI – Communications Port Programming Interface

CPSW3G – Common Platform Ethernet Switch 3-port Gigabit

DFU – Device Firmware Upgrade

DNI – Do Not Install

DRD – Dual-Role Device

DRP – Dual Role Port

E2E – Engineer to Engineer

EMC – Electromagnetic Compatibility

EMI – Electromagnetic Interference

eMMC – embedded Multi-Media Card

EMU – Emulation Control

ESD – Electrostatic discharge

ESL – Effective Series Inductance

ESR – Effective Series Resistance

FET – Field-Effect Transistor

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

I2C – Inter-Integrated Circuit

JTAG – Joint Test Action Group

LDO – Low Dropout

LVCMOS – Low voltage complementary metal oxide semiconductor

MAC – Media Access Controller

MCSPI – Multichannel Serial Peripheral Interface

MDI – Medium Dependent Interface

MDIO – Management Data Input/Output

MII – Media Independent Interface

MMC – Multi-Media Card

MMCSD – Multi-Media Card/Secure Digital

ODT – On-die Termination

OSPI – Octal Serial Peripheral Interface

OTP – One-Time-Programmable

PCB – Printed Circuit Board

PCIe – Peripheral Component Interconnect Express

PDN – Power Distribution Network

PET – Power Estimation Tool

PMIC – Power management integrated circuit

POR – Power-on Reset

PRU_ICSSG – Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

ROC – Recommended Operating Condition

SD – Secure Digital

SDIO – Secure Digital Input Output

SPI – Serial Peripheral Interface

TCK – JTAG Test Clock Input

TDI – JTAG Test Data Input

TDO – JTAG Test Data Output

TEN – Test Enable

TMS – JTAG Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – JTAG Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

XDS – eXtended Development System

Revision History

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