Application Note

AM62Px Escape Routing for PCB Design

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1 Introduction

The AM62Px is an extension of the low-power, low-cost Sitara Industrial/Auto grade family of processors. The AM62Px is based on the Cortex-A53 microprocessor, M4F microcontroller with dedicated peripherals, 3D graphics acceleration, dual display interfaces, and extensive peripheral and networking options for a variety of embedded applications. The AM62Px is available in a 17mm x 17mm FBGA package with a mix of 0.65-mm and 0.8 ball pitches. The package BGA design is built leveraging TI Via Channel Array Technology (VCA) technology, which enables package miniaturization while still utilizing low cost PCB routing rules. Via Channel Array (VCA) is built with careful considerations on escape routing to avoid costly High-Density Interconnect (HDI) and expensive Via technologies. This document is intended to provide a reference for escape routing on the AM62Px device. Care must be taken to route signals with special requirements such as DDR and high speed interfaces. Refer to the High-Speed Interface Layout Guidelines and DDR Routing Guidelines for more details. Details on Power Delivery Network are provided in AM62Px PDN Application note and any routing and layout requirements specified in those documents supersede the generic requirements provided here.

2 Via Channel Arrays

Via Channel Array Technology has been successfully used in a variety of TI products that help in minimizing package dimensions by using smaller ball pitch and low cost PCB routing. Via Channel technology is a way of enabling routing channels to escape innermost BGA positions. This allows several advantages. First, the via outside diameter (also known as the annular ring) can be larger than it normally would be if it had to be placed in between the BGAs in a tighter pitch, because all the vias are placed in special areas called *via channels*. This makes PCB manufacturing less expensive because larger vias are possible. Second, the vias are grouped in a radial pattern instead of a series of concentric rings around the middle of the chip, which is the case with normal BGA array PCB routing. The traces are more easily routed out of the inner parts of the chip because they are not restricted to the narrow paths in between many rows of vias. The unique outer row routing and the via channel inner routing are two important parts of this technology on the AM62Px. The AM62Px BGA Via Channel Array is shown in Figure 2-1.

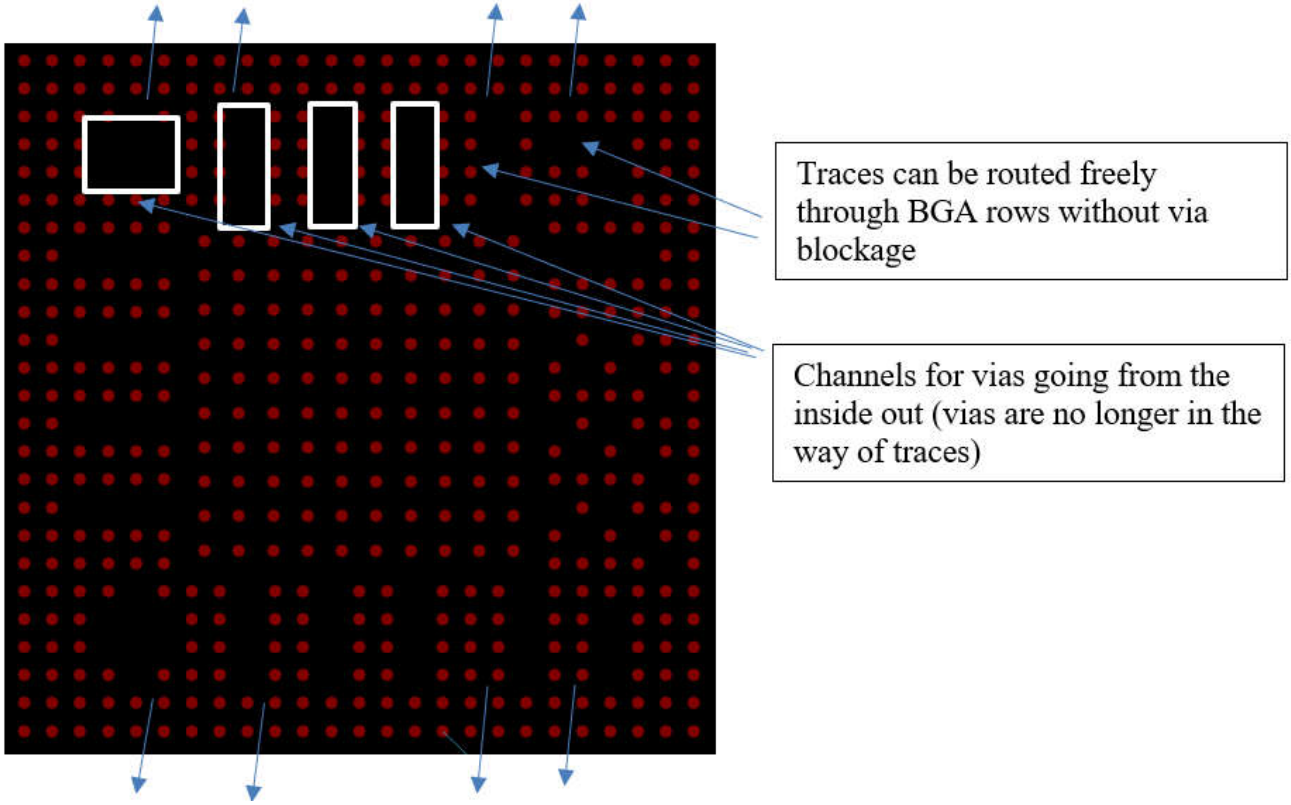

Figure 2-1. AM62Px BGA Array with Via Channels

For the first two rows (from the outside in) of the BGA array, the balls have been arranged to allow wider traces than would otherwise be possible. The first row (the outside row) supports any size trace desired, because the trace comes from the PCB ball land and goes out on the PCB. Normally, the second row traces must be routed in between the first row of the PCB ball lands. The AM62Px allows escapes using a 4mil trace width/space on internal and external layers.

Figure 2-2 shows the first two rows of the AM62Px package and how it is possible to route 4 mil traces and spaces in the areas between balls.

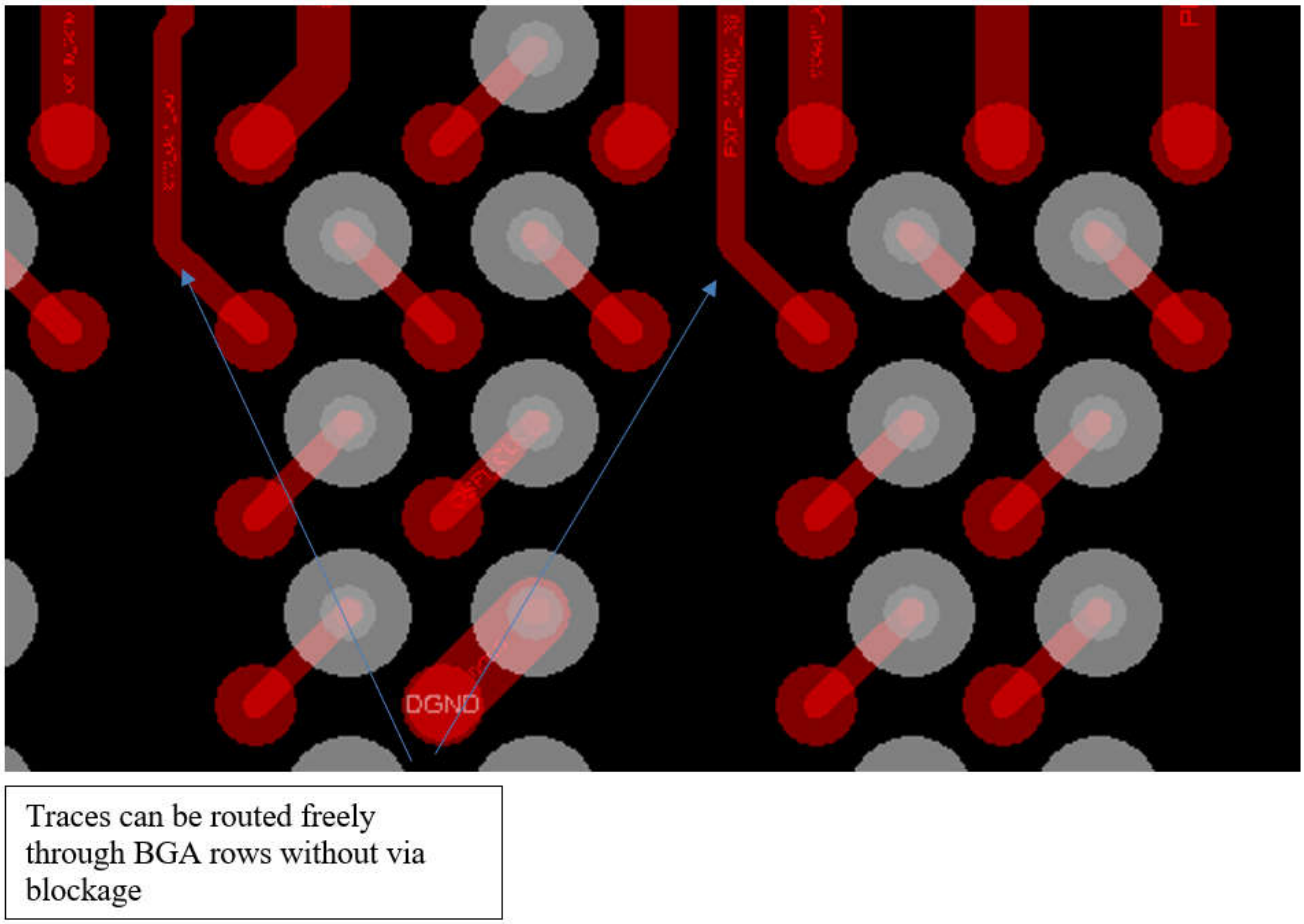

Figure 2-2. Outer Rows of Traces

Starting at the third row, as with any BGA package, vias are necessary. As stated earlier, the vias are gathered in the via channels, so the only vias that must be placed in between balls are some of the power vias in areas of ground or power copper pour. In this case, they have no regular via ring because they are located in an area of copper pour where all the surrounding balls share the same net. This is elaborated more in later sections with details on via sharing. Because the via ring is larger than one that would normally fit in between these balls with the required clearance, the layout tool may flag a design rule check (DRC) error; however, this is a false warning because there is no risk of shorting to a nearby pad as they are all on the same net. The rest of the vias must be placed into the via channels as shown below. Figure 2-3 shows how the vias are grouped in the via channels.

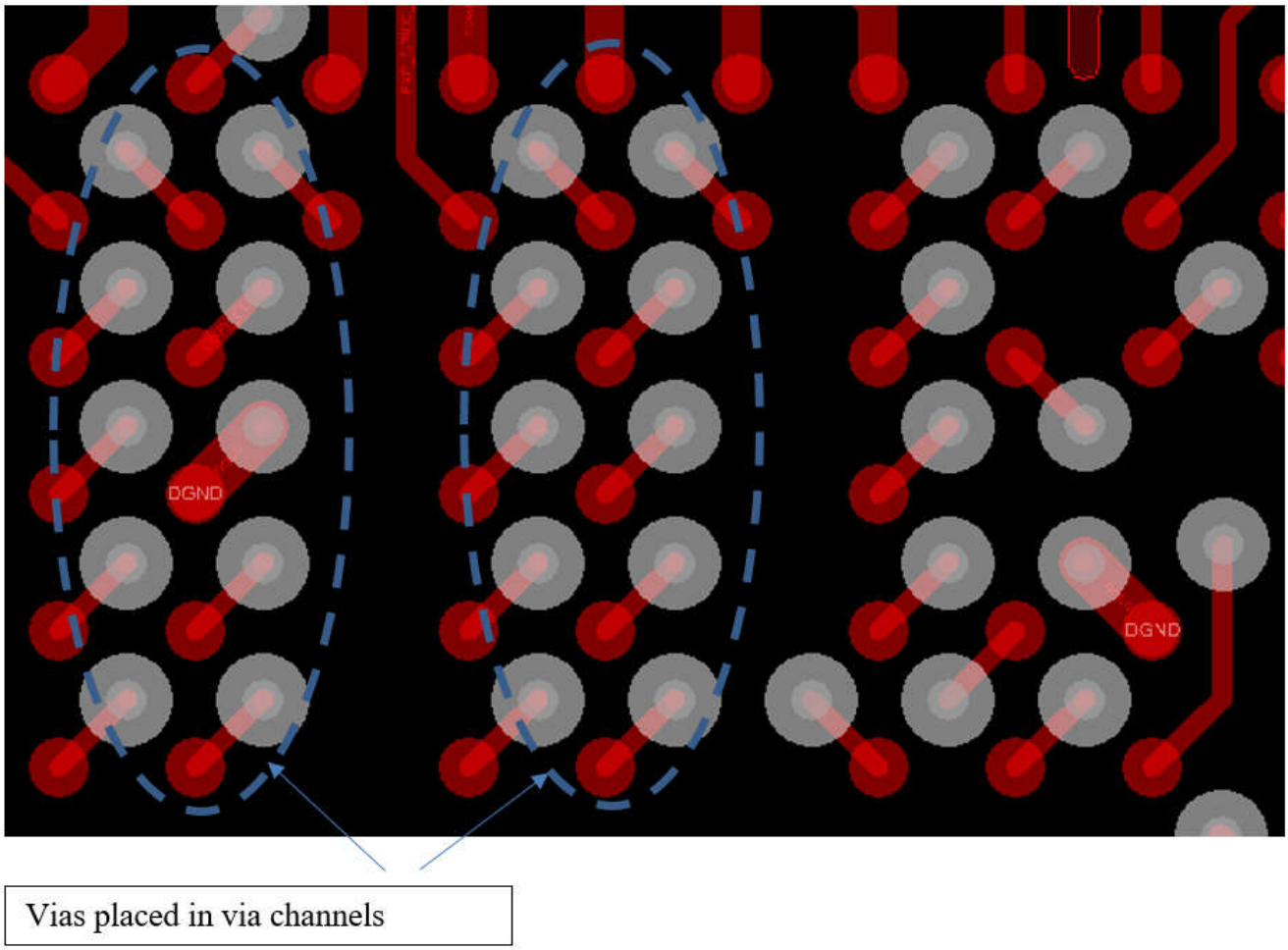

Figure 2-3. Vias in Via Channels

3 Width/Spacing Proposal for Escapes

The AM62Px Via channel array solution has been designed to support the following. The AM62Px package supports a similar feature set as several other competition solutions with approximately 15% smaller package area and ~10% wider line width. This solution reduces the PCB foot print and utilizes lower cost PCB rules, enabling compact and low-cost systems.

Table 3-1. Width/Spacing Proposal for Escapes

PCB Feature	PCB Routing Requirements
Minimum via pad diameter	18 mils
Via hole size	8 mils
Minimum trace width/spacing required in the BGA break out	4mil / 4mil
Number of layers used for escape	5
BGA land pad size	0.3 mm
Package Size	17 mm x 17 mm, 0.65/0.8-mm pitch w/ VCA
PCB layers (signal routing, total) recommended	4, 10
Solder resist clearance	0.07 mm **max**

4 Stackup

PCB stack-up is one of the first and important considerations in realizing a successful PCB. The AM62Px device supports a BGA array or 25x25 with a mixed 0.65/0.8-mm pitch and a body size of 17 mm. PDN compliance and robustness is critical to meet all the performance objectives of the device and associated peripherals. To enable this, TI recommends allocating two layers for power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High speed interfaces such as DDR, CSI, and USB require ground planes for impedance matching. Additionally, to meet the higher DDR interface speeds, ground layers both above and below the DDR signals are strongly recommended. The escapes on the AM62Px board design was achieved with 10 layers, as shown below.

Table 4-1. Example PCB Layer Stack-up

PCB Layer	Layer Routing, Planes or Pours
TOP	Component pads, Ground and signal escapes
Layer 2	Signal Routing
Layer 3	Ground
Layer 4	Signal Routing
Layer 5	Power/Gnd Fill for signals
Layer 6	Power/Gnd Fill for signals
Layer 7	Signal Routing
Layer 8	Ground
Layer 9	Signal Routing
BOTTOM	Ground, Signal and component pad routing

The AM62Px board design example provided is implemented in a 10-layer stack-up as described above. This board is designed for optimum signal integrity on the high-speed interfaces while limiting the board size. The AM62Px board is implemented without HDI (High Density Interconnect) and does not use micro vias, which are both intended to save board cost. All vias on the AM62Px board are Plated Through Hole (PTH) and pass completely through the board. Proper analysis shall be performed to validate both signal and power integrity, if further optimizations are required to reduce PCB stack-up and/or routing rules illustrated in this document.

5 Via Sharing

The Via Channel Array BGA pattern implemented on the AM62Px design offers opportunities for via sharing. Vias are shared across BGA pins and Figure 5-1 shows the via sharing opportunities for the GND net. Via sharing across BGA pins provides for easier escape routing and also robust electrical connection by connecting multiple pins.

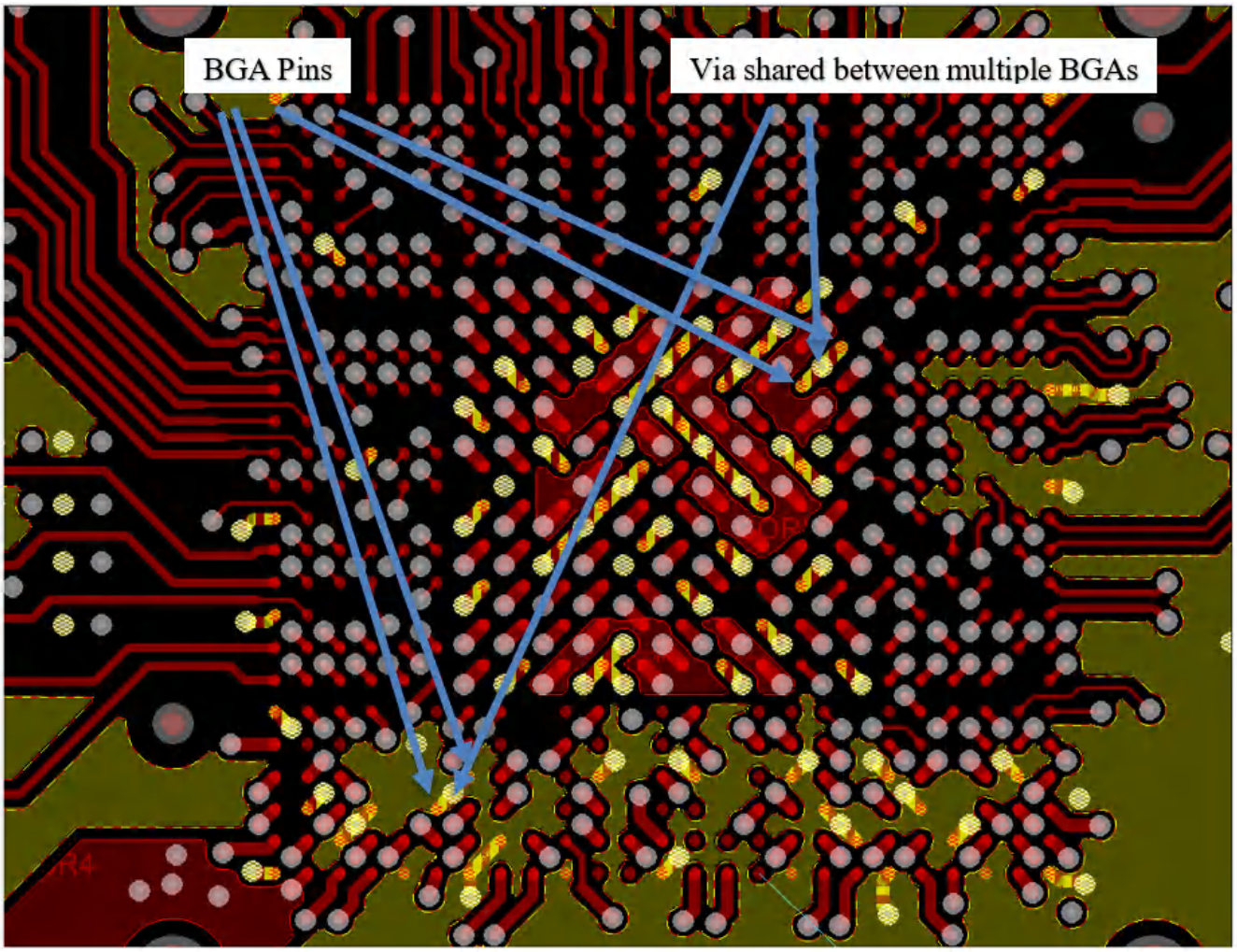

Figure 5-1. Via Sharing for VSS

6 Floorplan Component Placement

Careful analysis is required to analyze the locations of the interfaces used on the device and the associated components and connectors. Optimum trace routing will have routes as short as possible with a minimum cross-over. The AM62Px offers interface selection flexibility through pin-mux choices. Pin-muxing enables a same interface function made available on multiple pins and is selectable through a pin mux option. Favorable pin-mux options that ease PCB routing and component placement can be fully utilized to further optimize the PCB design. The figure below shows the default arrangement of the signal balls and the power and ground balls. Priority shall be given to component placements without pin-mux options such as DDR, CSI, DSI, USB, OLDI/LVDS, and so forth.

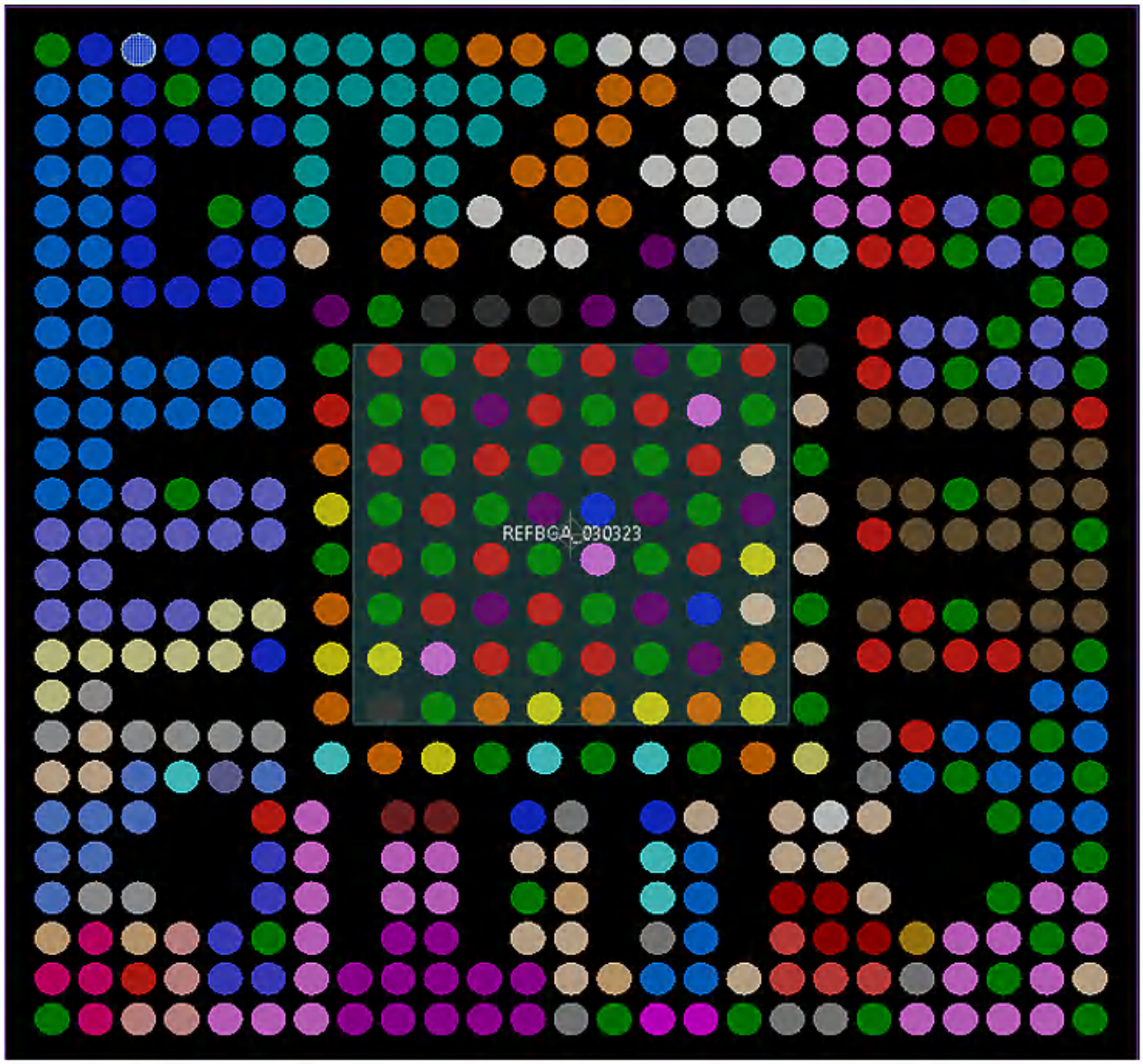

Figure 6-1. AM62Px Floorplan

7 Critical Interfaces Impact Placement

Placement of the AM62Px device and some of the components or connectors is also dictated by some of the highest performance interfaces such as DDR, CSI, and so forth. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

8 Routing Priority

As indicated earlier, critical interfaces affect component placement options. The next step in PCB design is to prioritize routing to these critical interfaces. Those with higher priority must be completed before implementing those of lower priority. It is imperative to route interface with the higher priority first. PCB layout teams often end up in a time intense, iterative process with sub optimal results when routing priorities are not established. The table below lists a recommended priority order for interfaces contained on the AM62Px family of devices. Individual design requirements may drive a need for adjustment of the priorities, but this serves as a good baseline and has been used for the board example illustrated in this document.

Table 8-1. Routing Priority

Interface	Routing Priority
LPDDR4	10 (Highest Priority)
CSI/DSI	9
OLDI	9
OSC	8
USB2, OSPI	8
Power distribution	7
RGMII	6
eMMC	5
Clocks	5
MII / RMII	4
SPI	4
Motor control	4
Analog	3
GPMC	2
GPIO	1
UART / CANUART	1
I2C / Temp Diode	1 (Lowest Priority)

The multi-gigabit DDR (dual data-rate) interface is the most critical due to its data rate and loss concerns. DDR is at the top of the priority list because it is very sensitive to PCB losses. Additionally, being single-ended in nature makes it highly susceptible to signal integrity issues such as crosstalk, especially at the high speeds targeted in this design. Next in the priority list is the CSI (Camera Serial Interface) and DSI (Display Serial interface). The limited length for these routes might affect the PCB placement of the CSI/DSI connector and the AM62Px device. CSI/DSI signals are found on the outer layers of the BGA footprint, allowing some of the traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. The one surprise may be power distribution, which is often left to last. This then results in poor decoupling performance or current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.**

9 SerDes Interfaces

The package BGA ball map is also arranged to support routing the higher priority interfaces first. Therefore, the SerDes CSI and DSI interfaces are located towards the outer two rings. The differential receive pair should be routed away from the SoC on the top layer leaving a gap without blocking vias. The lanes located on inner BGA rows require vias to escape as a differential pair on the bottom or on an interior layer. The VCA facilitates this for inner rows. See Figure 9-1 for an example of the escape of the SerDes signals on the AM62Px board on the top layer and on an inner layer. Wide traces can limit the signal loss but could violate the impedance requirements. For more detailed information on routing SerDes signals, refer to the document on High-Speed Interface Layout Guidelines.

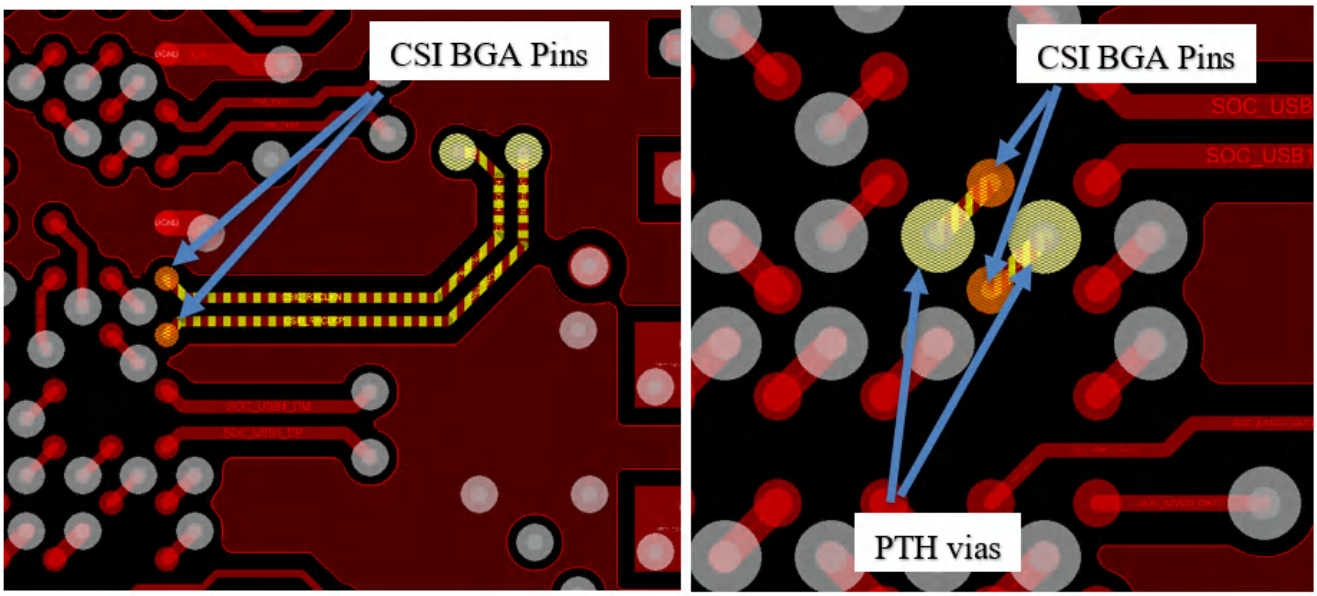

Figure 9-1. Serdes CSI Escapes for TOP layer (Left) and Inner layer (Right)

10 DDR Interfaces

The AM62Px supports connection to a LPDDR4 device. The DDR signals must be routed with highest priority. Refer to the DDR Routing Guidelines document for detailed recommendations for DDR routing. The images below show the BGA breakout for the DDR interface on the AM62Px Board.

The DDR SDRAM memory devices are normally arranged so that the data group balls are closest to the AM62Px device. The Package BGA ball map has been carefully planned to place the DDR address and command signals between data byte lanes 0/1 and data byte lanes 2/3.

Figure 10-1 and Figure 10-2 illustrate how to escape the DDR byte lanes 0 and 1, respectively. The use of Plated Through Hole (PTH) vias make the routing of these signals between the SoC and SDRAM possible on any layer. Likewise, the escape for DDR byte lanes 2 and 3 are shown respectively in Figure 10-3 and Figure 10-4.

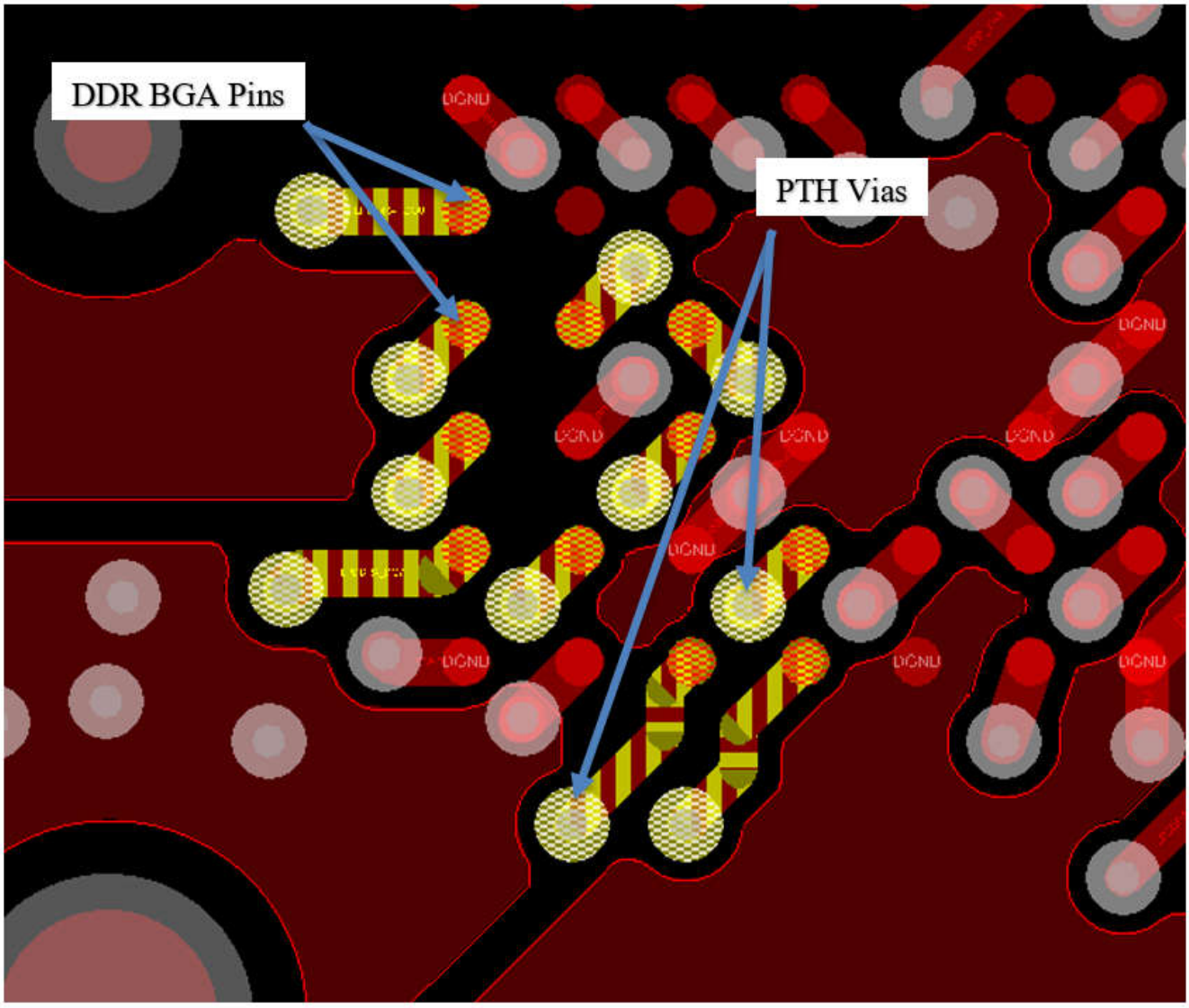

Figure 10-1. DDR Byte Lane0 Escape

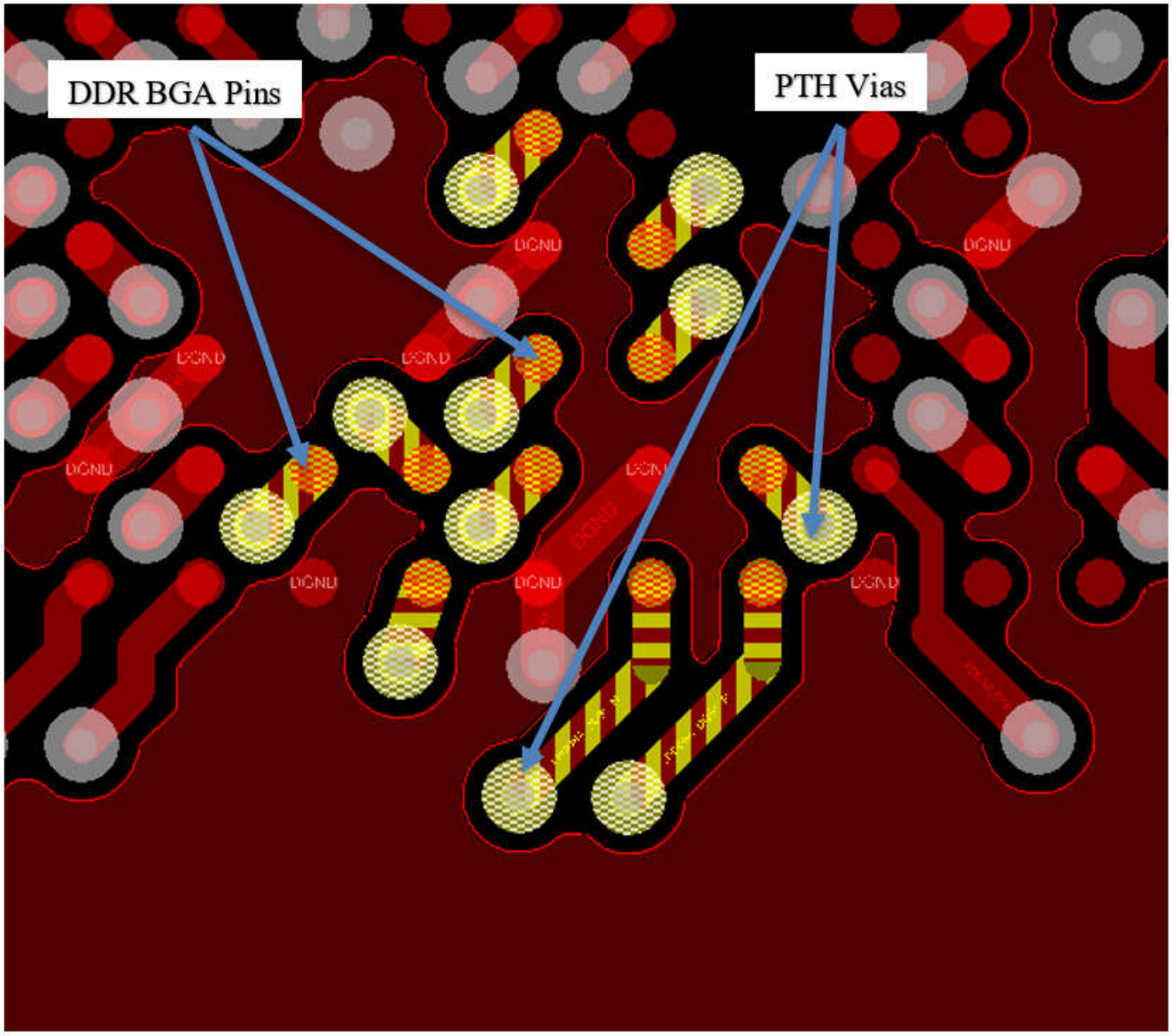

Figure 10-2. DDR Byte Lane1 Escape

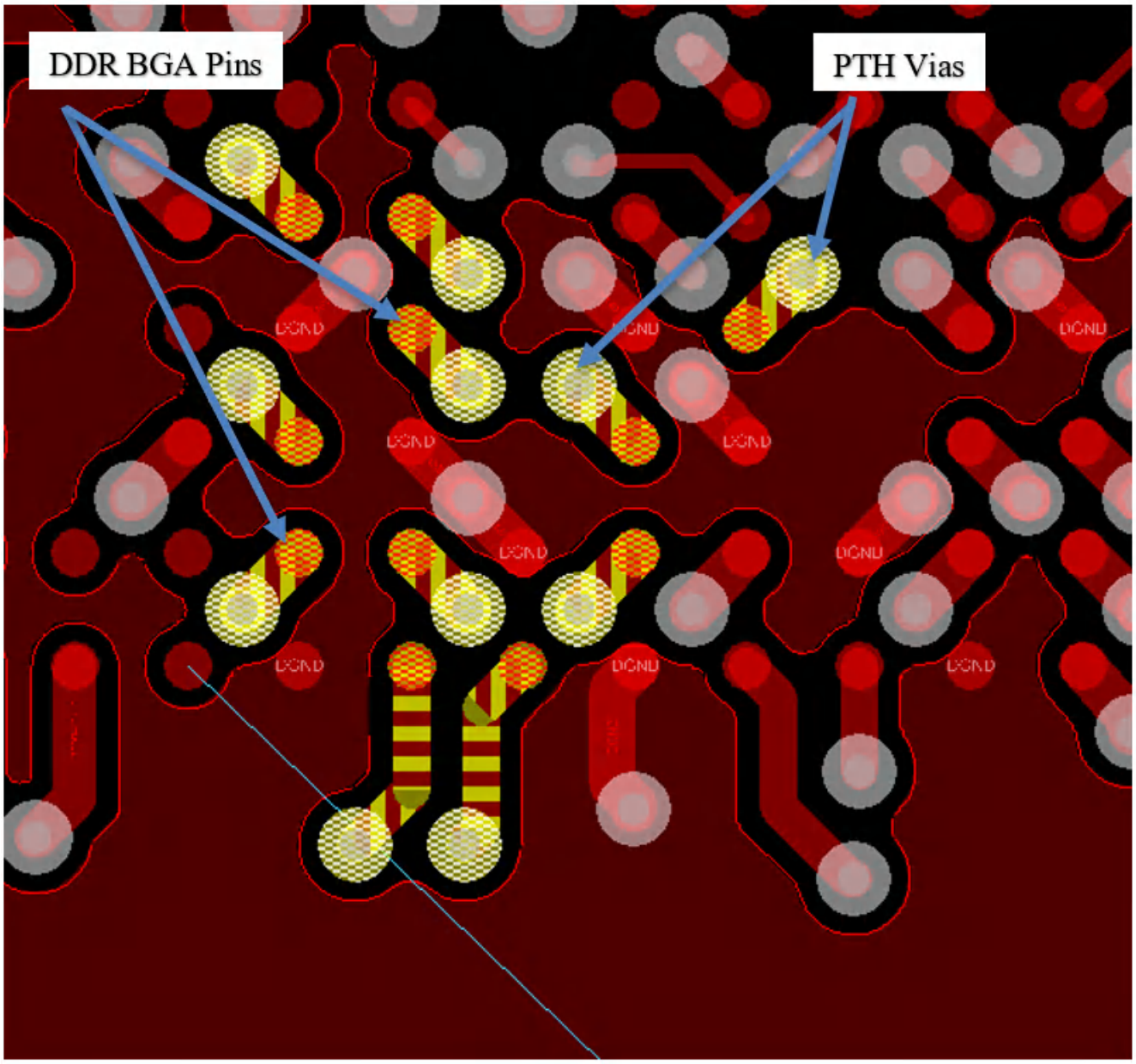

Figure 10-3. DDR Data Byte Lane 2 Escape

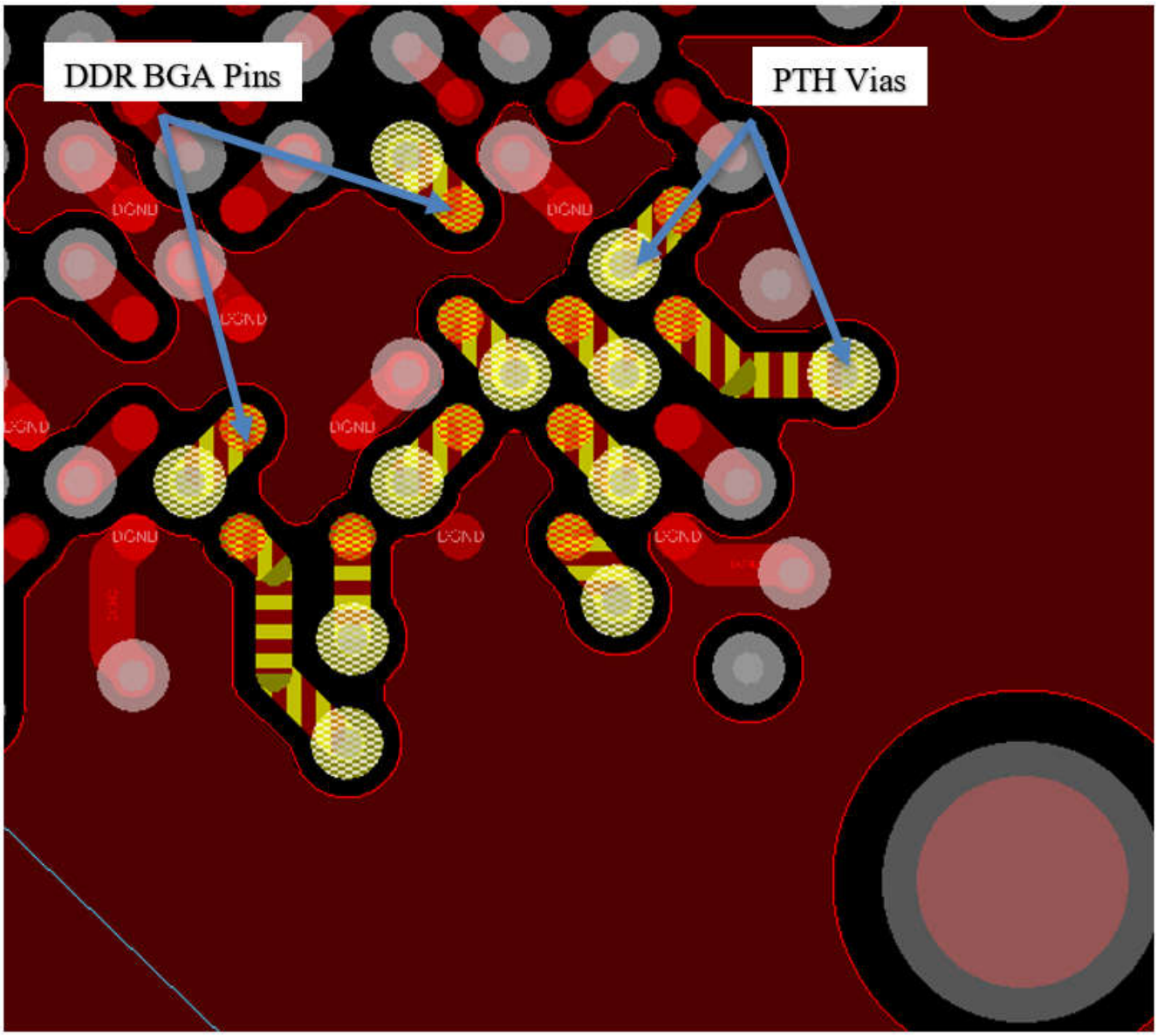

Figure 10-4. DDR Data Byte Lane 3 Escape

The address, command, and clock signals are routed directly to the memory device.

The top and inner layers are used to escape and route the address and command signals. The traces must be length matched to ensure that the signals arrive at the memory at the same time. Length matching must be from the SoC to memory pin individually and must include the stub to the memory pad and all via lengths. Refer to the DDR Routing Guidelines document for detailed recommendations for DDR routing.

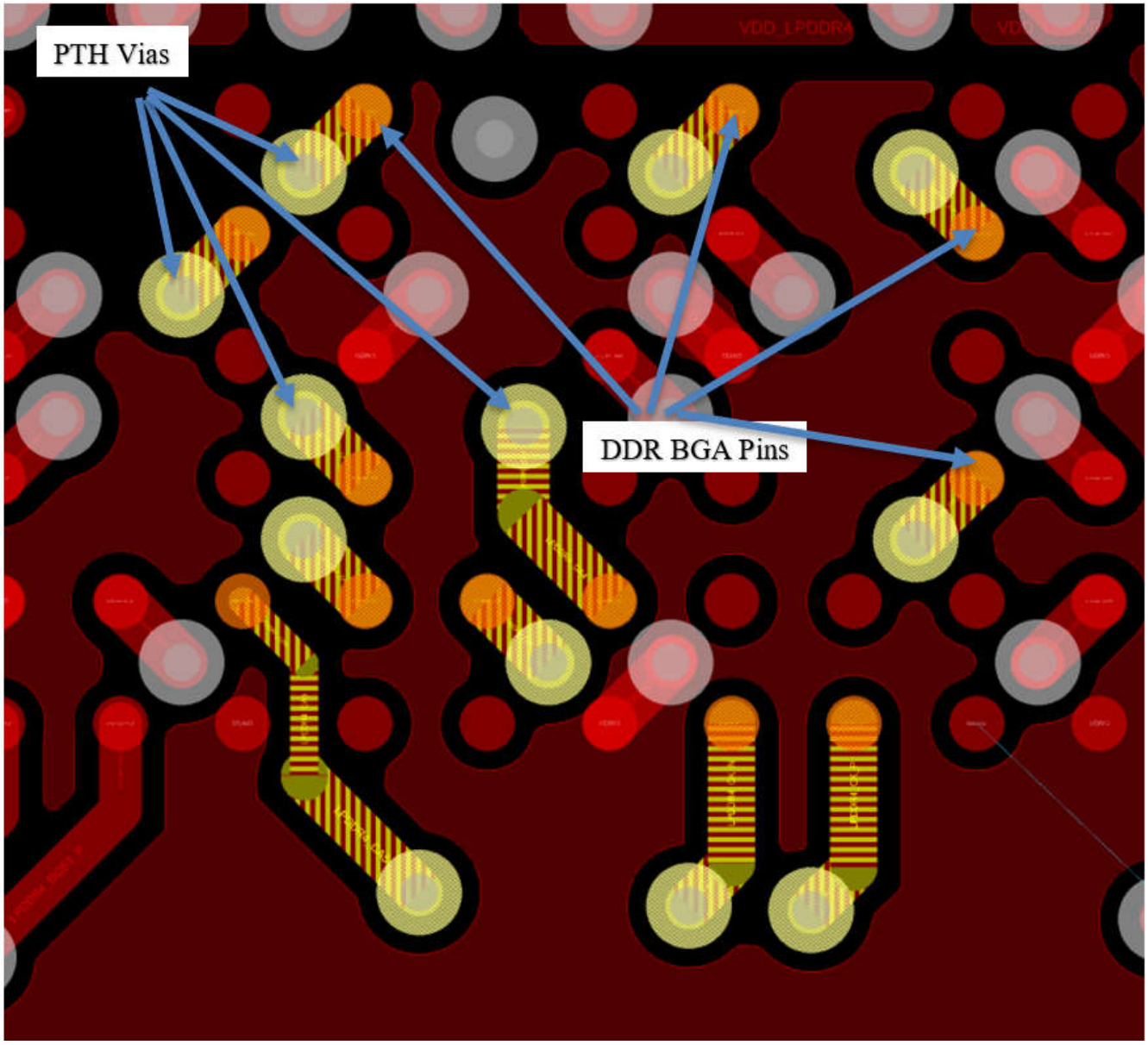

Figure 10-5. DDR Address/Cmd Escape

The escapes of the address and command signals on these layers are shown in Figure 10-5.

Address signals were routed directly from the SoC to the via next to the associated pad for the memory device. This requires that the address signals escape in the correct order. It is required to have the same number of vias for each of the address and command signals. The use of Plated Through Hole (PTH) vias allows the flexibility of routing the address/cmd signals on any layer.

11 Power Decoupling

The middle priority interfaces and the power distribution planes and pours would be routed next after the SerDes and DDR interfaces. It is strongly encouraged to complete all SerDes and DDR routing before continuing with other interfaces. The power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SerDes and DDR routes, as these can influence the return currents for the high-speed interfaces. The highest speed source-synchronous interfaces, such as RGMII and QSPI, may also require simulation, so these may also need to be completed at this time.

Special care is needed for the 1-uF output capacitors connected to the CAP_VDDS* BGA pins on the AM62Px device. These capacitors should be placed as close to the pin as possible and a low inductance path should be present between the CAP_VDDS BGA pin and the supply pad on the capacitor.

This placement can be improved if the capacitors can be placed directly under the SoC. The decoupling capacitors for the VDD_CORE and VDDS_DDR supplies should also receive the same priority as those on the CAP_VDDS* pins and should be placed under the socket, with minimum inductance connections to the respective BGA pins on the AM62Px device.

12 Route Lowest Priority Interfaces Last

When the length matching and simulations have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and then the lower priority interfaces.

13 Summary

The via channels have been carefully co-designed to ensure escapes for all signals and power while meeting the respective signal and power integrity goals for each interface.

A picture with AM62Px with all signals and power escaped is shown in Figure 13-1.

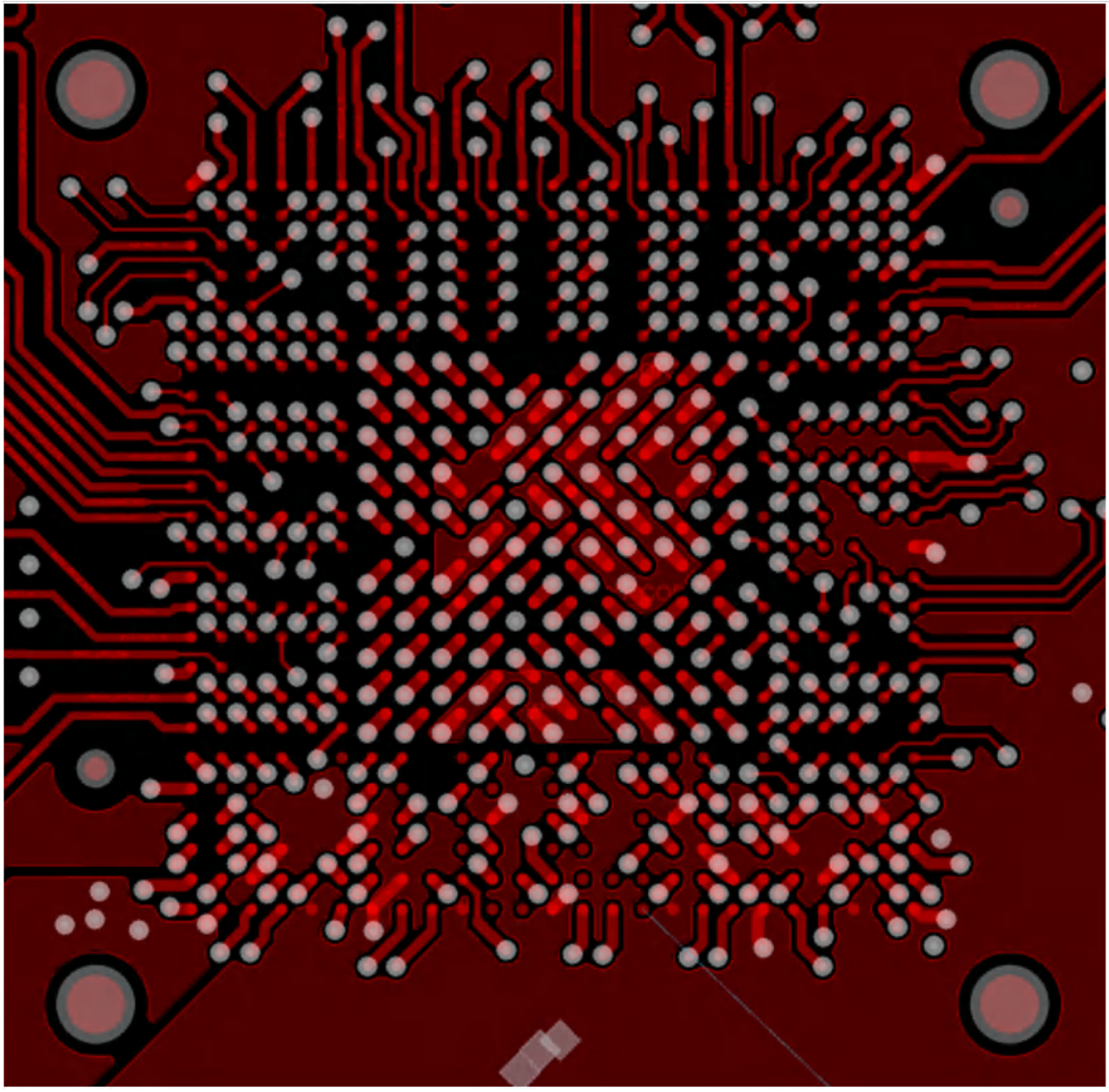

Figure 13-1. AM62Px with Complete Signal and Power Escapes

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 20, 2023 to January 31, 2024 (from Revision A (December 2023) to Revision B (January 2024))	Page
• Changed FBGA package size from 13mm x 13mm to 17mm x 17mm	2

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