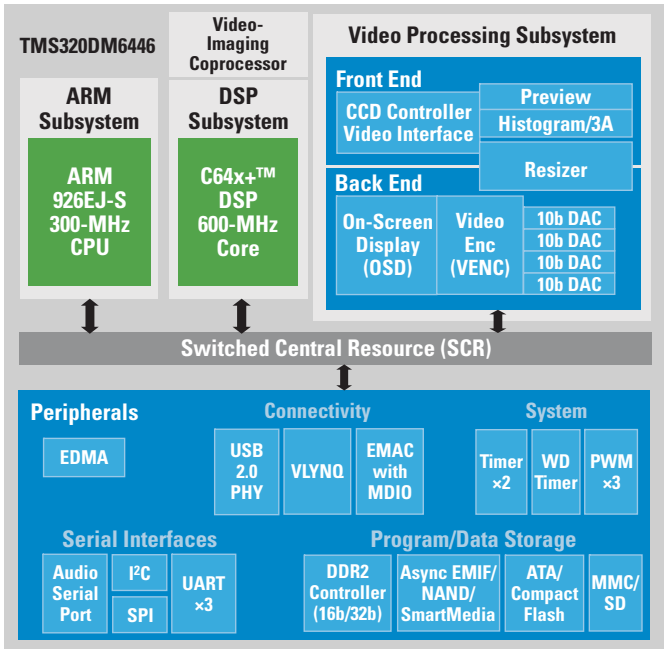
TMS320DM644x Digital Media Processors

Updated 1Q07

TMS320DM644x digital media processors are highly integrated SoCs based on an ARM926 processor and the TMS320C64x+™ DSP core. They are ideal for applications such as videophones, automotive infotainment, digital still cameras, streaming media, advanced set-top box and portable media devices such as security netcams and DVRs.

TMS320DM6446 Digital Media Processor Block Diagram



DaVinci™ Digital Media Processors in Production Now

Device	CPUs	Frequency (MHz)	L1/ SRAM (Bytes)	L2/ SRAM (Bytes)	ROM (Bytes)	External Memory I/F	EDMA	Video Ports (Configurable)	Serial I/F	Connectivity I/F	Program/ Data Storage	Voltage (V) Core	Voltage (V) I/O	Packaging	Price[1]
TMS320**DM6446**ZWT	C64x+, ARM9, DaVinci Video	594 (DSP) 297 (ARM)	112 K (DSP) 40 K (ARM)	64 K (DSP)	16 K (ARM)	1 16-/8-Bit EMIFA 1 32-/16-Bit DDR2	64 Ch	1 Input, 1 Output	ASP, I²C, SPI, 3 UARTs	USB 2.0, VLYNQ, 10/100 EMAC	Async SRAM, DDR2 SDRAM, NAND Flash, SmartMedia/xD	1.2	1.8/ 3.3	361 BGA, 16 × 16 mm	39.49
TMS320**DM6443**ZWT	C64x+, ARM9, DaVinci Video	594 (DSP) 297 (ARM)	112 K (DSP) 40 K (ARM)	64 K (DSP)	16 K (ARM)	1 16-/8-Bit EMIFA 1 32-/16-Bit DDR2	64 Ch	1 Output	ASP, I²C, SPI, 3 UARTs	USB 2.0, VLYNQ, 10/100 EMAC	Async SRAM, DDR2 SDRAM, NAND Flash, SmartMedia/xD	1.2	1.8/ 3.3	361 BGA, 16 × 16 mm	33.84
TMS320**DM6441**ZWT	C64x+, ARM9, DaVinci Video	513/405 (DSP) 256/202 (ARM)	112 K (DSP) 40 K (ARM)	64 K (DSP)	16 K (ARM)	1 16-/8-Bit EMIFA 1 32-/16-Bit DDR2	64 Ch	1 Input, 1 Output	ASP, I²C, SPI, 3 UARTs	USB 2.0, VLYNQ, 10/100 EMAC	Async SRAM, DDR2 SDRAM, NAND Flash, SmartMedia/xD	1.2/ 1.05	1.8/ 3.3	361 BGA, 16 × 16 mm	27.05

[1] *Prices are quoted in U.S. dollars and represent year 2007 suggested resale pricing. All prices are subject to change. Customers are advised to obtain the most current and complete pricing information from TI prior to placing orders. TI may verify final pricing prior to accepting any order.*

New devices are listed in red.

DaVinci™ Hardware and Software Development Tools

Digital Video Evaluation Module

Digital Video Evaluation Module (DVEVM) – The DVEVM enables developers to start immediate evaluation of the TMS320DM644x processors and begin building digital video applications quickly. The DVEVM allows developers to write production-ready application code for the ARM and provides access to the DSP core using DaVinci APIs. For more information visit **www.ti.com/dvevm**

Digital Video Software Development Kit

Digital Video Software Development Kit (DVSDK) – The Digital Video Software Development Kit (DVSDK) is designed to tune complex systems quickly and efficiently by incorporating multiple tools that significantly improve software integration and system visibility. The DVSDK requires a target platform for the TMS320DM644x processor and can be used in conjunction with the DVEVM or platforms from TI third parties. Review technical documents or learn specifics of the DVSDK at **www.ti.com/dvsdk**

DaVinci Hardware and Software Development Tools

Description	Part Number	$U.S.[1]
Evaluation Modules (EVMs)		
Digital Video Evaluation Module (DVEVM)	TMDXEVM6446 (U.S. part number) TMDXEVM6446-0E (European part number)	2,495
Digital Video Software Development Kit (DVSDK) with MontaVista™ Pro Linux, Code Composer Studio™ IDE and XDS560™ Emulator	TMDSSDK6446-L (U.S. part number) TMDSSDK6446-3L (U.S. part number)	6,995 10,995

[1] Prices are quoted in U.S. dollars and represent year 2007 suggested resale pricing. All prices are subject to change. Customers are advised to obtain the most current and complete pricing information from TI prior to placing orders. TI may verify final pricing prior to accepting any order.

New tools are listed in red.

Digital Media Software

eXpressDSP™ Digital Media Software is production tested and optimized for a portfolio of DSP and SoC platforms. Instead of investing time and effort in standardized media software, manufacturers are able to save years of development time to differentiate their digital media products. eXpressDSP digital media software is available for free evaluation and numerous flexible pricing options exist to fit any development need. Visit **www.ti.com/digitalmediasoftware** to:

- Evaluate digital media software at no charge for 60 days with a simple click-wrap license.
- Learn more about flexible production licensing that allows for a range of pricing options based on project quantity and download 10 KU volume pricing options.

Unlike example software or freeware, all digital media software components have been developed by following stringent coding guidelines. Accompanying each module is a re-targetable production library featuring reentrant code. Each module is fully documented with a datasheet, release notes, user guide and usage examples.

All digital media software is both unit tested and system tested by applying thousands of test vectors in world-class testing labs. In addition, a wide range of use-case scenarios from end equipments/applications, including cell phones, wireless networking, video/IP phones, streaming media, set-top boxes and others contribute to the library of test vectors used to validate each algorithm.

Current Listing of eXpressDSP Digital Media Software

e = encode **d** = decode

Currently Available	Available 1H 2007
H.264 MP **d** D1	WMV9 MP / VC1 **d** D1
H.264 BP **e/d** D1	WMV9 MP / VC1 **e** D1
MPEG-4 SP **e/d** D1	WMA8 **e**
MPEG-2 MP **d** D1	AAC HE **e**
JPEG **e/d** D1	AAC LC **e**
AAC LC **d**	G.729 AB **e/d**
MP3 **d**	G.726 **e/d**
G.711 **e/d**	G.723.1 **e/d**
HE-AAC **d**	
AC3 **d**	
WMA9 **d**	

Authorized Software Providers Support TI Digital Media Software

TI's Digital Media Software is fully supported through a worldwide network of Authorized Software Providers (ASPs). Highly qualified, trained ASPs make evaluation and implementation easy, so you can focus on differentiating products and accelerating your time-to-market.

Start your evaluation today – Offering production-ready software, and robust support, the TI Digital Media Software program includes:

- A free 60-day evaluation period, including four hours of technical support from your ASP
- Flexible production licensing models, which include up to 40 hours of technical support from your ASP

Authorized Software Providers by Region

	Regions						
ASPs	Americas	Europe	China	Asia – Other	Japan	Korea	India
ATEME	X	X	X	X	X	X	
eInfochips	X	X					X
eSOL					X		
Ingenient	X	X	X	X	X	X	
Ittiam	X	X		X	X	X	X
Logic	X						
MPC Data		X					
Wintech Digital			X	X			X

DaVinci Performance Benchmarks

TMS320DM644x Processor Video Capabilities

	TMS320DM6446	TMS320DM6443
STANDALONE CODECS		
MPEG-2 MP ML decode	720p (30 fps)	720p (30 fps)
MPEG-2 MP ML encode	D1^{+}	n/a
MPEG-4 SP decode	720p (30 fps)	720p (30 fps)
MPEG-4 SP encode	D1^{+}	n/a
VC1/WMV 9 decode	720p (30 fps)	720p (30 fps)
VC1/WMV 9 encode	D1^{+}	n/a
H.264 (Baseline) decode	D1^{+}	D1^{+}
H.264 (Baseline) encode	D1^{+}	n/a
H.264 (Main Profile) decode	D1^{+}	D1^{+}

$^{+}$ Denotes available processor headroom for analytics and/or other features
Encode is only available on the DM6446 processor.
Note: Performance will vary depending on efficiency of code and data stream used.
Resolution information: D1 (720×480) / 720p (1280×720)
Theoretical device capability may be available from some third parties. TI codecs currently tested only to D1 resolution.
Device capability estimated based on 600-MHz DM644x devices. Lower-speed-grade versions may be limited to lower resolutions.

All performance data is for 30-fps YUV 4:2:0 unless otherwise noted.
SP = Simple Profile / MP= Main Profile

The TMS320DM644x devices, available today, are based on the TMS320C64x+™ DSP core. TMS320C64x+ DSP core benchmarks include:

Filters

Benchmark	Description	Formula
Complex FIR filter	Computes a complex FIR filter (direct-form) with nh coefficients and nr output samples. Nh and nr must be a multiple of 4.	nh * nr / 2 + 16 For nh = 32 and nr = 100: cycles = 1616
FIR filter	Computes a real FIR filter (direct-form) with nh coefficients and nr output samples. Nh and nr must be a multiple of 8.	T ≥ 32: nh * nr / 8 + 22 Other: 32 * nr / 8 + 22 For nh = 32 and nr = 100: cycles = 422
IIR biquad	Performs single biquad IIR filter for nx samples.	nx*4 + 25 For nx = 16: cycles = 89
Autocorrelation	Performs nr autocorrelations, each of length nx, producing nr output results.	nx < nx ≥ 40: 20 + (2 * nr) + (nx * nr / 8) For nr = 160, nx = 40: cycles = 1140

FFTs

Benchmark	Description	Formula
Complex, forward FFT (radix 4) with digit reversal	Computes a complex forward radix-4 nx-point FFT. Input data, output data and coefficients are 16-bit.	0.75*nx*log4(nx) + 38 For nx = 1024: cycles = 3878
Extended-precision, mixed-radix 16×32 FFT with rounding, digit reversal	Computes an extended-precision complex forward mixed-radix nx-point FFT with rounding and digit reversal. Input data and output data are 32-bit, coefficients are 16-bit.	[10.25*nx/8+10]*ceil[log4(nx) – 1] + 6*nx/4 + 81 For nx = 124: cycles = 6905
Extended-precision, mixed-radix 32×32 FFT with rounding, digit reversal	Computes an extended-precision complex-forward mixed-radix nx-point FFT with rounding and digit reversal. Input data, output data and coefficients are 32-bit.	[12*nx/8+12]*ceil[log4(nx) – 1] + 6*nx/4 + 47 For nx = 1024: cycles = 7775

Vector

Benchmark	Description	Formula
Vector dot product	Computes dot-product of two vectors of size nx elements.	nx/4 + 14 For nx = 100: cycles = 39
Vector sum	Computes and nx-element vector sum of two vectors. The result is stored in a third vector.	3*(nx/8) + 10 For nx = 256: cycles = 106

Search

Benchmark	Description	Formula
Maximum value of a vector	Finds the element with maximum value in a vector of size nx.	nx/8 + 13 For nx = 256: cycles = 45
Index of the maximum element of a vector	Finds the index of the element with the maximum value in a vector of size nx.	nx/4 + 20 For nx = 100: cycles = 45

Image/Video Compression/Decompression

Benchmark	Description	Formula
8×8 block forward discrete cosine transfrom (FDCT)	Computes a series of num_fdcts 8×8 forward discrete cosine transforms (FDCT)	num_fdcts * 52 + 56 For num_fdcts = 6: cycles = 368
8×8 block inverse discrete cosine transform (IDCT)	Computes a series of num_idcts IEEE 1180 - 1990 compliant 8×8 inverse discrete cosine transforms (IDCT)	num_idcts * 72 + 63 For num_idcts = 6: cycles = 495

Telecom

Benchmark	Description	Formula
convenc3	Implements rate=1/3, R=9 convolutional encoding.	cycles = 14 + 3*ceil((nbits+8)/32) For nbits = 512: cycles = 65
crc32	Compute 32-bit cyclic redundancy check (CRC) of the input data.	14 + N/2, N = num of Bytes For N = 128: cycles = 78

For the most up-to-date information, visit www.ti.com/davinci

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