OMAP5912 Multimedia Processor Camera Interface Reference Guide

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Preface

Read This First

About This Manual

This document describes the camera interface implemented in the OMAP5912 multimedia processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

Documentation that describes the OMAP5912 device, related peripherals, and other technical collateral, is available in the OMAP5912 Product Folder on TI's website: www.ti.com/omap5912.

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Contents

Figures

Tables

Camera Interface

This document describes the camera interface implemented in the OMAP5912 multimedia processor.

1 Camera Parallel Interface

A 32-bit camera interface connects a camera module to the MPU OCP bus (in production silicon OMAP5912, formerly called peripheral bus in XOMAP5912 and POMAP5912 silicon) of the device. The interface handles multiple image formats synchronized on vertical and horizontal synchronization signals. Data transfer between the camera and the interface can be done synchronously or asynchronously. The data is stored in a buffer to be sent over the OCP bus, using the DMA mode or the CPU mode (bypass mode).

The interface supports 8-bit parallel image data ports and horizontal/vertical signal ports separately (stand-alone synchronous method). The camera interface has a DMA port. For pre-production silicon (i.e., XOMAP5912 or POMAP5912), the camera interfaces use the TI-peripheral bus for internal connectivity. For production silicon (OMAP5912), the camera interface uses the OCP-TI/OCP-T2 bus (see Figure 1).

1.1 Functional Architecture

The camera architecture consists of four functional blocks:

- Buffer: Stores the data word received from the camera module and transfers it to the MPU peripheral bridge, using the DMA mode or the CPU mode. It contains a 128-word FIFO.

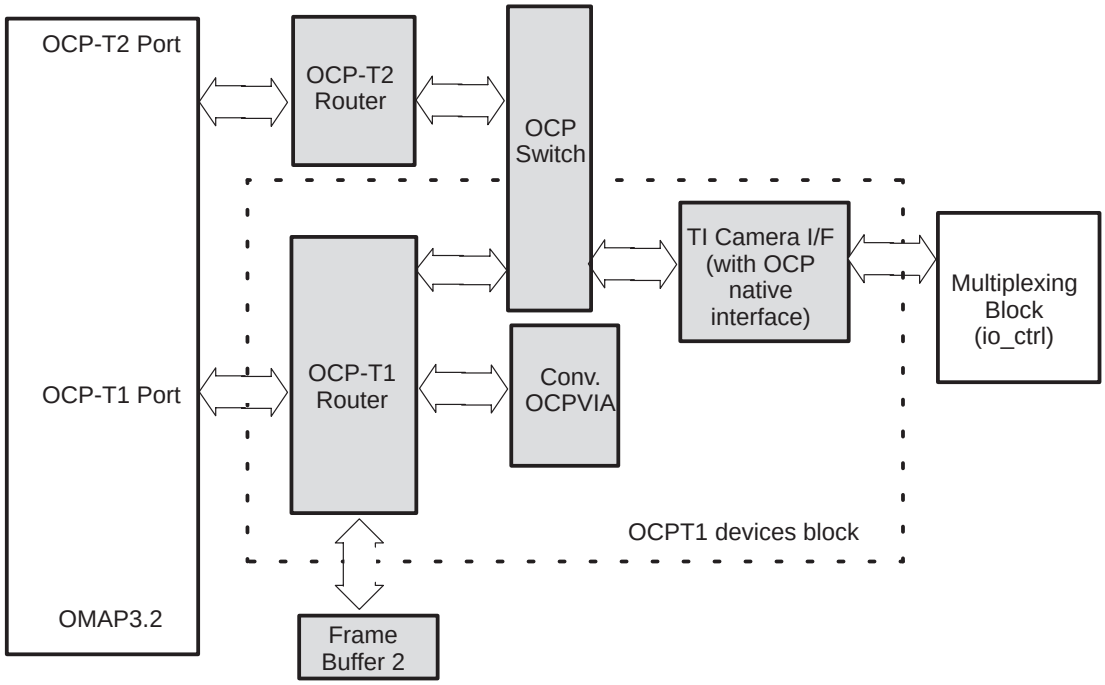
  The 8-bit data received from the camera module is packed into 32 bits. A 128-bit-deep FIFO is implemented to provide local buffering of the data and to control the DMA request when the camera interface is enabled in DMA mode. The main goals of this mode are:

  - To discharge the CPU of the data transfer
  - To reduce the real time constraints of the DMA read (FIFO buffering part)
  - To group the x DMA accesses in only one time slot (FIFO block part)

  The user can, however, forward a direct transfer to the CPU in bypass mode by disabling the DMA request line.

- Clock divider: Manages the clock division and handles the external clock generation for synchronous/asynchronous mode gating.
- Interrupt generator: Generates an interrupt to indicate the start and end of frame, start and end of image, and FIFO overflow.
- Registers: Connect status, control, and data 32-bit registers.

Figure 1. Camera Interface Interconnects for Production Silicon



1.1.1 Camera IF Clocks

For production silicon (OMAP5912), the camera IF functional clock is either the TC2_CK divided down (see the CONTROLCLK.FOCSMOD bits for divide-down options) or CAM.LCLK (input pin J15). The camera IF interface clock is TC2_CK.

For pre-production silicon (XOMAP5912 or POMAP5912), the camera IF functional clock is either the ARMPER_CK divided down (see the CONTROLCLK.FOCSMOD bits for divide-down options) or CAM.LCLK (input pin J15). The camera IF interface clock is ARMPER_CK.

1.1.2 Camera Data Validation

The incoming byte on CAM_D can be latched on the rising or falling edge of CAM.LCLK generated by the camera itself. The POLCLK bit in the clock control register selects the polarity of CAM.LCLK.

The camera interface must be programmed so that data is always captured opposite the launch edge. For example, if data is latched by the sensor on the rising edge of CAM.LCLK, the interface must be configured to catch the data on the falling edge of CAM.LCLK.

The high level of the vertical synchronous and horizontal synchronous signals indicates that the data is valid on CAM_D. This level is registered in VSTATUS and HSTATUS, which are updated at edge detection of vertical and horizontal synchronous signals.

Figure 2 shows the image data transfer, and Figure 3 shows the timing chart.

Figure 2. Image Data Transfer

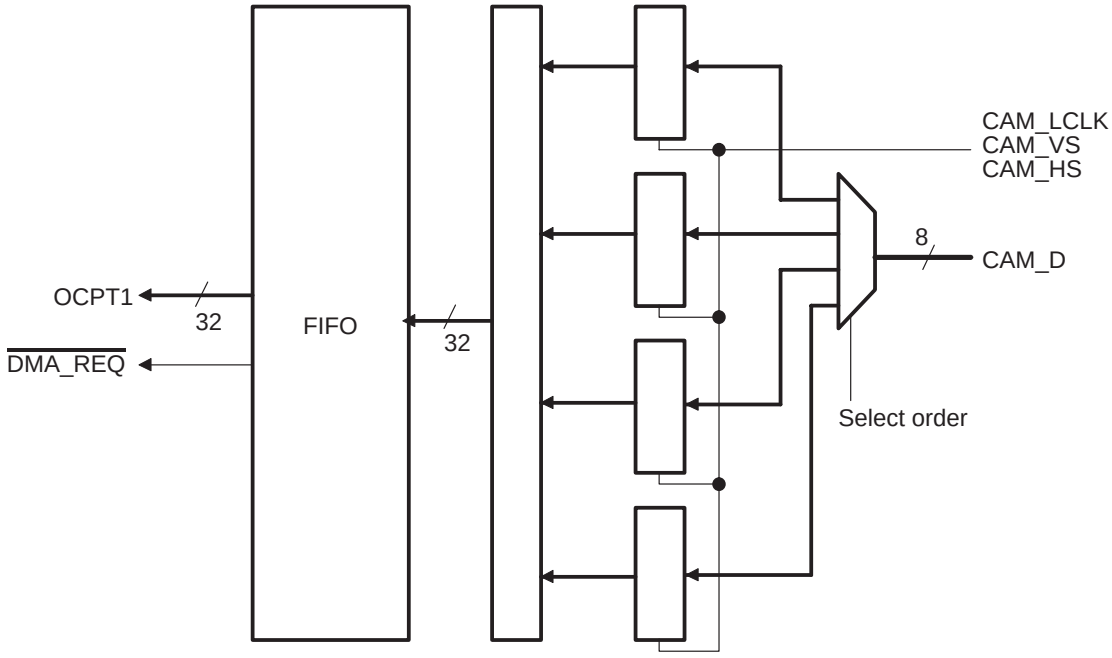
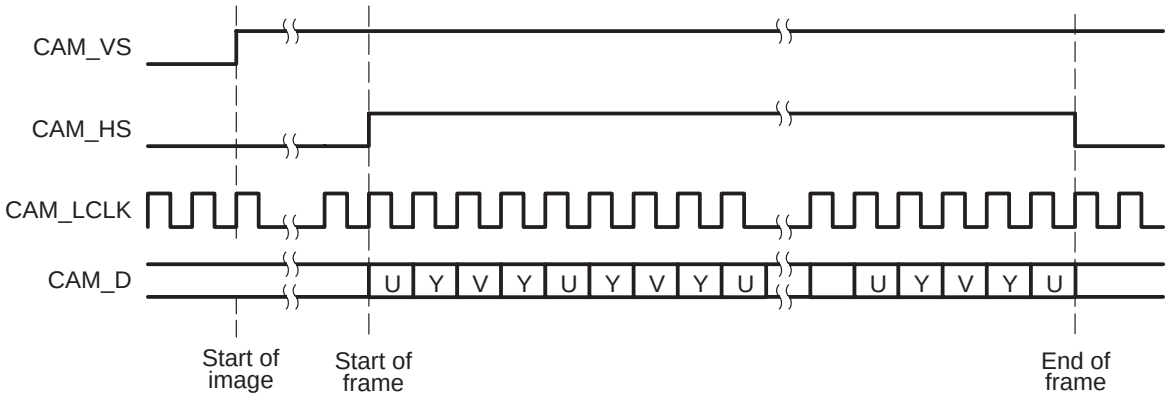


Figure 3. Timing Chart of Image Data Transfer (POLCLK = 1)



The clock can be gated during the VSYNC and/or HSYNC blanking periods, but it must be left to run because a process based on LCLK clears all internal resynchronization registers while VSYNC or HSYNC is low, before starting a new frame or new image. This mechanism prevents the FIFO from retaining any remaining (and likely garbage) data left over from a previous frame, which could corrupt the data of a new frame.

If either CAM_VS or CAM_HS goes inactive before receiving all four bytes, the data in buffers is cleared by the active CAM.LCLK edge and is not written into FIFO.

1.1.3 Autostart

Autostart is a protection function that prevents a start of capture during an image transfer. Autostart is launched after enabling the LCLK and waits for the next inactive level of CAM_VS to enable the data capture so that the transfer starts at the beginning of the image.

Note:

If a reset FIFO occurs (see section 1.1.4) while the interface is latching data, the capture is automatically disabled and the autostart function is enabled.

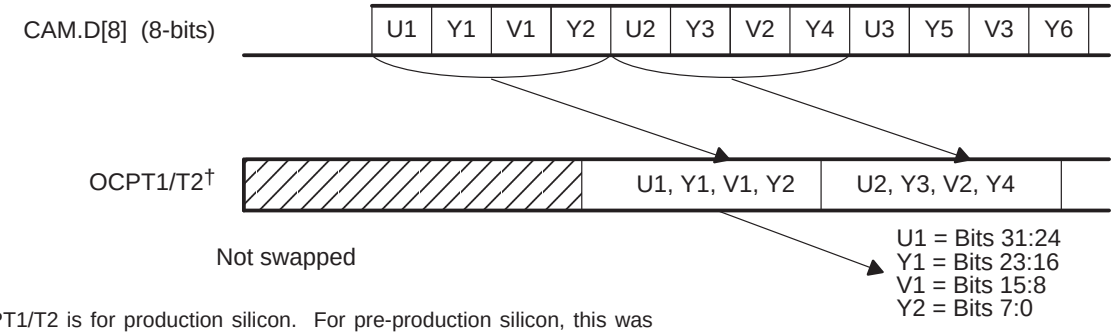
1.1.4 Reset FIFO

An active-high reset FIFO is implemented at the RAZ_FIFO bit (18) of the camera mode register. This feature clears any remaining data in the FIFO before starting a new transfer. It also resets all status and control signals around the FIFO, such as the read and write pointers, the FIFO full interrupt, the FIFO peak counter, and the 32-bit resynchronization registers.

1.1.5 Set of Order

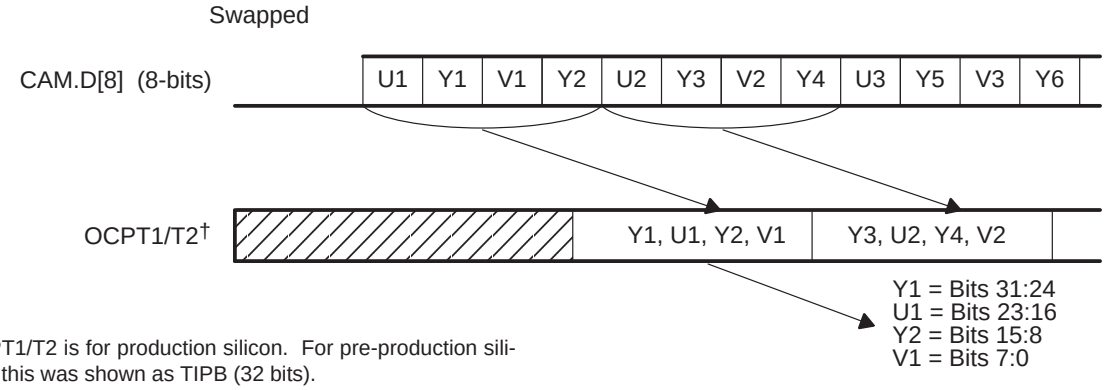
Each four bytes received from the camera must be packed and can be swapped to follow the order YUV specified in the camera mode register by ORDERCAMD. Figure 4 and Figure 5 show the camera data order not swapped and swapped, respectively.

Figure 4. Order of Camera Data on TIPB (Not Swapped)



† OCPT1/T2 is for production silicon. For pre-production silicon, this was shown as TIPB (32 bits).

Figure 5. Order of Camera Data on TIPB (Swapped)



† OCPT1/T2 is for production silicon. For pre-production silicon, this was shown as TIPB (32 bits).

1.1.6 FIFO Buffer (128 x 32)

A write access is applied to the FIFO for each 32-bit word received. When the write FIFO counter reaches the trigger level, an interrupt request can be generated. The trigger level is programmable.

In DMA mode, the threshold can be programmed between 1 and 128, but the DMA must be set up to read the threshold amount out of FIFO per the DMA request issued by the camera interface. Otherwise, the locking mechanism is

never rearmed, and it prevents DMA requests from being issued after every read.

A pulse on the DMA request (see Figure 6 and Figure 7) occurs when the number of words in the FIFO is above the threshold. The DMA request occurs if the number of remaining words is above the threshold and the system DMA has completed the transfer (number of words read by the DMA = threshold).

The camera FIFO continues to fill (up to its maximum 128 values) when an interrupt or DMA request has been generated but not responded to yet. When a data value is read from the camera FIFO, another IRQ or DMA request is immediately generated, as long as the amount of data present in the FIFO is above the trigger level.

Figure 6. DMA Request

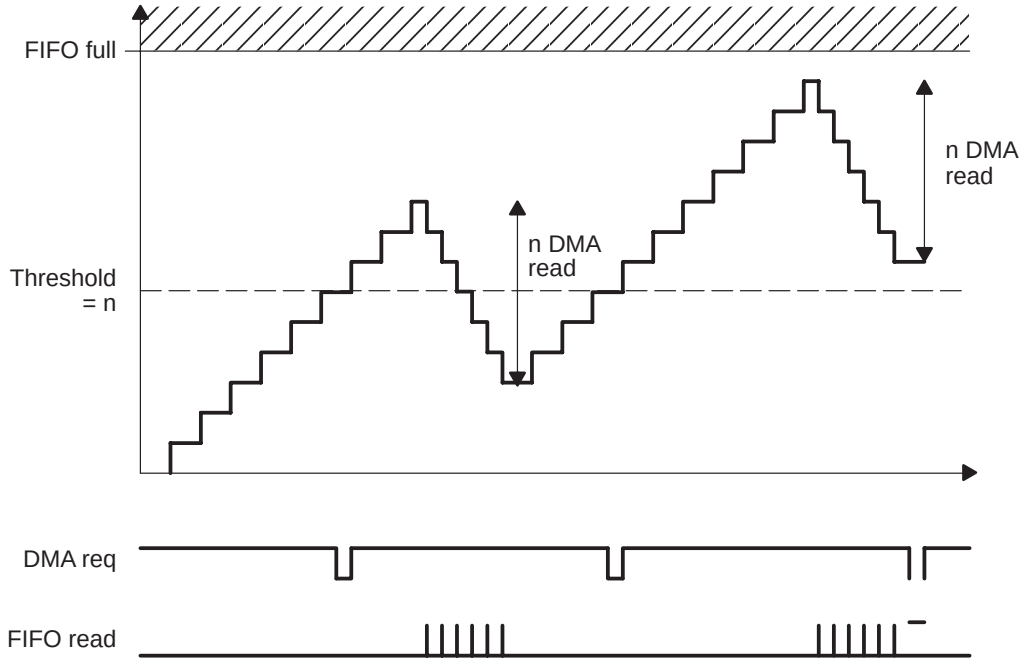
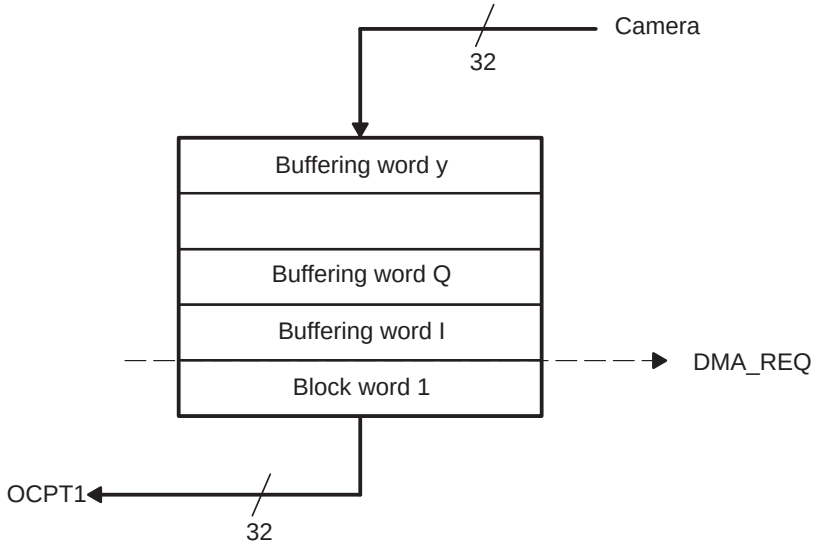


Figure 7. FIFO Buffer Parts



1.1.7 Clock Divider

The clock divider takes the ARMPER_CK clock source to generate the external clock CAM.EXCLK. The division factor is programmable in the clock control register through FOSCMOD (see Table 3).

It is assumed that the switch is made when CAM.EXCLK is disabled (glitch protection).

The clock divider also allows disabling the external clock by setting the CAMEXCLK_EN bit.

1.1.8 Interrupt Generator

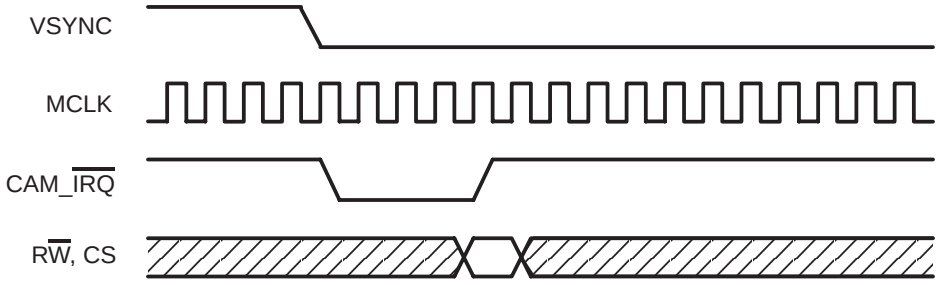
The interrupt generator handles six cases of interrupt:

- ❏ Data transfer interrupt. One IRQ is generated per word received.
- ❏ HSYNC rising edge (start of frame)
- ❏ HSYNC falling edge (end of frame). See Figure 8.
- ❏ VSYNC rising edge (start of image)
- ❏ VSYNC falling edge (end of image)
- ❏ FIFO overflow

Each case is registered by activating (high) one of the six interrupt register bits to indicate the origin of the interrupt. However, the interrupt mask register can disable the source of the interruption.

Only one line of interrupt is used to ask for a read of the interrupt register. When the read occurs, the register is automatically reset and the interrupt signal is released.

Figure 8. IRQ Generated on VSYNC Falling Edge



1.1.9 DMA Procedure

A typical procedure to perform the data transfer by DMA is as follows:

1) Rising edge of VSYNC sends an interrupt to ARM926EJS to alert the system DMA that a start of image has occurred. The system DMA is programmed to move one complete image of data, and give an interrupt when complete.

2) High level of HSYNC and proper clock edge start the first data transfer from the camera to the camera interface. After the first two pixels of data are received (8 bits x 4 transfers = 32 bits), a DMA request is made. The system DMA moves the 32-bit data to a predefined SDRAM location.

3) The camera, the device camera interface, and the system DMA continue the transfer of data. That is, 352/2 * 288 = 50688 transfers for a camera interface image format. After the full image is transferred, the DMA sends an interrupt to the ARM926EJS to signal that the end of frame occurred.

The camera interface and system DMA can be configured in many ways to move the data, but in this sequence the interrupt load on the ARM926EJS is minimal.

1.1.10 Camera IF Registers

The camera interface contains several registers for communication between the TIPB (in pre-production silicon) or OCPT1/T2 (production silicon) and the camera module. These registers mainly control clock generation, interrupt request, and status register (see section 1.1.11).

Table 1 shows the default configuration at reset.

Table 1. Default Configuration at Reset

Item	Function
ORDERCAMD	Not swapped
MASK	Interrupts on VSYNC and HSYNC disabled
FOSCMOD	Division rate for CAM.EXCLK = 1 (12 MHz)
POLCLK	Data latched on rising edge of CAM.LCLK
CAMEXCLK_EN	CAM.EXCLK disabled
MCLK_EN	Internal clock disabled
APLL_EN	APLL clock source disabled
THRESHOLD	Trigger level = 1 word

1.1.11 Camera Interface Registers

Table 2 lists the camera interface registers. Table 3 through Table 9 describe the bits of the individual registers.

Table 2. Camera Interface Registers

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1)†				
Register	**Description**	**R/W**	**Size**	**Offset**
CTRLCLOCK	Clock control	R/W	32 bits	0x00
IT_STATUS	Interrupt source status	R	32 bits	0x04
MODE	Camera interface mode configuration	R/W	32 bits	0x08
STATUS	Status	R	32 bits	0x0C
CAMDATA	Image data	R	32 bits	0x10

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.
‡ These registers are available only on production silicon.
The register base addresses for production silicon camera interface are:
0x2007 D800 (when CONF_5912_CTRL[6] = 0)
0x3007 D800 (when CONF_5912_CTRL[6] = 1)

Table 2. Camera Interface Registers (Continued)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1)†				
Register	**Description**	**R/W**	**Size**	**Offset**
GPIO	Camera interface GPIO (general-purpose input/output)	R/W	32 bits	0x14
PEAK_COUNTER	FIFO peak counter	R/W	32 bits	0x18
CONF_5912_CTRL	Configuration Control‡	R/W	32 bits	0xFFFE 1150
BURSTDATA0	Burst Data 0‡	R/W	32 bits	0x20
BURSTDATA1	Burst Data 1‡	R/W	32 bits	0x24
BURSTDATA2	Burst Data 2‡	R/W	32 bits	0x28
BURSTDATA3	Burst Data 3‡	R/W	32 bits	0x2C

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.
‡ These registers are available only on production silicon.
The register base addresses for production silicon camera interface are:
0x2007 D800 (when CONF_5912_CTRL[6] = 0)
0x3007 D800 (when CONF_5912_CTRL[6] = 1)

Table 3. Clock Control Register (CTRLCLOCK)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x00)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:8	RESERVED	This field is reserved (unknown value after reset).	R/W	ND
7	LCLK_EN	0: Disables. 1: Enables incoming CAM.LCLK.	R/W	0x0
6	RESERVED	Reserved	R/W	0x0
5	MCLK_EN	MCLK_EN must be set prior to reading any camera register. 0: Disables. 1: Enables internal clock of interface.	R/W	0x0
4	CAMEXCLK_EN	0: Disables. 1: Enables CAM.EXCLK.	R/W	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 3. Clock Control Register (CTRLCLOCK) (Continued)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x00)†

Bit	Name	Function	R/W	Reset
3	POLCLK	Sets polarity of CAM.LCLK: 0: Data latched on rising edge. 1: Data latched on falling edge.	R/W	0x0
2:0	FOSCMOD	Sets the frequency of the CAM.EXCLK clock These are for production silicon only; for earlier versions of silicon, TC2_CK should be shown as ARM_PER_CK 000: TC2_CK / 8 (production silicon only) 001: TC2_CK / 3 010: TC2_CK / 16 011: TC2_CK / 2 100: TC2_CK / 10 101: TC2_CK / 4 110: TC2_CK / 12 111: Inactive	R/W	0x00

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

The MCLK_EN bit gates the 12-MHz master clock of the camera interface to either disable the clock when switching between two clock domains or save power consumption when the camera module is not used. To clear PEAK_COUNTER, read all data in FIFO and then write PEAK_COUNTER with 0.

Table 4. Interrupt Source Status Register (IT_STATUS)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x04)†

Bit	Name	Function	R/W	Reset
31:6	RESERVED	Reserved bits.	R	0xX
5	DATA_TRANSFER	Data transfer status. Set to 1 when trigger is reached. Reset by reading IT_STATUS if no event in the meantime.	R	0x0
4	FIFO_FULL	Detect rising edge on FIFO full flag. Reset by reading IT_STATUS if no event in the meantime.	R	0x0
3	H_DOWN	Flag for horizontal synchronous falling edge occurred. Reset by reading IT_STATUS if no event in the meantime.	R	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 4. Interrupt Source Status Register (IT_STATUS) (Continued)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x04)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
2	H_UP	Flag for horizontal synchronous rising edge occurred. Reset by reading IT_STATUS if no event in the meantime.	R	0x0
1	V_DOWN	Flag for vertical synchronous falling edge occurred. Reset by reading IT_STATUS if no event in the meantime.	R	0x0
0	V_UP	Flag for vertical synchronous rising edge occurred. Reset by reading IT_STATUS if no event in the meantime.	R	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 5. Camera Interface Mode Configuration Register (MODE)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x08)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:19	RESERVED	Reserved bits	R/W	0xX
18	RAZ_FIFO	When 1: Clears data in the FIFO; reinitializes read and write pointers; clears FIFO full interrupt, FIFO peak counter; and resynchronizes.	R/W	0x0
17	EN_FIFO_FULL	0: Disables. 1: Enables interrupt on FIFO_FULL.	R/W	0x0
16	EN_NIRQ	0: Disables. 1: Enables data transfer interrupt (bypass DMA mode).	R/W	0x0
15:9	THRESHOLD	Programmable DMA request trigger value. DMA request is made when FIFO counter is equal to the threshold value. Currently, set this field to 1 in DMA mode.	R/W	0x0000001
8	DMA	Enables DMA mode when 1.	R/W	0x0
7	EN_H_DOWN	Enables interrupt on HSYNC falling edge. Active when 1.	R/W	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 5. Camera Interface Mode Configuration Register (MODE) (Continued)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x08)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
6	EN_H_UP	Enables interrupt on HSYNC rising edge. Active when 1.	R/W	0x0
5	EN_V_DOWN	Enables interrupt on VSYNC falling edge. Active when 1.	R/W	0x0
4	EN_V_UP	Enables interrupt on VSYNC rising edge. Active when 1.	R/W	0x0
3	ORDERCAMD	Sets order of 2 consecutive bytes received from camera (YUV format). Not swapped when 0, swapped when 1.	R/W	0x0
2:1	IMGSIZE	Sets image size:. 00: CIF 01: QCIF 10: VGA 11: QVGA Currently, these bits have no effect on the operation of the camera interface.	R/W	0x00
0	CAMOSC	0: Set synchronous mode. 1: Set asynchronous mode. Currently, this has no effect on the camera interface.	R/W	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 6. Status Register (STATUS)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x0C)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:2	RESERVED	Reserved bits	R	0xX
1	HSTATUS	CAM_HS status (edge detection)	R	0x0
0	VSTATUS	CAM_VS status (edge detection)	R	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 7. Camera Interface GPIO Register (GPIO)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x14)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:1	RESERVED	Reserved bits	R/W	0xX
0	CAM_RST	Reset for camera module	R/W	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 8. Image Data Register (CAMDATA)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x10)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:0	CAMDATA	Image data from FIFO	R	0x0

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 9. FIFO Peak Counter Register (PEAK_COUNTER)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0x18)†				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:7	RESERVED	Reserved	R/W	Unknown
6:0	PEAK_COUNTER	Maximum number of words written to FIFO during the transfer since the last clear to zero	R/W	0x0000000

† For pre-production silicon (XOMAP5912 or POMAP5912) the base address = 0xFFFB 6800.

Table 10. Configuration Control Register (CONF_5912_CTRL) (production silicon only)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0xFFFE 1150)				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:8	RESERVED	Reserved	R/W	0x0000
7	RESERVED	Reserved	R/W	0x0
6	CAMERA_T1/T2	Define OCP target sources of TI camera 0: TI camera is on OCP T1 1: TI camera is on OCP T2	R/W	0x0
5	RESERVED	Not used	R	0x0
4	RESERVED	Reserved	R	0x0

Table 10. Configuration Control Register (CONF_5912_CTRL) (production silicon only) (Continued)

Base Address = 0x2007 D800 (when CONF_5912_CTRL[6] = 0 or 0x3007 D800 (when CONF_5912_CTRL[6] = 1) (Offset = 0xFFFE 1150)				
Bit	**Name**	**Function**	**R/W**	**Reset**
3	RESERVED	Reserved	R/W	0
2	RESERVED	This bit should be set to 0.	R/W	0
1	RESERVED	Reserved	R/W	1
0	RESERVED	Reserved	R/W	0

Table 11. Burst Data 0 Register (BURSTDATA0)

Base Address = Camera I/F (OCPT1/T2 (Offset = 0x20)				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:1	BURST0	First through fourth (0−3), respectively, element of image data from FIFO (burst access)	R/W	Unknown

Table 12. Burst Data 1 Register (BURSTDATA1)

Base Address = Camera I/F (OCPT1/T2 (Offset = 0x24)				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:1	BURST1	First through fourth (0−3), respectively, element of image data from FIFO (burst access)	R/W	Unknown

Table 13. Burst Data 2 Register (BURSTDATA2)

Base Address = Camera I/F (OCPT1/T2 (Offset = 0x28)				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:1	BURST2	First through fourth (0−3), respectively, element of image data from FIFO (burst access)	R/W	Unknown

Table 14. Burst Data 3 Register (BURSTDATA3)

Base Address = Camera I/F (OCPT1/T2 (Offset = 0x2C)				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:1	BURST3	First through fourth (0−3), respectively, element of image data from FIFO (burst access)	R/W	Unknown

1.2 Clock Switching Procedures

1.2.1 CAM.EXCLK Switch Protocol

The CAM.EXCLK switch protocol is required for any change of the CAM.EXCLK frequency value to first disable both the 12-MHz clock source and the APLL clock source in clock control registers:

1) Disable MCLK and APLL_CLK (MCLK_EN = 0, DPLL_EN = 0, FOSCMOD = FOSCMOD).

2) Change CAM.EXCLK value (FOSCMOD = new FOSCMOD).

3) Enable MCLK and APLL_CLK (MCLK_EN = 1, DPLL_EN = 1, FOSCMOD = FOSCMOD).

1.2.2 CAM.LCLK Switch Protocol

Bit 3 of the clock control register (POLCLK) sets the polarity of CAM.LCLK. CAM.LCLK must be disabled before selecting the rising or falling edge.

1) Disable CAM.LCLK (LCLK_EN = 0).

2) Set the new polarity (POLCLK = 1 or 0).

3) Enable CAM.LCLK (LCLK_EN = 1).

Revision History

Table 15 lists the changes made since the previous version of this document.

Table 15. Document Revision History

Page	Additions/Modifications/Deletions
7	Modified the second paragraph of Section 1
8	Added Figure 1 to show how the camera interface connects in the production silicon
8	Rewrote Section 1.1.1
11	Changed TIPB to OCPT1/T2 to reflect production silicon and added note explaining the previous silicon
11	Changed TIPB to OCPT1/T2 to reflect production silicon and added note explaining the previous silicon
15	Added production silicon information to Section 1.1.10
15	Added five new registers for production silicon to Table 2
16	Changed description for bits 5 and 2:0 in Table 3
20 − 21	Added Table 10 through Table 14 for new registers in production silicon

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