TMS320DM360x Digital Media System-on-Chip (DMSoC) Key Scan

User's Guide

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Read This First

About This Manual

This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRUFG5 — *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFG8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide* This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFG9 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide* This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH0 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide* This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH1 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide* This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFH2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide*** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFH3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide*** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.

SPRUFH5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide*** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH6 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide*** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide*** This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide*** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

SPRUFH9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide*** This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFI0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide*** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFI1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide*** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFI2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFI3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide*** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.

SPRUFI4 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide*** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide*** This document describes the operation of the ethernet media access controller interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide*** This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide*** This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide*** This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.

SPRUFJ0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide*** This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).

SPRUGG8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Face Detection User's Guide*This document describes the face detection capabilities for the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Introduction

The key scan module functions are described in this section.

1 Features

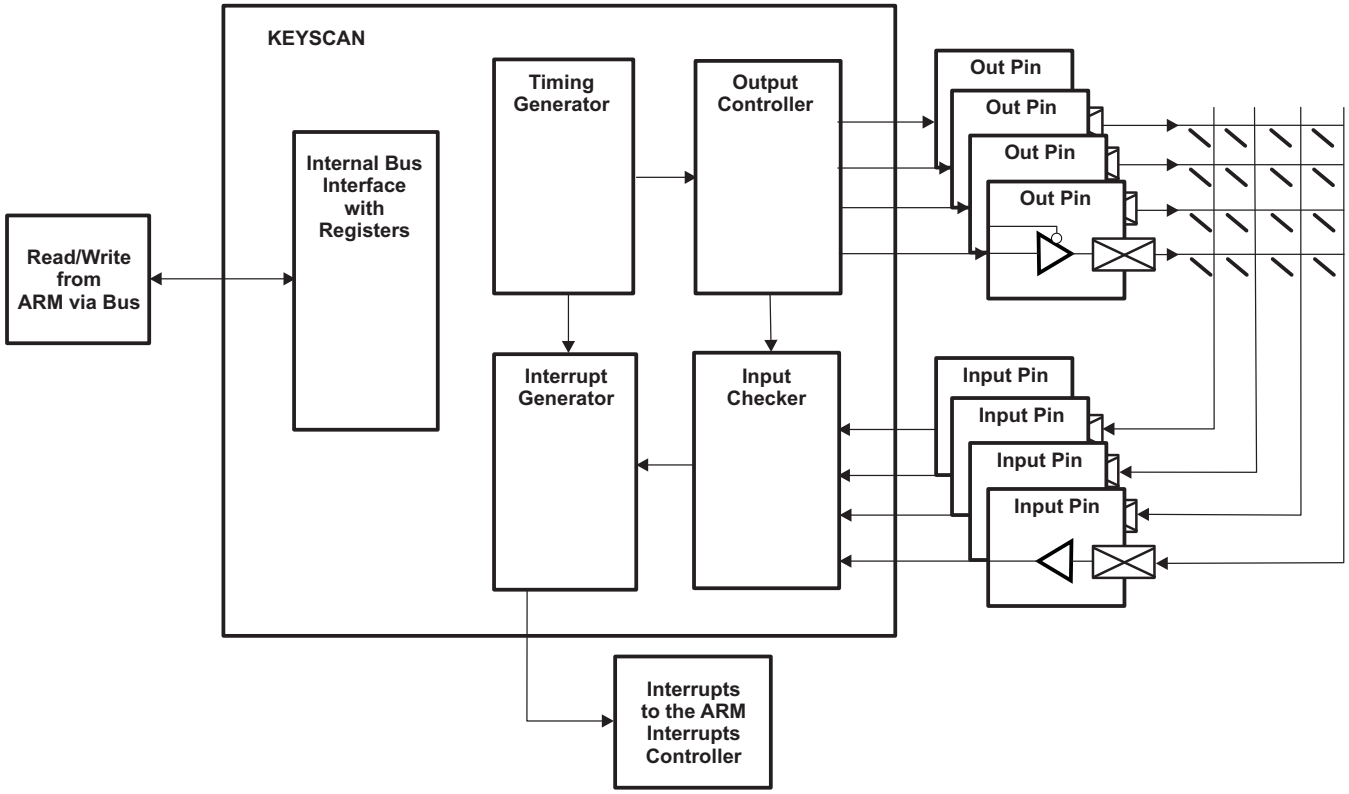
The DM36x key scan module supports two types of key matrices — 4x4 and 5x3 key scan functions. It also supports the following features:

- Two scan modes
  - Channel interval mode
  - Scan interval mode
- Programmable key scan time
  - Strobe time
  - Interval time
- Two input detection modes
  - Direct mode
  - 3-data check mode
- Generates an interrupt to detect
  - Key input changes
  - Periodic time intervals after a key is pressed

1.1 Block Diagram

Figure 1 shows the key scan block diagram.

Figure 1. Key Scan Block Diagram



1.2 Industry Compliance Statement

The key scan module does not conform to any recognized industry standards.

2 Peripheral Architecture

2.1 Clock Control

The key scan module can operate from two clock sources. Clock source selection is based on the programing of the KEYSCLKS bit of the PERI_CLKCTL register. For more information on device clocking, refer to the *TMS320DM36x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

2.2 Signal Descriptions

The key scan module generates signals on eight separate pins: KEYA[3:0] and KEYB[3:0]. The key scan signal descriptions are shown in Table 1. Refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) Data Manual* (SPRS457) for more information on these pins.

Table 1. Key Scan Output Types

Signal name	Signal Type	Function
KEYA0	Input	Key scan Input Signal: A0
KEYA1	Input	Key scan Input Signal: A1
KEYA2	Input	Key scan Input Signal: A2
KEYA3	Input	Key scan Input Signal: A3
KEYB0	Output	Key scan Output Signal: B0
KEYB1	Output	Key scan Output Signal: B1

Table 1. Key Scan Output Types (continued)

Signal name	Signal Type	Function
KEYB2	Output	Key scan Output Signal: B2
KEYB3	Input/Output	Key scan Input/Output Signal: B3

2.3 Key Scan Functional Operation

2.3.1 Key Scan Operation: Output Type

The key scan module produces two types of output: Always Out and Active Low. Always Out uses a diode for each switch on the multi-on switch. Since these pins are In/Out pins for the whole device, it needs pull-up for the Active Low output.

Table 2. Key Scan Output Types

Output Type	Output pin Condition	Pin Buffer		Comments
		Output Enable	Output Data	
Always out	Scan active	Enable	Low	
	Scan inactive	Enable	High	
Active low	Scan active	Enable	Low	
	Scan inactive	Disable	Hi-Z	Need pull-up for input buffer

2.3.2 Key Scan Operation: Matrix Types

The key scan module supports the following 4x4 or 5x3 configurations, as shown in Figure 2 and Figure 3.

Figure 2. Key Scan External Circuit Diagram (4x4)

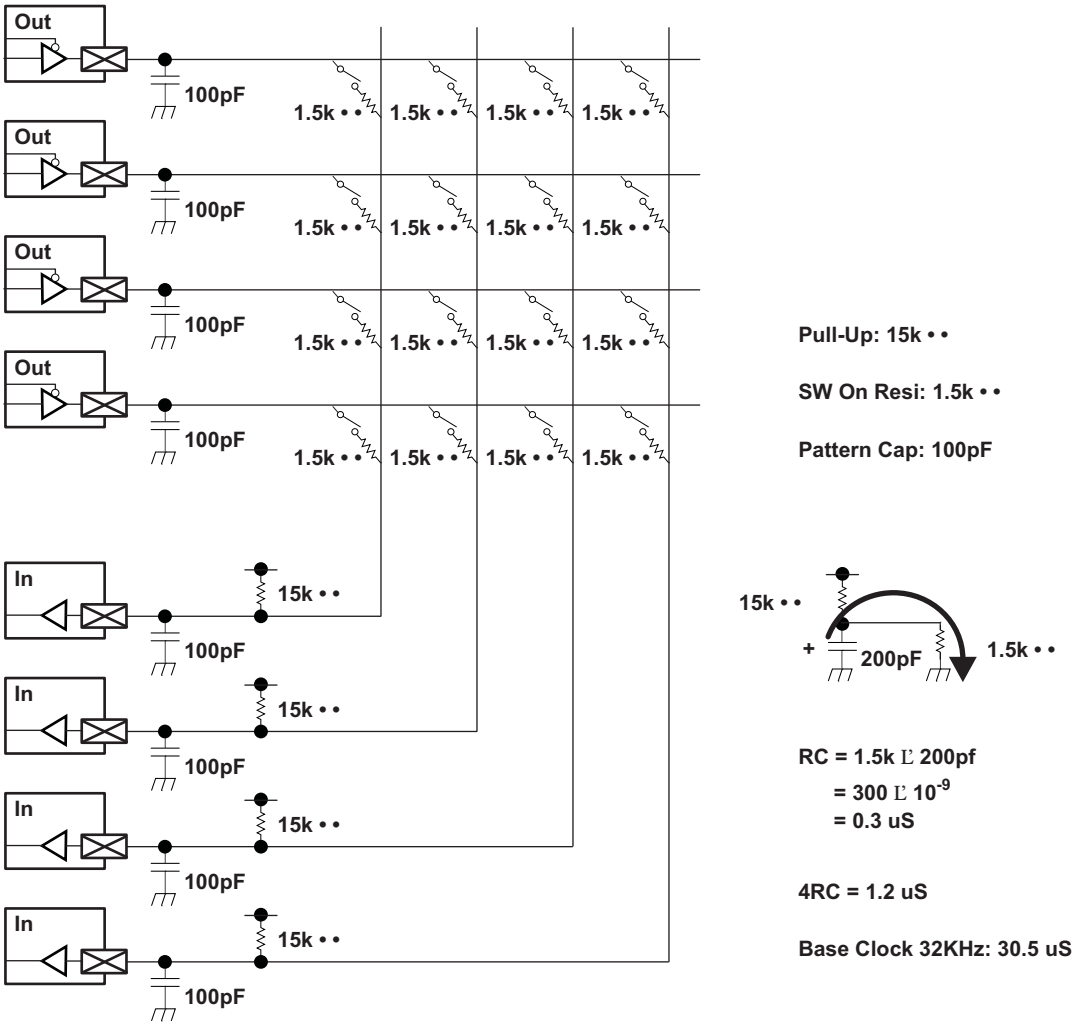
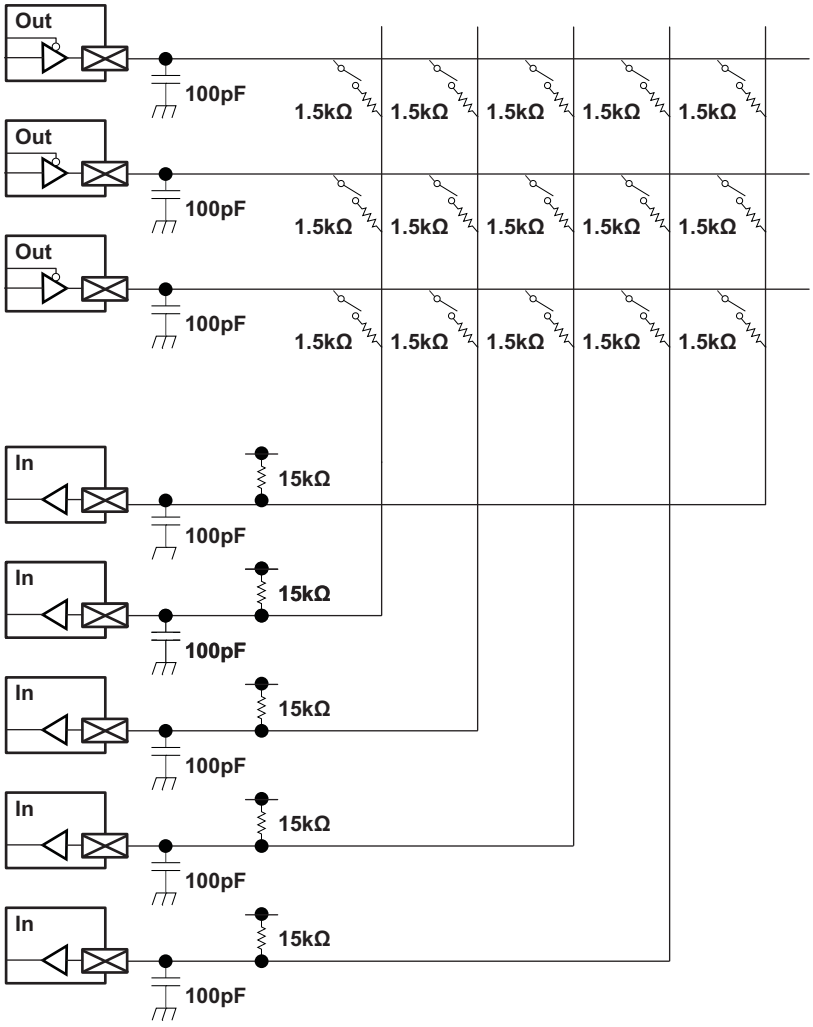


Figure 3. Key Scan External Circuit Diagram (5x3)



2.3.3 Key Scan Operation: Scan Mode

This module supports two types of scan modes: scan interval mode and channel interval mode. Each mode has the capacity to be run with 4x4 or 5x3 configurations.

- Scan interval mode: This mode contains the interval time for each scan strobe access. Scan interval mode for 4x4 is shown in Figure 4, and for 5x3 it is shown in Figure 5.
- Channel interval mode: This mode contains the interval time for each channel strobe access. Channel interval mode for 4x4 is shown in Figure 6, and for 5x3 it is shown in Figure 7.

Figure 4. Scan Interval at 4x4 Mode

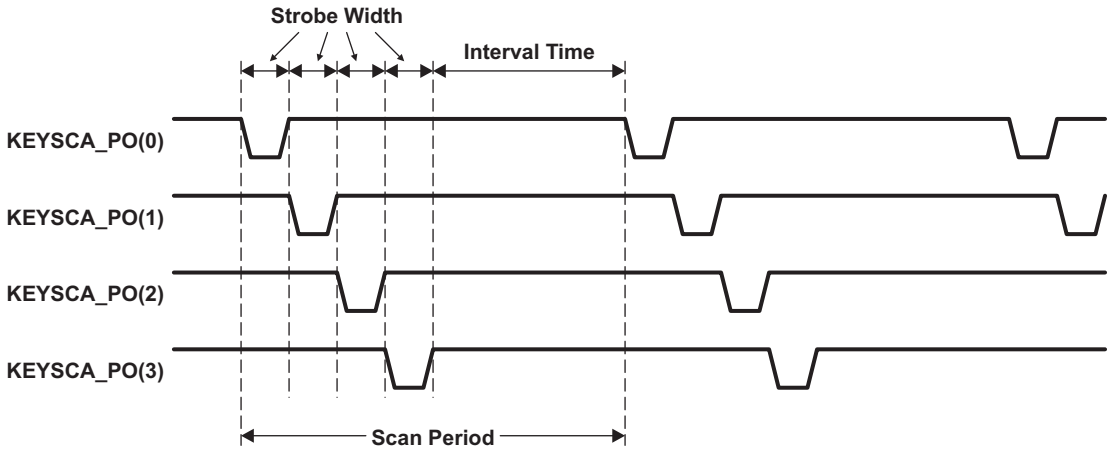


Figure 5. Scan Interval Mode at 5x3

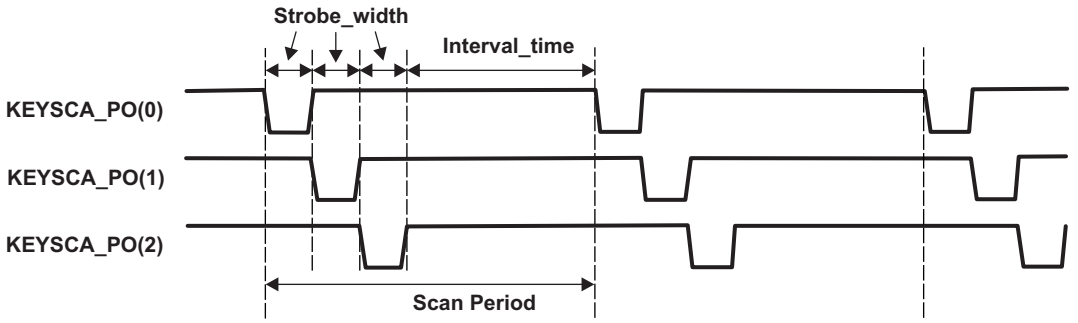


Figure 6. Channel Interval at 4x4 Mode

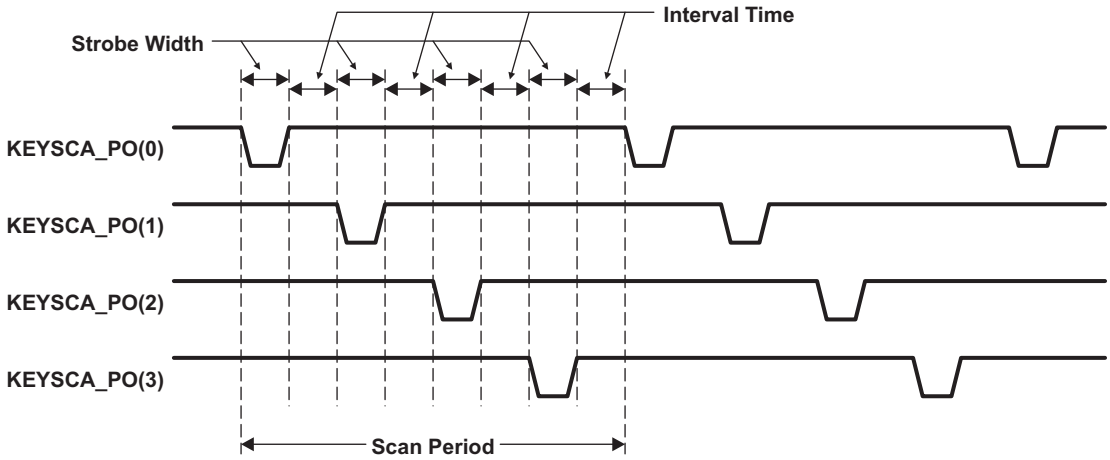
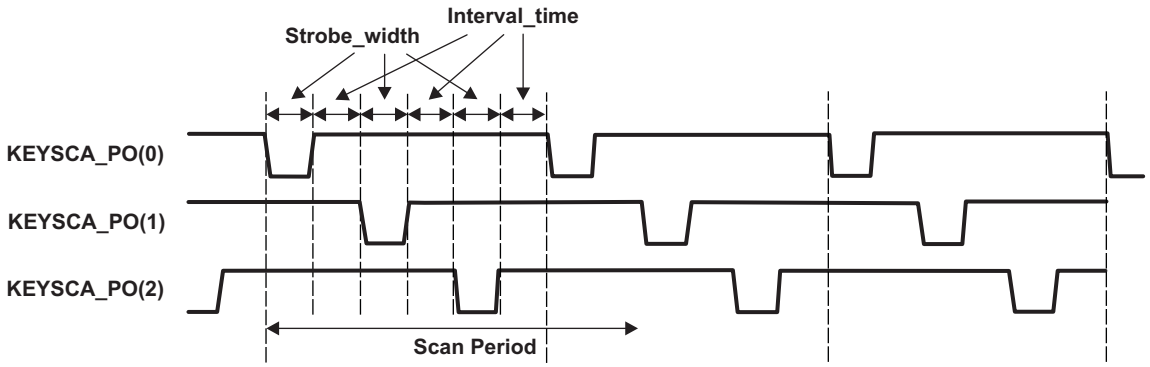


Figure 7. Channel Interval Mode at 5x3



2.3.4 Key Scan Operation: Scan Period

The scan period for both scan modes is determined by the strobe width value (STWIDTH) in the strobe width register (STBRWIDTH), and the interval width value (INTERVAL) in the interval time register (INTERVALTIME).

For 4x4 key scan function, the scan period is (4 x (STWIDTH + 1) + INTERVAL) x peripheral clock period.

For 5x3 key scan function, the scan period is (3 x (STWIDTH + 1) + INTERVAL) x peripheral clock period.

2.4 Input Mode and Anti-Chattering

There are two input method types:

- Direct Input: Inputs the data value directly
- 3-Data Input: Prevents anti-chattering because it will scan the key three times before update.

Figure 8. Key Scan Input Data Function

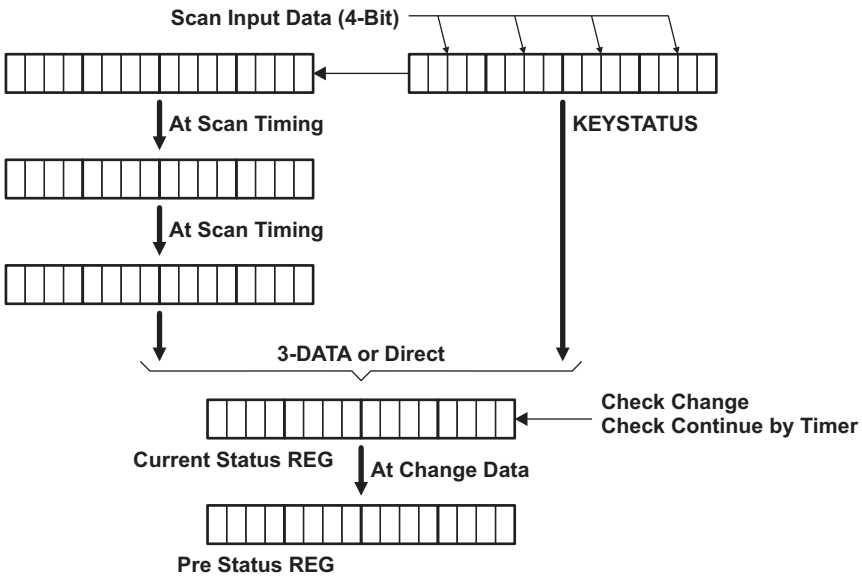


Figure 9. Key Scan Operation for Chattering-1

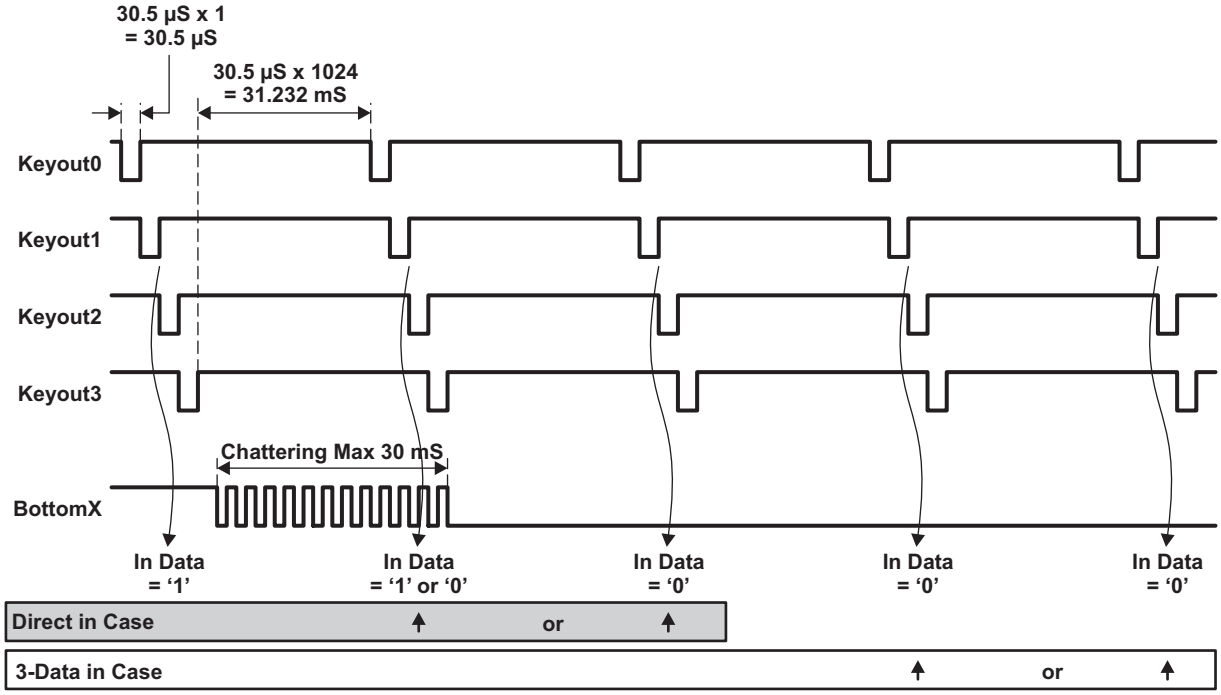
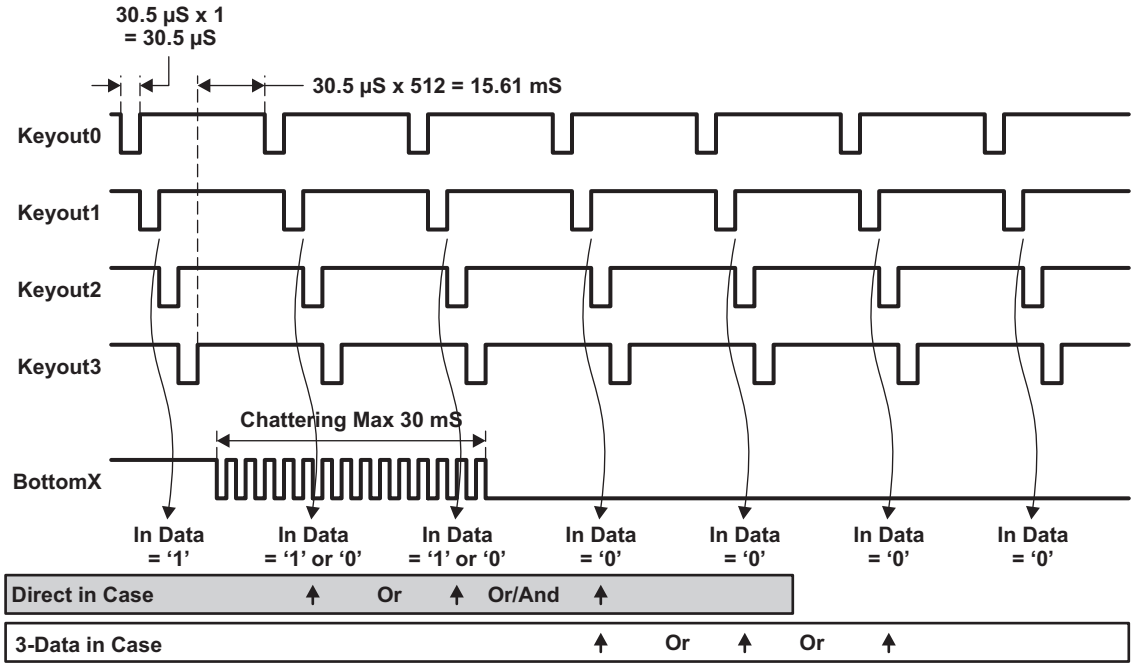


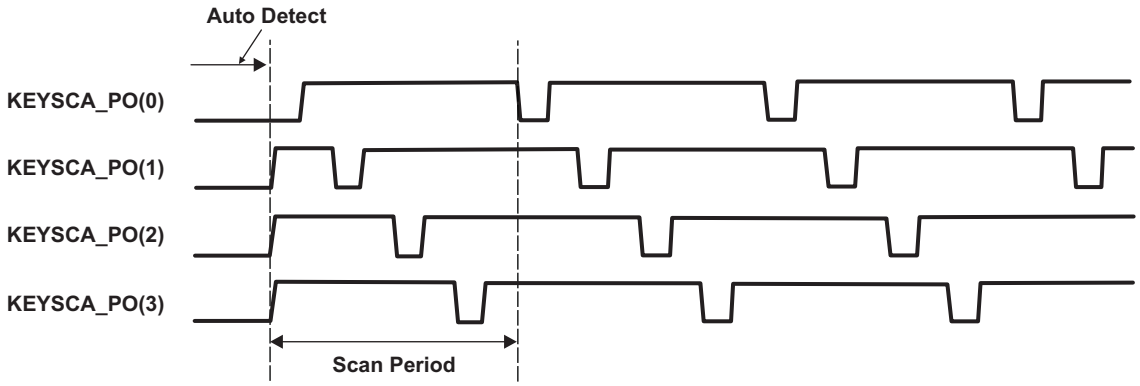
Figure 10. Key Scan Operation for Chattering-2



2.5 Auto Detect Function

After the auto detect mode detects that a key has been pressed, it immediately begins scanning. Normally, the anti-chatter function is ON. That means, if a key is pressed, auto detect mode (all outputs are low) occurs and continues for a clock count during scanning, until the key pressing is recognized for the third time. When setting this mode, make sure that Enable is turned off.

Figure 11. Auto Detect Mode at 4x4



2.6 Software and Hardware Reset Considerations

A software reset (such as a reset generated by the emulator) causes the key scan registers to return to their default state after reset.

A hardware reset of the processor causes the key scan registers to return to their default values after reset.

2.7 Initialization

The following section provides procedures for initializing the key scan in 4x4 mode or 5x3 mode.

- Turn on the lpsc module.
- Initialize the pinmux register.
- Initialize the strobe width (STRBWIDTH), interval time (INTERVALTIME) registers.
- Initialize the key control register according to requirements.
  The following settings are available inside the key control register:
  - Module enable/disable
  - Auto detect mode enable/disable (when this mode is enabled make sure that the module is disabled)
  - Keyboard type (4x4 or 5x3)
  - Scan mode and output type (as explained in Section 2.3)
  - Update method
- Enable the required interrupts in the INTENA register.
- In polling mode, poll the INTFLG status register to determine which kinds of events you want to occur or not occur. Polling can be done without enabling the interrupts.
- After the interrupt occurs or a particular status register is set, read the CURRENTST register to detect which key is pressed.
- Clear the interrupt using the INTCLR register.

2.8 Interrupt Support

2.8.1 Interrupt Events and Requests

The key scan module has a single interrupt signal to the arm interrupt controller (AINTC).

- Key scan generates an interrupt to the CPU if any changes are found in any key status. The status of this interrupt is reflected in the key data change interrupt flag bit (CHNGFLG) in the interrupt flag control register (INTFLG). The CHNGFLG bit is cleared by writing a 1 to the key data change interrupt flag clear bit (CHNGCLR) in the interrupt clear control register (INTCLR).

- After a key is pressed, key scan starts counting up from 0 to the set value configured in intervals of the timer interrupt flag output set bit (CONTITIMER) in the continuous timer (CONTITIME) register. When the value reaches a set value, key scan generates interrupts at regular time intervals. The status of this interrupt is reflected in the continuous interrupt flag bit (CONTIFLG) in the interrupt flag control (INTFLG) register. When key scan recognizes that a key has been released, the count value returns to 0. The CONTIFLG bit is cleared by writing a 1 to the continuous interrupt flag clear bit (CONTICLR) in the interrupt clear control (INTCLR) register .

2.8.2 Interrupt Multiplexing

The key scan interrupt is not multiplexed with any other interrupts. Refer to the *TMS320DM36x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5) for more information on the system control module and ARM Interrupt controller

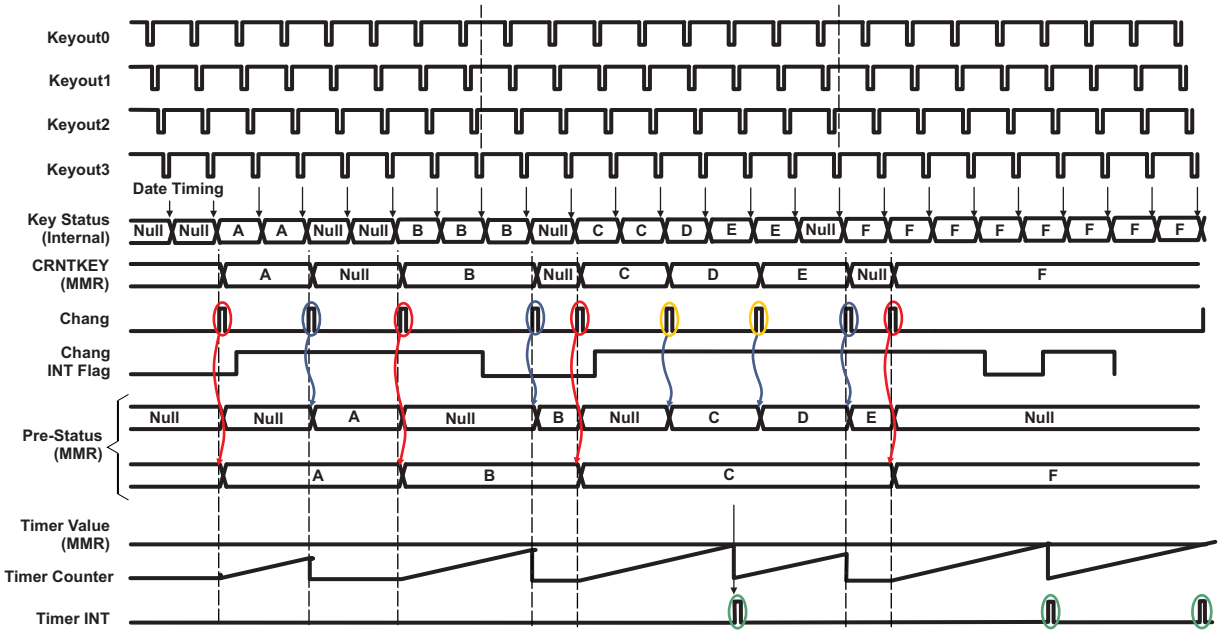
2.8.3 Key Scan Previous Status Register Update Method and Interrupt Generation

The input data is changed at scan time with the input method types discussed in Section 2.4. You can read this value with the key scan current status (CURRENTST) register. The key scan previous status (PREVIOUSST) register keeps the existing value prior to the input data.

There are two types of update methods for this register; both can be selected by key scan control (KEYCTRL) register.

- Previous mode. The PREVIOUSST register will always keep the data from the key that was previously pressed. This register will update when the CURRENTST register is changed.
- First-Switch mode. The PREVIOUSST register will update only when the CURRENTST register updates the date from the no-switch condition (NULL) as shown in Figure 12.

Figure 12. Key Scan Interrupt and Pre-Status



Red shows the interrupt generated when the UPDATE method is in first-switch mode.
Blue shows the interrupt generated when the UPDATE method is in previous mode.
Yellow shows the interrupt generated only when the UPDATE method is in previous mode; this is a special case where there is no occurrence of a NULL condition between a two-switch press. This kind of interrupt will not generate when we operate the key scan module in first-switch mode.
Green indicates when the continuous timer interrupts will be generated.

2.9 EDMA Event Support

The key scan module does not generate any EDMA events.

2.10 Power Management

The key scan peripheral can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the key scan peripheral is controlled by the Power and Sleep Controller (PSC) processor. The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM36x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5)

2.11 Emulation Considerations

The key scan peripheral supports emulation suspend. The response of the key scan events to emulation suspend events (such as halts and breakpoints) is controlled by the FREE bit in the emulation control (EMUCTRL) register. Key scan either stops exchanging data after a scan period (FREE = 0) or continues to run (FREE = 1) when an emulation suspend event occurs. For more information, see the description of the FREE bit in Section 3.10 .

3 Registers

Table 3 lists the memory-mapped registers for the key scan controller. See the device-specific data manual for the memory address of these registers

Table 3. Key Scan Memory Map Registers

Offset	Register	Description	Location
0x0	KEYCTRL	Key Control Register	Section 3.1
0x4	INTCENA	Interrupt Enable Control Register	Section 3.2
0x8	INTFLG	Interrupt Flag Control Register	Section 3.3
0xC	INTCLR	Interrupt Clear Control Register	Section 3.4
0x10	STRBWIDTH	Strobe Width Register	Section 3.5
0x14	INTERVALTIME	Interval Time Register	Section 3.6
0x18	CONTITIME	Continuous Timer Register	Section 3.7
0x1C	CURRENTST	Key Scan Current Status Register	Section 3.8
0x20	PREVIOUSST	Key Scan Previous Status Register	Section 3.9
0x24	EMUCTRL	Emulation Control Register	Section 3.10

3.1 Key Scan Control (KEYCTRL) Register

The key scan control (KEYCTRL) register is shown in Figure 13 and described in Table 4.

Figure 13. Key Scan Control (KEYCTRL) Register

31							8
Reserved							
R-0							

7	6	5	4	3	2	1	0
Reserved	MODE	OUTPUTTYPE	SCANMODE	AUTODET	CHATOFF	PREVMODE	KEYEN
R-0	R/C-0	R/W-0	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4. Key Scan Control (KEYCTRL) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6	MODE		Key matrix type
		0	4x4 matrix type
		1	5x3 matrix type
5	OUTPUTTYPE		Output type
		0	Active low type
		1	Always out type
4	SCANMODE		Scan mode select bit
		0	Scan interval mode
		1	Channel interval mode
3	AUTODET		Automatic key detection function select bit
		0	Automatic key function is OFF
		1	Automatic key function is ON
2	CHATOFF		Anti-chatter function select bit
		0	Anti-chatter function is ON
		1	Anti-chatter function is OFF
1	PREVMODE		Previous status update mode select bit
		0	Previous mode
		1	First bottom mode
0	KEYEN		Module enable
		0	Disable key detection
		1	Enable key detection

3.2 Interrupt Enable Control (INTCENA) Register

The interrupt enable control (INTCENA) register is shown in Figure 14 and described in Table 5.

Figure 14. Interrupt Enable Control (INTCENA) Register

31	4	3	2	1	0
Reserved		CONTIENA	OFFENA	ONENA	CHNGENA
R-0		R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5. Interrupt Enable Control (INTCENA) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3	CONTIENA		Continuous Interrupt Enable
		0	Disable
		1	Enable
2	OFFENA		Key Data All Off Interrupt Enable
		0	Disable
		1	Enable
1	ONENA		Key Data On Interrupt Enable
		0	Disable
		1	Enable
0	CHNGENA		Key Data Change Interrupt Enable
		0	Disable
		1	Enable

3.3 Interrupt Flag Control (INTFLG) Register

The interrupt flag control (INTFLG) register is shown in Figure 15 and described in Table 6.

Figure 15. Interrupt Flag Control (INTFLG) Register

31 4	3	2	1	0
Reserved	CONTIFLG	OFFFLG	ONFLG	CHNGFLG
R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. Interrupt Flag Control (INTFLG) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3	CONTIFLG		Continuous Interrupt Flag
		0	No interrupt
		1	Interrupt
2	OFFFLG		Key Data All Off Interrupt Flag
		0	No interrupt
		1	Interrupt
1	ONFLG		Key Data On Interrupt Flag
		0	No interrupt
		1	Interrupt
0	CHNGFLG		Key Data Change Interrupt Flag
		0	No interrupt
		1	Interrupt

3.4 Interrupt Clear Control (INTCLR) Register

The interrupt clear control (INTCLR) register is shown in Figure 16 and described in Table 7.

Figure 16. Interrupt Clear Control (INTCLR) Register

31	4	3	2	1	0
Reserved		CONTICLR	OFFCLR	ONCLR	CHNGCLR
R-0		C-0	C-0	C-0	C-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. Interrupt Clear Control (INTCLR) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3	CONTICLR		Continuous Interrupt Flag Clear
		1	Clear Interrupt Flag
2	OFFCLR		Key Data All Off Interrupt Flag Clear
		1	Clear Interrupt Flag
1	ONCLR		Key Data On Interrupt Flag Clear
		1	Clear Interrupt Flag
0	CHNGCLR		Key Data Change Interrupt Flag Clear
		1	Clear Interrupt Flag

3.5 Strobe Width (STRBWIDTH) Register

The strobe width (STRBWIDTH) register is shown in Figure 17 and described in Table 8.

Figure 17. Strobe Width (STRBWIDTH) Register

31	8	7	0
Reserved		STWIDTH	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. Strobe Width (STRBWIDTH) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	STWIDTH	0-FFh	Strobe width set bit. The strobe width is: Peripheral Clock period x (STWIDTH + 1)

3.6 Interval Time (INTERVALTIME) Register

The interval time (INTERVALTIME) register is shown in Figure 18 and described in Table 9.

Figure 18. Interval Time (INTERVALTIME) Register

31	8	7	0
Reserved		INTERVAL	
R-0		R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. Interval Time (INTERVALTIME) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	INTERVAL		Interval width set bit The Interval width is: Peripheral Clock period x INTERVAL
		00000000	256
		00000001	512
		00000010	768
		:	:
		11111111	65556

3.7 Continuous Time (CONTITIME) Register

The continuous time (CONTITIME) register is shown in Figure 19 and descried in Table 10.

Figure 19. Continuous Time (CONTITIME) Register

31	8	7	0
Reserved		CONTTIMER	
R-0		R/W-8	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. Continuous Time (CONTITIME) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	CONTTIMER		Interval of the Timer Interrupt flag output set bit. An interrupt is generated at each time of: Peripheral Clock period x CONTITIMER
		00000000	8192
		00000001	16384
		00000010	24576
		:	:
		11111111	2097152

3.8 Key Scan Current Status (CURRENTST) Register

The key scan current status (CURRENTST) register is shown in Figure 20 and described in Table 11.

Figure 20. Key Scan Current Status (CURRENTST) Register

31															16
Reserved															
R-0															
15															0
CURST[15:0]															
R-0xFFFF															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. Key Scan Current Status (CURRENTST) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	CURST[15:0]		Current key status
		0	Key on
		1	Key off

3.9 Key Scan Previous Status (PREVIOUSST) Register

The key scan previous status (PREVIOUSST) register is shown in Figure 21 and described in Table 12.

Figure 21. Key Scan Previous Status (PREVIOUSST) Register

31															16
Reserved															
R-0															
15															0
PREST[15:0]															
R-0xFFFF															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. Key Scan Previous Status (PREVIOUSST) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	PREST[15:0]		Previous key status bit
		0	Key on
		1	Key off

3.10 Emulation Control (EMUCTRL) Register

The emulation control (EMUCTRL) register is shown in Figure 22 and described in Table 13.

Figure 22. Emulation Control (EMUCTRL) Register

31	3	2	1	0
Reserved		RT_SEL	SOFT	FREERUN
R-0		R-1	R-0	R-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 13. Emulation Control (EMUCTRL) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	RT_SEL		Support only emulation suspend
1	SOFT		Key scan supports only soft stop
		1	Soft stop: Stop peripheral related operations gracefully at the earliest opportunity after the current application specific processing task is completed.
0	FREERUN		Emulation free bit. This bit controls whether or not the key scan will respond to the emulation suspend signal that it has been programmed to monitor
		0	Free-running mode is disabled. During emulation halt, Key scan Stop peripheral related operations gracefully at the earliest opportunity after the current application specific processing task is completed.
		1	Free-running mode is enabled. During emulation halt, the Key scan module continues to operate.

4 Revision History

This document has been revised to include the following technical change(s).

Table 14. Revisions

Location	Additions/Deletions/Edits
Figure 2	Changed figure.
Figure 3	Changed figure.

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