User's Guide

Migration Between TMS320F2837x/2807x and TMS320F28P65x

ABSTRACT

This migration guide describes the hardware and software differences to consider when moving between F2837x/F2807x and F28P65x C2000™ MCUs. This document shows the block diagram between the two MCUs as a visual representation on what blocks are similar or different. It also highlights the features that are unique between the two devices for all available packages in device comparison table. To facilitate application and hardware migration between F2837x and F28P65x devices, the PCB hardware section provides guidance on how to proceed with the common 176-pin package. A supplemental topic was included with recommendations for designing a 100-pin hardware that works for both F2837x and F28P65x 100-pin devices for early development of F28P65x application using F2837x 100-pin device. The digital general-purpose input/output (GPIO) and analog multiplex comparison tables show pin functionality between the two MCUs. F2807x is a single CPU, 120MHz variant of F2837x with only the 176-pin and 100-pin packages availble. The device comparison table only compares the superset F2837x device that has the complete set of peripherals and pins. Consult the F2807x datasheet for the more information on the available peripherals and pins if this will be used in migration. This serves as a reference for hardware design and signal routing when considering a move between the two devices. Lastly, the F28P65x software support is only in EABI format. The EABI migration is discussed in Section 5.

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1 Feature Differences Between F2837x and F28P65x

The 176-pin and 100-pin are the common packages between F2837x, F2807x and F28P65x. It is possible to migrate between F2837x, F2807x and F28P65x 176-pin with the caveats in this document taken into account. A supplemental section has been added with recommendations for a PCB design to accommodate 100-pin devices for F2837x and F28P65x, to account for application development using F28P65x with F2837x device. The recommendations cover F2837x but same recommendations apply to F2807x. Consult F2807x datasheet for more details on peripherals and pins that are available.

Note

This comparison guide focuses on the superset devices: F28387 and F28P65X. Other part numbers in this product family have reduced feature support. For details specific to part numbers, see the device-specific data sheet.

1.1 F2837x and F28P65x Feature Comparison

An overlaid block diagram of F2837x and F28P65x is shown in Figure 1-1 while feature comparison of the superset part numbers for the F2837x and F28P65x devices is shown in Table 1-1.

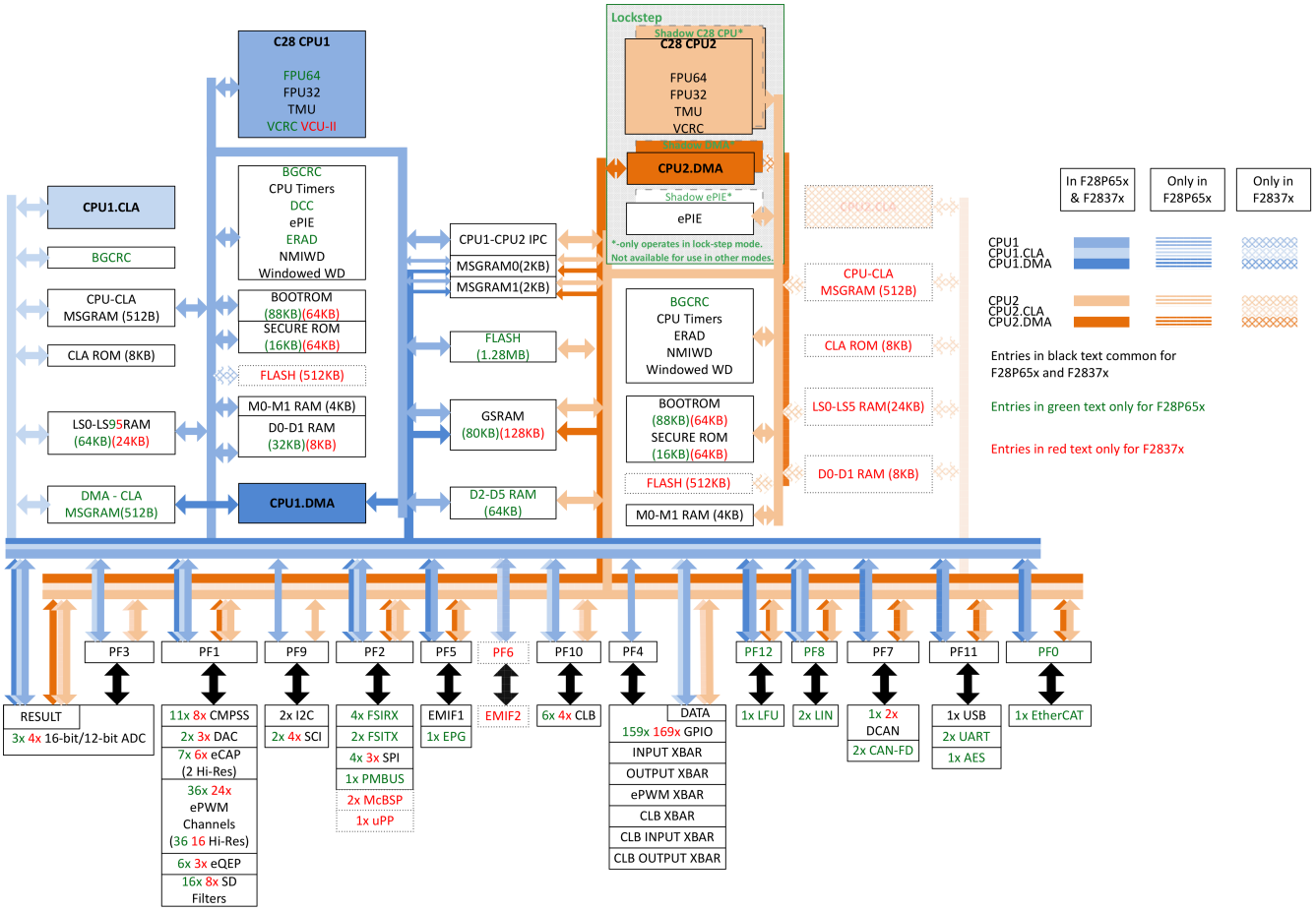


Figure 1-1. F2837x and F28P65x Overlaid Functional Block Diagram

Table 1-1. F2837x and F28P65x Superset Device Comparison

FEATURE		F2837x			F28P65x			
		100-Pin PZ	176-Pin PTP	337-Ball ZWT	100-Pin PZP	176-Pin PTP	169-Ball NMR	256-Ball ZEJ
C28x Subsystem								
C28x	Number	2			2			
	Frequency (MHz)	200			200			
	32-bit and 64-bit Floating-Point Unit (FPU)	Yes			Yes			
	VCRC	–			Yes			
	VCU-II	Yes			–			
	TMU - Type 0	Yes			Yes			
	C28x Lockstep (LCM)	–			Yes			
CLA	Number	2 - Type 1			1 - Type 2			
	Frequency (MHz)	200			200			
C28x Flash		1MB (512KW)			1.28MB(640KW)			
C28x RAM	Dedicated RAM	24KB (12KW)			104KB (52KW)			
	Local Shared RAM	48KB (24KW)			64KB (32KW)			
	Global Shared RAM	128KB(64KW)			80KB (40KW)			
	Total RAM	200KB(100KW)			248KB (124KW)			
Background Cyclic Redundancy Check (BGCRC) module		–			3 (1 per CPU and CLA)			
Configurable Logic Block (CLB)		8 tiles			6 tiles			
32-bit CPU Timers		6 (3 per CPU)			6 (3 per CPU)			
6-Channel DMA - Type 0		2 (1 per CPU)			2 (1 per CPU)			
Dual-zone Code Security Module (DCSM) for on-chip flash and RAM		Yes			Yes			
Advanced Encryption Standard (AES) Accelerator		–			Yes			
Embedded Real-time Analysis and Diagnostic (ERAD)		–			Yes			
EMIF	EMIF1 (16-bit or 32-bit)	1			–	1		
	EMIF2 (16-bit)	–		1	–			
External Interrupts		5			5			
Message RAM	C28x CPU1, C28x CPU2	4KB (2KW)			4KB (2KW)			
	C28x CPUs and CLAs	1KB (0.5KW)			0.5KB (0.25KW)			
	DMAs and CLAs	1KB (0.5KW)			0.5KB (0.25KW)			
Non-maskable Interrupt Watchdog (NMIWD) timers		2 (1 per CPU)			2 (1 per CPU)			
Watchdog (WD) timers		2 (1 per CPU)			2 (1 per CPU)			
Pins and Power Supply								
Internal 3.3v to 1.2v Voltage Regulator		Yes			Yes			
GPIO	I/O Pins (shared by CPU1, CPU2 and CM for 2838x)	41	97	169	49	96	108	163
	Input XBAR	Yes			Yes			
	Output XBAR	Yes			Yes			
AIO (analog with digital inputs)		–			13	14	13	18
AGPIO (analog with digital inputs and outputs)		–			11	22	21	22

Table 1-1. F2837x and F28P65x Superset Device Comparison (continued)

FEATURE		F2837x			F28P65x			
		100-Pin PZ	176-Pin PTP	337-Ball ZWT	100-Pin PZP	176-Pin PTP	169-Ball NMR	256-Ball ZEJ
C28x Analog peripherals								
Analog-to-Digital Converter (ADC) (configurable to 12-bit or 16-bit)		4 - Core: Type 4; Wrapper: Type 3			3 - Core: Type 4; Wrapper: Type 4			
ADC 16-bit mode	MSPS	1.1			1.1			
	Conversion Time (ns)	915			915			
ADC 12-bit mode	MSPS	3.5			3.5			
	Conversion Time (ns)	280			280			
ADC Input channels (single-ended mode)		14	20	24	24	36	34	40
ADC Input channels (differential mode)		–	9	12	11	18	17	19
Temperature Sensor		1			1			
Comparator subsystem (CMPSS) (each CMPSS has two comparators and two internal DACs)		8			11			
Buffered Digital-to-Analog Converter (DAC)		3			2			
C28x Control Peripherals								
eCAP/HRCAP	Total inputs	6 - Type 0			7 - Type 3			
	Channels with high-resolution capability	2 (eCAP5 and eCAP6)			2 (eCAP6 and eCAP7)			
ePWM/HRPWM	Total channels	24 - Type 4			36 - Type 5			
	Channels with high-resolution capability	16 (ePWM1-ePWM8)			36 (ePWM1-ePWM18)			
ePWM XBAR		Yes			Yes			
eQEP modules		3 - Type 0			6 - Type 2			
SDFM channels		8 - Type 0			16 - Type 2			
C28x Communications Peripherals								
Fast Serial Interface (FSI) RX		–			4 - Type 2			
Fast Serial Interface (FSI) TX		–			2 - Type 2			
Inter-Integrated Circuit (I2C)		2 - Type 0			2 - Type 1			
Multi-channel Buffered Serial Port (McBSP) - Type 1		2			–			
Power Management Bus (PMBus) - Type 0		–			1			
Local Interconnect Network (LIN) - Type 1		–			2			
Serial Communications Interface (SCI) - Type 0 (UART-compatible)		4			2			
Serial Peripheral Interface (SPI) - Type 2		2			4			
Controller Area Network (CAN) 2.0B - Type 0		2			1			
CAN with Flexible Data-Rate (CAN-FD)		–			2 - Type 2			
Ethernet for Control Automation Technology (EtherCAT)		–			–	1		
Universal Asynchronous Receiver-Transmitter (UART)		–			2			
Universal Serial Bus (USB) - Type 0		1			1			
Temperature and Qualification								
Junction Temperature ($TJ_$)		–40°C to 150°C						

Table 1-1. F2837x and F28P65x Superset Device Comparison (continued)

FEATURE	F2837x			F28P65x			
	100-Pin PZ	176-Pin PTP	337-Ball ZWT	100-Pin PZP	176-Pin PTP	169-Ball NMR	256-Ball ZEJ
Free-Air Temperature ($TA_)$	–40°C to 125°C						
Package Options with AEC-Q100 Qualification available	No	Yes	Yes	Yes	Yes	No	Yes

2 PCB Hardware Changes

The common packages between F2837x and F28P65x devices are 176-Pin PTP and 100-Pin PZ. It is possible to drop-in a 176-pin F28P65x device on an existing F2837x application board and this section covers how to go about such migration and other considerations for pin assignments that have changed. The drop-in migration is covered in Section 2.2.

A supplemental topic has been added to this section about designing a common 176-Pin and 100-Pin board to accommodate both F2837x and F28P65x device for early development with F2837x that would eventually be replaced with F28P65x part. This topic is covered in Section 2.3 and Section 2.4, respectively.

In some cases, an existing application on the superset F2837x 337-BGA ZWT package might be moving to either the F28P65x 256-BGA ZEJ or 169-BGA NMR package. Section 2.5 provides some guidelines when considering F28P65x BGA devices.

Note

Overall compatibility depends on more than just the pins. Please review all the changes in this document during the migration process.

2.1 PCB Hardware Changes for the 176-Pin PTP and 100-Pin PZP Package

This section describes the F2837x and F28P65x pin differences and similarities that exist in the 176-Pin PTP and 100-pin PZ packages. Figure 2-1 and Figure 2-2 are the overlay diagrams between F2837x and F28P65x that categorize compatibility of the 176 and 100-pin devices.

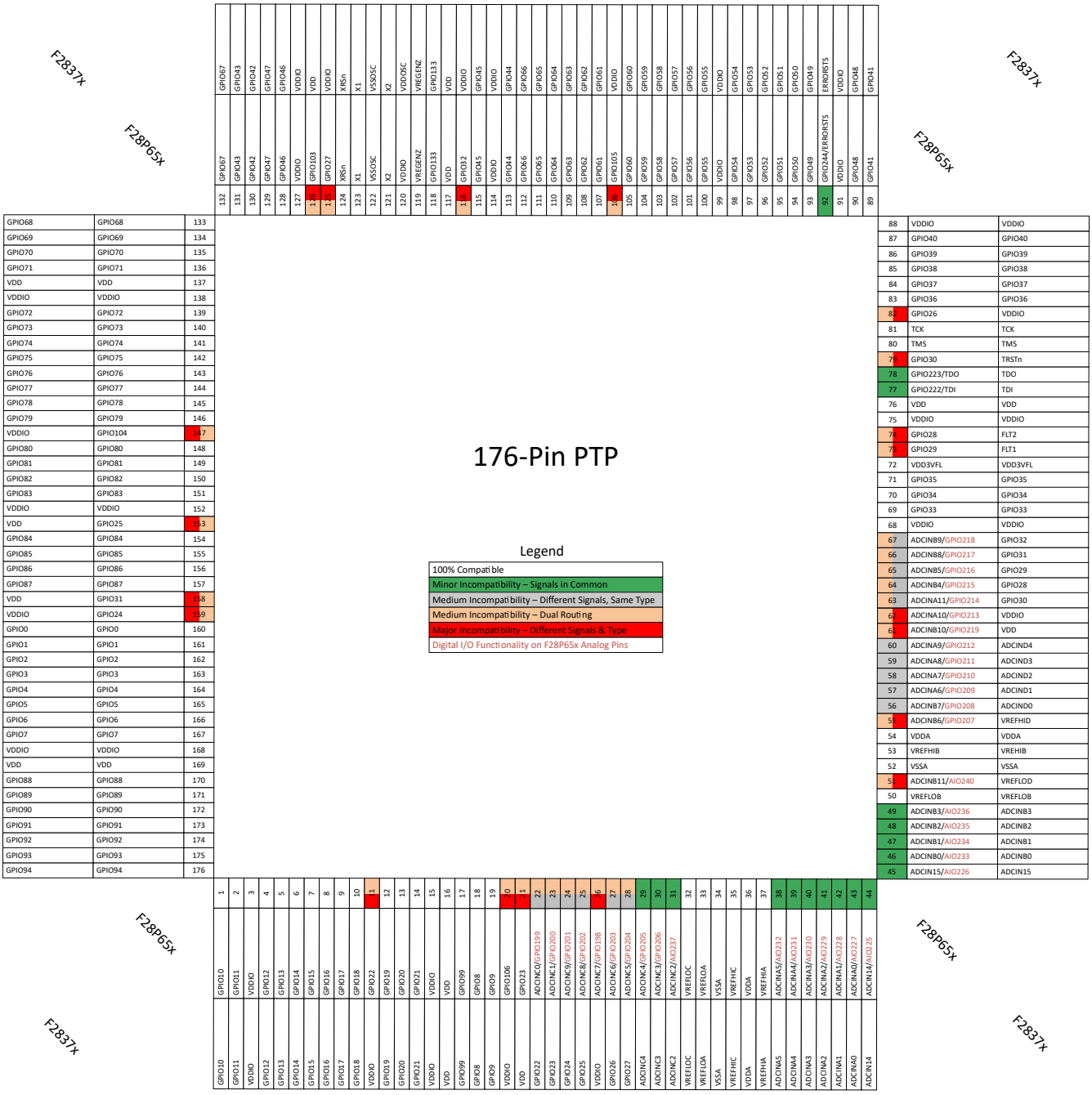
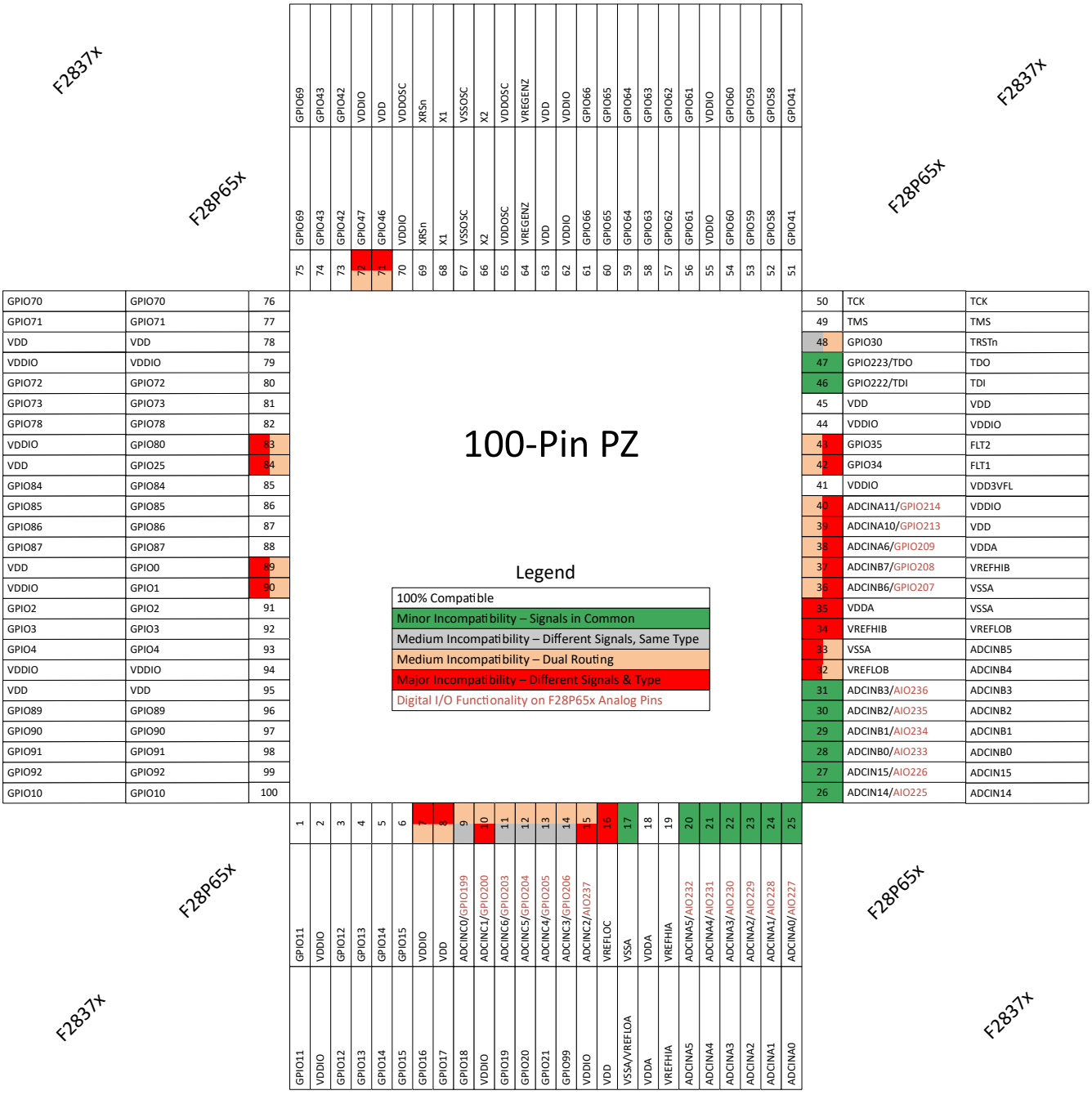


Figure 2-1. F2837x and F28P65x 176-Pin Overlay



GPIO70	GPIO70	76
GPIO71	GPIO71	77
VDD	VDD	78
VDDIO	VDDIO	79
GPIO72	GPIO72	80
GPIO73	GPIO73	81
GPIO78	GPIO78	82
VDDIO	GPIO80	83
VDD	GPIO25	84
GPIO84	GPIO84	85
GPIO85	GPIO85	86
GPIO86	GPIO86	87
GPIO87	GPIO87	88
VDD	GPIO0	89
VDDIO	GPIO1	90
GPIO2	GPIO2	91
GPIO3	GPIO3	92
GPIO4	GPIO4	93
VDDIO	VDDIO	94
VDD	VDD	95
GPIO89	GPIO89	96
GPIO90	GPIO90	97
GPIO91	GPIO91	98
GPIO92	GPIO92	99
GPIO10	GPIO10	100

50	TCK	TCK
49	TMS	TMS
48	GPIO30	TRSTn
47	GPIO223/TDO	TDO
46	GPIO222/TDI	TDI
45	VDD	VDD
44	VDDIO	VDDIO
43	GPIO35	FLT2
42	GPIO34	FLT1
41	VDDIO	VDD3VFL
40	ADCINA11/GPIO214	VDDIO
39	ADCINA10/GPIO213	VDD
38	ADCINA6/GPIO209	VDDA
37	ADCINB7/GPIO208	VREFHIB
36	ADCINB6/GPIO207	VSSA
35	VDDA	VSSA
34	VREFHIB	VREFLOB
33	VSSA	ADCINB5
32	VREFLOB	ADCINB4
31	ADCINB3/AIO236	ADCINB3
30	ADCINB2/AIO235	ADCINB2
29	ADCINB1/AIO234	ADCINB1
28	ADCINB0/AIO233	ADCINB0
27	ADCIN15/AIO226	ADCIN15
26	ADCIN14/AIO225	ADCIN14

1	GPIO11	GPIO11
2	VDDIO	VDDIO
3	GPIO12	GPIO12
4	GPIO13	GPIO13
5	GPIO14	GPIO14
6	GPIO15	GPIO15
7	VDDIO	GPIO16
8	VDD	GPIO17
9	ADCINC0/GPIO199	GPIO18
10	ADCINC1/GPIO200	VDDIO
11	ADCINC6/GPIO203	GPIO19
12	ADCINC5/GPIO204	GPIO20
13	ADCINC4/GPIO205	GPIO21
14	ADCINC3/GPIO206	GPIO99
15	ADCINC2/AIO237	VDDIO
16	VREFLOC	VDD
17	VSSA	VSSA/VREFLOA
18	VDDA	VDDA
19	VREFHIA	VREFHIA
20	ADCINA5/AIO232	ADCINA5
21	ADCINA4/AIO231	ADCINA4
22	ADCINA3/AIO230	ADCINA3
23	ADCINA2/AIO229	ADCINA2
24	ADCINA1/AIO228	ADCINA1
25	ADCINA0/AIO227	ADCINA0

75	GPIO69	GPIO69
74	GPIO43	GPIO43
73	GPIO42	GPIO42
72	GPIO47	VDDIO
71	GPIO46	VDD
70	VDDIO	VDDOSC
69	XRSn	XRSn
68	X1	X1
67	VSSOSC	VSSOSC
66	X2	X2
65	VDDOSC	VDDOSC
64	VREGENZ	VREGENZ
63	VDD	VDD
62	VDDIO	VDDIO
61	GPIO66	GPIO66
60	GPIO65	GPIO65
59	GPIO64	GPIO64
58	GPIO63	GPIO63
57	GPIO62	GPIO62
56	GPIO61	GPIO61
55	VDDIO	VDDIO
54	GPIO60	GPIO60
53	GPIO59	GPIO59
52	GPIO58	GPIO58
51	GPIO41	GPIO41

Figure 2-2. F2837x and F28P65x 100-Pin Overlay

2.2 Use of Existing 176-Pin F2837x PCB Design

Considerations for the use of existing F2837x 176P PCB design with with a F28P65x device is covered in this section. Table 2-1 outlines the migration.

For the color legend, see Figure 2-1.

For certain pins, GPIO number assignments have moved to different pin positions in F28P65x. Additionally, F28P65x ADCD is not available, however the F2837x ADCD pin resources are now ADCA and ADCB channels in F28P65x. Section 2.2.3 covers the migration changes that need to take place in the application software for the GPIO and ADC changes between F2837x and F28P65x devices.

Table 2-1. 176-Pin PTP Between F2837x and F28P65x

Pin No	Pin Name		Transition Type	Action	
	F2837x	F28P65x		F2837x to F28P65x	F28P65x to F2837x
Minor Incompatibility - Signals in Common(1)					
29	ADCINC4	ADCINC4/GPIO205	Common Analog Channel	Use ADCINC4	
30	ADCINC3	ADCINC3/GPIO206		Use ADCINC3	
31	ADCINC2	ADCINC2/AIO237		Use ADCINC2	
38	ADCINA5	ADCINA5/AIO232		Use ADCINA5	
39	ADCINA4	ADCINA4/AIO231		Use ADCINA4	
40	ADCINA3	ADCINA3/AIO230		Use ADCINA3	
41	ADCINA2	ADCINA2/AIO229		Use ADCINA2	
42	ADCINA1	ADCINA1/AIO228		Use ADCINA1	
43	ADCINA0	ADCINA0/AIO227		Use ADCINA0	
44	ADCIN14	ADCIN14/AIO225		Use ADCIN14	
45	ADCIN15	ADCIN15/AIO226		Use ADCIN15	
46	ADCINB0	ADCINB0/AIO233		Use ADCINB0	
47	ADCINB1	ADCINB1/AIO234		Use ADCINB1	
48	ADCINB2	ADCINB2/AIO235		Use ADCINB2	
49	ADCINB3	ADCINB3/AIO236		Use ADCINB3	
77	TDI	GPIO222/TDI	Common JTAG	Use TDI	
78	TDO	GPIO223/TDO		Use TDO	
92	ERRORSTS	GPIO224/ERRORSTS	Common ERROR Pin	Use ERRORSTS	
Medium Incompatibility - Different Signals, Same Type					
22	GPIO22	ADCINC0/GPIO199	GPIO Function Compatible. Software needs to account for the change in GPIO assignment on these pins.	Update code to GPIO199	Update code to GPIO22
23	GPIO23	ADCINC9/GPIO200		Update code to GPIO200	Update code to GPIO23
24	GPIO24	ADCINC8/GPIO201		Update code to GPIO201	Update code to GPIO24
25	GPIO25	ADCINC7/GPIO202		Update code to GPIO202	Update code to GPIO25
27	GPIO26	ADCINC6/GPIO203		Update code to GPIO203	Update code to GPIO26
28	GPIO27	ADCINC5/GPIO204		Update code to GPIO204	Update code to GPIO27
63	GPIO30	ADCINA11/GPIO214		Update code to GPIO214	Update code to GPIO30
64	GPIO28	ADCINB4/GPIO215		Update code to GPIO215	Update code to GPIO28
65	GPIO29	ADCINB5/GPIO216		Update code to GPIO216	Update code to GPIO29
66	GPIO31	ADCINB8/GPIO217		Update code to GPIO217	Update code to GPIO31
67	GPIO32	ADCINB9/GPIO218		Update code to GPIO218	Update code to GPIO32
56	ADCIND0	ADCINB7	Analog Function Compatible	Update code to ADCINB7	Update code to ADCIND0
57	ADCIND1	ADCINA6		Update code to ADCINA6	Update code to ADCIND1
58	ADCIND2	ADCINA7		Update code to ADCINA7	Update code to ADCIND2
59	ADCIND3	ADCINA8		Update code to ADCINA8	Update code to ADCIND3
60	ADCIND4	ADCINA9		Update code to ADCINA9	Update code to ADCIND4
Major incompatibility - Different Signals and Types					
79	TRSTn	GPIO30	TRSTn Function	Do not use as GPIO as this has a 2.2k pulldown resistor	Use as TRSTn pin with a 2.2k pulldown resistor

Table 2-1. 176-Pin PTP Between F2837x and F28P65x (continued)

Pin No	Pin Name		Transition Type	Action	
	F2837x	F28P65x		F2837x to F28P65x	F28P65x to F2837x
11	VDDIO	GPIO22	Power to GPIO	Connect to 3.3V Supply. Ensure the GPIO is not configured as output	Use as VDDIO
20	VDDIO	GPIO106			
82	VDDIO	GPIO26			
106	VDDIO	GPIO105			
116	VDDIO	GPIO32			
125	VDDIO	GPIO27			
147	VDDIO	GPIO104			
159	VDDIO	GPIO24			
126	VDD	GPIO103		Connect to 1.2V Supply. Disable digital input for GPIO	Use as VDD
153	VDD	GPIO25			
158	VDD	GPIO31			
61	VDD	ADCINA10/GPIO213	Power To Analog	Option to use the analog channels to monitor VDD, VDDIO, VREFLO or VREFHI signals	Use as VDD
20	VDDIO	ADCINC1/GPIO198			Use as VDDIO
68	VDDIO	ADCINB10/GPIO219			
51	VREFLOD	ADCINB11	Reference to Analog		Use as analog reference pins
55	VREFHID	ADCINB6			
73	FLT1	GPIO29	Test Pads to GPIO	Use as GPIO pins if routed properly in board	Use as test pads
74	FLT2	GPIO28			

(1) Channel to use selected in software

2.2.1 JTAG TRSTn No-Connect

When migrating from the F2837x to the F28P65x device, the TRSTn pin in the JTAG connection should be left as a no-connect. For a visualization, see Figure 2-3.

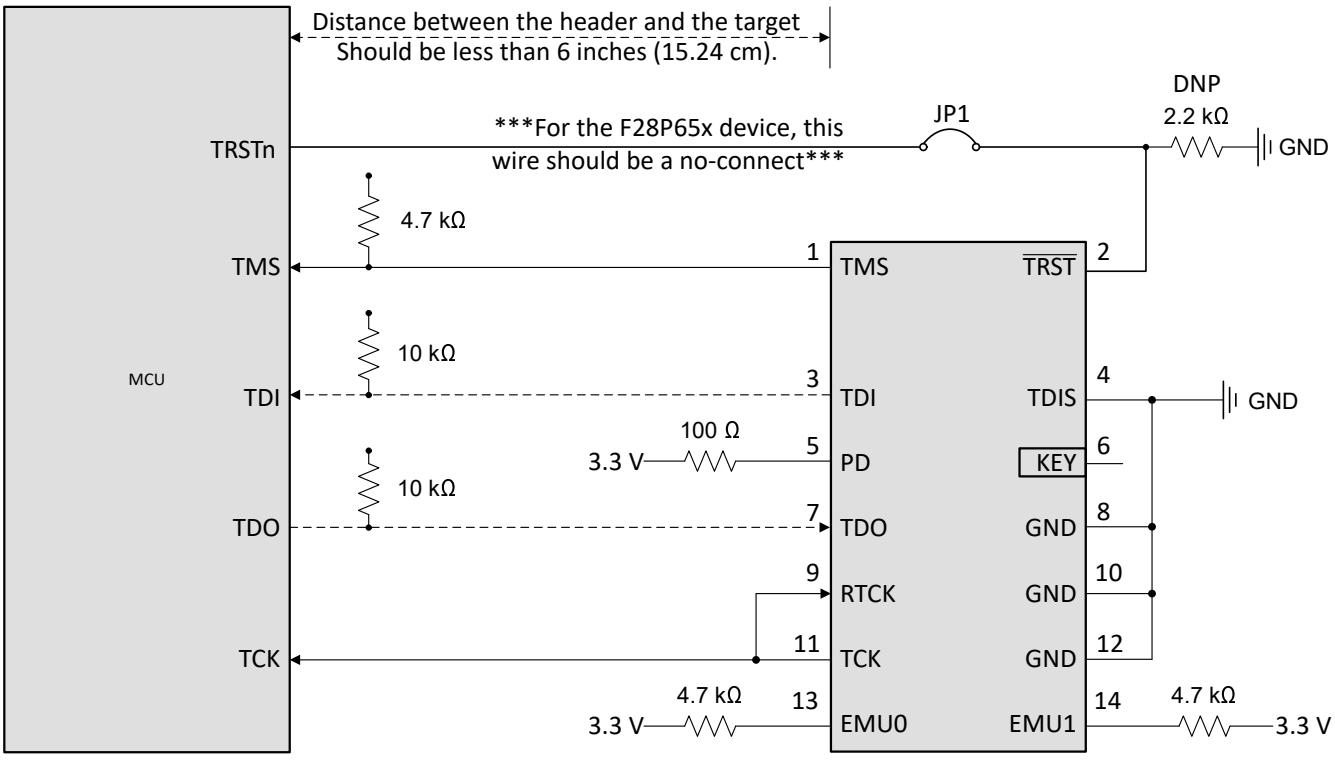


Figure 2-3. JTAG Connection Diagram

2.2.2 GPIO Input Buffer Control Register

The GPIO input buffer control register (GPIOINENACTRL) configures whether the input buffer is enabled or disabled. Default setting is disabled. In the case where the corresponding GPIO is connected to VDD after migrating to F28P65x, the appropriate GPIO bit in this register has to be set to '1' to prevent errors when powering up the F28P65x device. This register is in the analog subsystem, which has a base address of 0x0005 D700. GPIOINENACTRL has an offset of 0x134.

Table 2-2. GPIOINENACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	GPIO103	R/W	1h	One time configuration for GPIO103 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
4	GPIO46	R/W	1h	One time configuration for GPIO46 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
3	GPIO31	R/W	1h	One time configuration for GPIO31 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
2	GPIO25	R/W	1h	One time configuration for GPIO25 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
1	GPIO23	R/W	1h	One time configuration for GPIO23 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
0	GPIO0	R/W	1h	One time configuration for GPIO0 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn

2.2.3 176-Pin GPIO Pin/Multiplex and ADCD Considerations

Section 2.2.3.1 outlines the GPIO number and the corresponding peripheral multiplex pin functions of certain pin positions that changed from F2837x to F28P65x. Most of the peripheral functions on these pin positions were retained for both devices, with the exception of a few, as shown on the table. Examples below illustrate how to account for the GPIO number and peripheral function changes:

- If in F2837x application, pin 22 is used as GPIO22 SCIB_TX (mux position 3) pin and F28P65x device is dropped-in, GPIO pin assignment has to be changed to GPIO199 SCIB_TX (mux positon 3) in the software

Section 2.2.3.2 outlines the ADC channels that will take the position of ADCD module when moving from F2837x to F28P65x. Change the ADC channel setup accordingly depending on which function/channel assignment is allocated based on the table.

2.2.3.1 176-Pin PTP Pins with Different GPIO Assignment

Table 2-3. 176-P PTP Legend

Color	Description
	common for both devices
	applicable only for F2837x
	applicable only for F28P65x

Note

For the mux table below, there would be instances where SPI pins will show differences, but this will be only with the name. Functionality will be the same. Name change in F28P65x are as follows:

- SPI_SOMI to SPI_POCI
- SPI_SIMO to SPI_PICO
- SPI_STE to SPI_PTE

Table 2-4. Mux Table Lookup for GPIO Number Changes

Pin	0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15
22	GPIO22	EQEP1_STROBE	MCLKXA	SCIB_TX	EPWM12_A	SPIB_CLK	SD1_D4						
	GPIO199		EPWM17_A					MCANA_TX	EMIF1_RAS			SPIC_CLK	ESC_TX1_DATA0
23	GPIO23	EQEP1_INDEX	MFSXA	SCIB_RX	EPWM12_B	SPIB_STE	SD1_C4						
	GPIO200		EPWM17_B			SPIB_PTE		MCANA_RX	EMIF1_CAS	ESC_TX1_DATA1		SPIC_PTE	ESC_PHY_RESETn
24	GPIO24	OUTPUTXBAR1	EQEP2_A	MDXB	LINB_TX	SPIB_SIMO	SD2_D1						
	GPIO201			EPWM18_A		SPIB_PICO		PMBUSA_SCL	EMIF1_DQM0	ESC_TX1_DATA2	EPWM13_A	ESC_RX0_DATA1	ESC_RX0_CLK
25	GPIO25	OUTPUTXBAR2	EQEP2_B	MDRB	LINB_RX	SPIB_SOMI	SD2_C1						
	GPIO202			EPWM18_B		SPIB_POCI		PMBUSA_SDA	EMIF1_DQM1	ESC_TX1_DATA3	EPWM13_B	FSITXA_D1	
27	GPIO26	OUTPUTXBAR3	EQEP2_INDEX	MCLKXB	OUTPUTXBAR3	SPIB_CLK	SD2_D2						
	GPIO203			SPIA_POCI			SD3_D1	PMBUSA_ALERT	EMIF1_DQM2	ESC_MDIO_CLK	EPWM14_A	FSITXA_D0	EPWM8_B
28	GPIO27	OUTPUTXBAR4	EQEP2_STROBE	MFSXB	OUTPUTXBAR4	SPIB_STE	SD2_C2						
	GPIO204			SPIA_CLK		SPIB_PTE		PMBUSA_CTL	EMIF1_DQM3	ESC_MDIO_DATA	EPWM14_B	FSITXA_CLK	SD1_D3
64	GPIO28	SCIA_RX	EMIF1_CS4n		OUTPUTXBAR5	EQEP3_A	SD2_D3						
	GPIO215			CANA_RX				EMIF1_CS2n	I2CB_SDA	SPIC_POCI	EPWM15_A	LINA_TX	EMIF1_D12
65	GPIO29	SCIA_TX	EMIF1_SDCKE		OUTPUTXBAR6	EQEP3_B	SD2_C3						
	GPIO216			SPID_CLK				EMIF1_CS3n	ESC_LATCH0	ESC_I2C_SDA	EPWM15_B	ESC_SYNC0	EMIF1_D13
63	GPIO30	CANA_RX	EMIF1_CLK	MCANA_RX	OUTPUTXBAR7	EQEP3_STROBE	SD2_D4						
	GPIO214							EMIF1_CS4n	ESC_LATCH1	ESC_I2C_SCL	EPWM16_A	ESC_SYNC1	SPID_PICO

Table 2-4. Mux Table Lookup for GPIO Number Changes (continued)

Pin	0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15
66	GPIO31	CANA_TX	EMIF1_WEn	MCANA_TX	OUTPUTXBAR8	EQEP3_INDEX	SD2_C4						
	GPIO217							EMIF1_RNW	I2CA_SDA	SPID_PTE	EPWM16_B	LINB_TX	SPID_POCI
67	GPIO32	I2CA_SDA	EMIF1_CS0n										
	GPIO218			SPIA_PICO	EQEP4_A	LINB_TX	CLB_OUTPUTXBAR1	EMIF1_OEn	I2CA_SCL				SPID_CLK

2.2.3.2 ADCD Channel Migration

Table 2-5. 176-Pin PTP ADCD Resource Migration

Pin No	Pin Name		Transition Type	Action	
	F2837x	F28P65x		F2837x to F28P65x	F28P65x to F2837x
56	ADCIND0	ADCINB7	Analog Function Compatible	Update code to ADCINB7	Update code to ADCIND0
57	ADCIND1	ADCINA6		Update code to ADCINA6	Update code to ADCIND1
58	ADCIND2	ADCINA7		Update code to ADCINA7	Update code to ADCIND2
59	ADCIND3	ADCINA8		Update code to ADCINA8	Update code to ADCIND3
60	ADCIND4	ADCINA9		Update code to ADCINA9	Update code to ADCIND4
51	VREFLOD	ADCINB11	Reference to Analog	ADCINB11 can be used to sample VREFLO signal	Use as analog reference pins
55	VREFHID	ADCINB6		ADCINB6 can be used to sample VREFHI signal	

2.3 176-Pin PTP New PCB Design

To enable early development on F28P65x using existing F2837x 176-Pin device, this supplemental section covers the dual routing technique as illustrated in Figure 2-4. The complete pin usage recommendation is outlined in Figure 2-1.

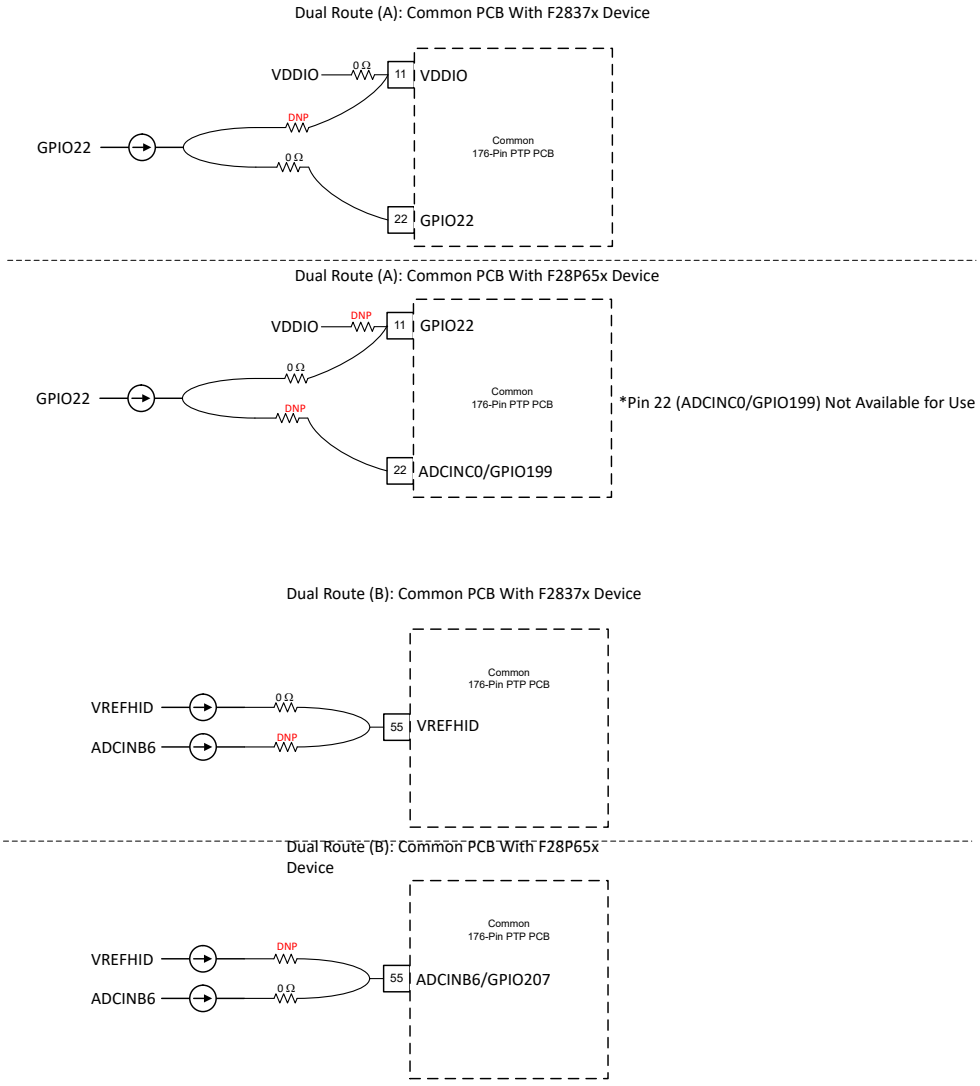


Figure 2-4. Dual Routing Technique Illustrated

For the color legend, see Figure 2-1.

Table 2-6. Common 176-Pin PTP PCB Design for F2837x and F28P65x

Pin No	Pin Name		Transition Type	Action	
	F2837x	F28P65x		F2837x to F28P65x	F28P65x to F2837x
Minor Incompatibility - Signals in Common					
29	ADCINC4	ADCINC4/GPIO205	Common Analog Channel	Use ADCINC4	
30	ADCINC3	ADCINC3/GPIO206		Use ADCINC3	
31	ADCINC2	ADCINC2/AIO237		Use ADCINC2	
38	ADCINA5	ADCINA5/AIO232		Use ADCINA5	
39	ADCINA4	ADCINA4/AIO231		Use ADCINA4	
40	ADCINA3	ADCINA3/AIO230		Use ADCINA3	
41	ADCINA2	ADCINA2/AIO229		Use ADCINA2	
42	ADCINA1	ADCINA1/AIO228		Use ADCINA1	
43	ADCINA0	ADCINA0/AIO227		Use ADCINA0	
44	ADCIN14	ADCIN14/AIO225		Use ADCIN14	
45	ADCIN15	ADCIN15/AIO226		Use ADCIN15	
46	ADCINB0	ADCINB0/AIO233		Use ADCINB0	
47	ADCINB1	ADCINB1/AIO234		Use ADCINB1	
48	ADCINB2	ADCINB2/AIO235		Use ADCINB2	
49	ADCINB3	ADCINB3/AIO236		Use ADCINB3	
77	TDI	GPIO222/TDI	Common JTAG	Use TDI	
78	TDO	GPIO223/TDO		Use TDO	
92	ERRORSTS	GPIO224/ERRORSTS	Common ERROR Pin	Use ERRORSTS	
Medium Incompatibility - Different Signals, Same Type					
56	ADCIND0	ADCINB7	Analog Function Compatible	Update code to ADCINB7	Update code to ADCIND0
57	ADCIND1	ADCINA6		Update code to ADCINA6	Update code to ADCIND1
58	ADCIND2	ADCINA7		Update code to ADCINA7	Update code to ADCIND2
59	ADCIND3	ADCINA8		Update code to ADCINA8	Update code to ADCIND3
60	ADCIND4	ADCINA9		Update code to ADCINA9	Update code to ADCIND4
Medium incompatibility - Dual routing [1]					
22	GPIO22	ADCINC0/GPIO199	Dual PCB Route, through 0-Ohm Resistor or DNP to either GPIO channel or Power pin.	Dual route (A) to Pin 22 and Pin 11	
23	GPIO23	ADCINC9/GPIO200		Dual route (A) to Pin 23 and Pin 16	
24	GPIO24	ADCINC8/GPIO201		Dual route (A) to Pin 24 and Pin 159	
25	GPIO25	ADCINC7/GPIO202		Dual route (A) to Pin 25 and Pin 153	
27	GPIO26	ADCINC6/GPIO203		Dual route (A) to Pin 27 and Pin 82	
28	GPIO27	ADCINC5/GPIO204		Dual route (A) to Pin 28 and Pin 125	
63	GPIO30	ADCINA11/GPIO214		Dual route (A) to Pin 63 and Pin 79, consult datasheet for F2837x TRSTn requirement	
64	GPIO28	ADCINB4/GPIO215		Dual route (A) to Pin 64 and Pin 74	
65	GPIO29	ADCINB5/GPIO216		Dual route (A) to Pin 65 and Pin 73	
66	GPIO31	ADCINB8/GPIO217		Dual route (A) to Pin 66 and Pin 158	
67	GPIO32	ADCINB9/GPIO218		Dual route (A) to Pin 67 and Pin 116	
Medium incompatibility - Dual routing[2]					
55	VREFHID	ADCINB6	ADC VREFHI to Analog	Populate 0 ohm resistor to ADCINB6	Populate 0 ohm resistor to VREFHID
51	VREFLOD	ADCINB11	ADC VREFLO to Analog	Populate 0 ohm resistor to ADCINB11	opulate 0 ohm resistor to VREFLOD
79	TRSTn	GPIO30	TRSTn Function	Populate 0 ohm resistor to GPIO30	Populate 0 ohm resistor to TRSTn
20	VDDIO	GPIO106	Dual PCB Route, through 0-Ohm Resistor or DNP to GPIO/AGPIO channel or Power pin.	Populate 0 ohm resistor to GPIO/AGPIO	Populate 0 ohm resistor to VDDIO
106	VDDIO	GPIO105			
147	VDDIO	GPIO104			
20	VDDIO	ADCINC1/GPIO198			
68	VDDIO	ADCINB10/GPIO219			
61	VDD	ADCINA10/GPIO213			Populate 0 ohm resistor to VDD
153	VDD	GPIO25			
158	VDD	GPIO31			
126	VDD	GPIO103			

[1] Use Dual Routing example diagram (A) in Figure 2-4
[2] Use Dual Routing example diagram (B) in Figure 2-4

Table 2-6. Common 176-Pin PTP PCB Design for F2837x and F28P65x (continued)

Pin No	Pin Name		Transition Type	Action	
	F2837x	F28P65x		F2837x to F28P65x	F28P65x to F2837x
74	FLT2	GPIO28	Dual PCB Route, through 0-Ohm Resistor or DNP to GPIO channel or FLT	Populate 0 ohm resistor to GPIO channel	Populate 0 ohm resistor to FLT pads
73	FLT1	GPIO29			

2.4 100-Pin PZP New PCB Design

To enable early development on F28P65x using existing F2837x 100-Pin device, this supplemental section covers the dual routing technique as illustrated in Figure 2-5. The complete pin usage recommendation is outlined in Figure 2-2.

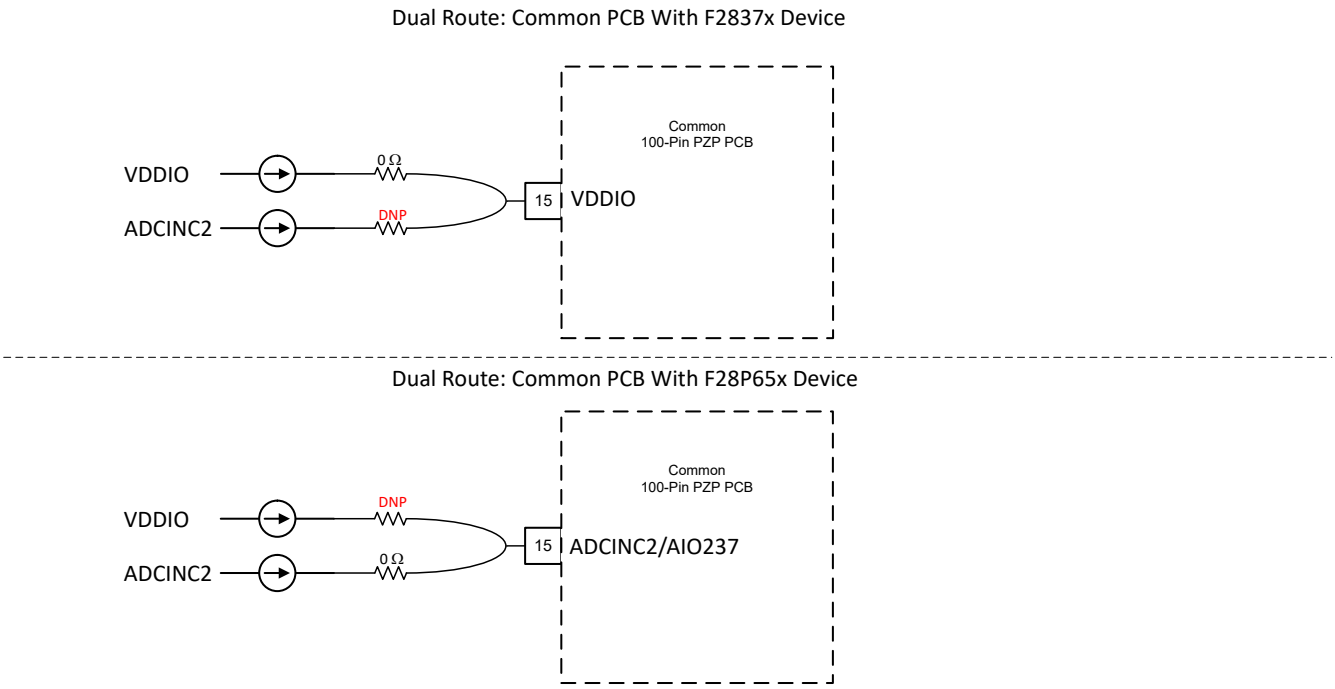


Figure 2-5. Dual Routing Technique Illustrated

For the color legend, see Figure 2-2.

Table 2-7. Common 100-Pin PTP PCB Design for F2837x and F28P65x

Pin No	Pin Name		Transition Type	Action	
	F2837x	F28P65x		F2837x to F28P65x	F28P65x to F2837x
Minor Incompatibility - Signals in Common					
17	VSSA/ VREFLOA	VSSA	Common Analog Channel	Use VSSA	
20	ADCINA5	ADCINA5/AIO232		Use ADCINA5	
21	ADCINA4	ADCINA4/AIO231		Use ADCINA4	
22	ADCINA3	ADCINA3/AIO230		Use ADCINA3	
23	ADCINA2	ADCINA2/AIO229		Use ADCINA2	
24	ADCINA1	ADCINA1/AIO228		Use ADCINA1	
25	ADCINA0	ADCINA0/AIO227		Use ADCINA0	
26	ADCIN14	ADCIN14/AIO225		Use ADCIN14	
27	ADCIN15	ADCIN15/AIO226		Use ADCIN15	
28	ADCINB0	ADCINB0/AIO233		Use ADCINB0	
29	ADCINB1	ADCINB1/AIO234		Use ADCINB1	
30	ADCINB2	ADCINB2/AIO235		Use ADCINB2	
31	ADCINB3	ADCINB3/AIO236		Use ADCINB3	
46	TDI	GPIO222/TDI	Common JTAG	Use TDI	
47	TDO	GPIO223/TDO		Use TDO	
Medium incompatibility - Dual routing[3]					

Table 2-7. Common 100-Pin PTP PCB Design for F2837x and F28P65x (continued)

Pin No	Pin Name		Transition Type	Action	
	F2837x	F28P65x		F2837x to F28P65x	F28P65x to F2837x
7	GPIO16	VDDIO		Populate 0 ohm resistor to VDDIO	Populate 0 ohm resistor to GPIO
8	GPIO17	VDD		Populate 0 ohm resistor to VDD	
32	ADCINB4	VREFLOB		Populate 0 ohm resistor to VREFLOB	Populate 0 ohm resistor to ADC channel
33	ADCINB5	VSSA		Populate 0 ohm resistor to VSSA	
9	GPIO18	ADCINC0/GPIO199	Dual PCB Route, through 0-Ohm Resistor or DNP.	Populate 0 ohm resistor to GPIO/AGPIO	Populate 0 ohm resistor to GPIO
11	GPIO19	ADCINC6/GPIO203			
12	GPIO20	ADCINC5/GPIO204			
13	GPIO21	ADCINC4/GPIO205			
14	GPIO99	ADCINC3/GPIO206			
48	TRSTn	GPIO30			Populate 0 ohm resistor to TRSTn
37	VREFHIB	ADCINB7/GPIO208			Populate 0 ohm resistor to VREFHIB
39	VDD	ADCINA10/GPIO213			Populate 0 ohm resistor to VDD
71	VDD	GPIO46			
84	VDD	GPIO25			
89	VDD	GPIO0			
15	VDDIO	ADCINC2/AIO237			Populate 0 ohm resistor to VDDIO
10	VDDIO	ADCINC1/GPIO200			
40	VDDIO	ADCINA11/GPIO214			
72	VDDIO	GPIO47			
83	VDDIO	GPIO80			
90	VDDIO	GPIO1			
38	VDDA	ADCINA6/GPIO209			Populate 0 ohm resistor to VDDA
33	VSSA	ADCINB5			Populate 0 ohm resistor to VSSA
36	VSSA	ADCINB6/GPIO207			
42	FLT1	GPIO34			Populate 0 ohm resistor to FLT pads
43	FLT2	GPIO35			
Major incompatibility (have to be isolated by 0 ohm resistor) - Dual routing[4]					
16	VDD	VREFLOC	Dual PCB Route, through 0-Ohm Resistor or DNP.	Populate 0 ohm resistor to VREFLO	Populate 0 ohm resistor to VDD
34	VREFLOB	VREFHIB		Populate 0 ohm resistor to VREFHI	Populate 0 ohm resistor to VREFLO
35	VSSA	VDDA		Populate 0 ohm resistor to VDDA	Populate 0 ohm resistor to VSSA

2.5 337-BGA ZWT Application to 256-BGA ZEJ or 169-BGA NMR

F2837x BGA pinout is only available in 337-BGA ZWT pinout. In F28P65x, BGA pinout is available in both 256 ZEJ and 169 NMR package outlines. There is obviously no board reusability when switching from F2837x BGA to F28P65x BGA due to the different package types involved so a new board design is required. Table 2-8 provides the comparison of the available digital channels and Table 2-9 shows the analog channels while Table 2-10 summarizes the available resources on the different BGA packages for both F2837x and F28P65x devices. Use these tables as references in planning pin resources when designing new schematics/boards for F28P65x BGA devices. In general, there will be more available flexible analog and digital pins in either the F28P65x 256 or 169 BGA compared to the F2837x BGA package.

Table 2-8. F2837x and F28P65x BGA Digital Channel Comparison

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
GPIO0	GPIO0	GPIO0
GPIO1	GPIO1	GPIO1
GPIO2	GPIO2	GPIO2
GPIO3	GPIO3	GPIO3
GPIO4	GPIO4	GPIO4
GPIO5	GPIO5	GPIO5
GPIO6	GPIO6	GPIO6
GPIO7	GPIO7	GPIO7

[3] Use Dual Routing example diagram in Figure 2-5
[4] Use Dual Routing example diagram in Figure 2-5

Table 2-8. F2837x and F28P65x BGA Digital Channel Comparison (continued)

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
GPIO8	GPIO8	GPIO8
GPIO9	GPIO9	GPIO9
GPIO10	GPIO10	GPIO10
GPIO11	GPIO11	GPIO11
GPIO12	GPIO12	GPIO12
GPIO13	GPIO13	GPIO13
GPIO14	GPIO14	GPIO14
GPIO15	GPIO15	GPIO15
GPIO16	GPIO16	GPIO16
GPIO17	GPIO17	GPIO17
GPIO18	GPIO18	GPIO18
GPIO19	GPIO19	GPIO19
GPIO20	GPIO20	GPIO20
GPIO21	GPIO21	GPIO21
GPIO22	GPIO22	GPIO22
GPIO23	GPIO23	GPIO23
GPIO24	GPIO24	GPIO24
GPIO25	GPIO25	GPIO25
GPIO26	GPIO26	GPIO26
GPIO27	GPIO27	GPIO27
GPIO28	GPIO28	GPIO28
GPIO29	GPIO29	GPIO29
GPIO30	GPIO30	GPIO30
GPIO31	GPIO31	
GPIO32	GPIO32	GPIO32
GPIO33	GPIO33	GPIO33
GPIO34	GPIO34	GPIO34
GPIO35	GPIO35	GPIO35
GPIO36	GPIO36	GPIO36
GPIO37	GPIO37	GPIO37
GPIO38	GPIO38	GPIO38
GPIO39	GPIO39	-
GPIO40	GPIO40	GPIO40
GPIO41	GPIO41	GPIO41
GPIO42	GPIO42	GPIO42
GPIO43	GPIO43	GPIO43
GPIO44	GPIO44	GPIO44
GPIO45	GPIO45	GPIO45
GPIO46	GPIO46	-
GPIO47	GPIO47	-
GPIO48	GPIO48	GPIO48
GPIO49	GPIO49	GPIO49
GPIO50	GPIO50	GPIO50
GPIO51	GPIO51	GPIO51
GPIO52	GPIO52	GPIO52
GPIO53	GPIO53	GPIO53
GPIO54	GPIO54	GPIO54

Table 2-8. F2837x and F28P65x BGA Digital Channel Comparison (continued)

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
GPIO55	GPIO55	GPIO55
GPIO56	GPIO56	GPIO56
GPIO57	GPIO57	GPIO57
GPIO58	GPIO58	GPIO58
GPIO59	GPIO59	GPIO59
GPIO60	GPIO60	-
GPIO61	GPIO61	GPIO61
GPIO62	GPIO62	GPIO62
GPIO63	GPIO63	GPIO63
GPIO64	GPIO64	GPIO64
GPIO65	GPIO65	GPIO65
GPIO66	GPIO66	GPIO66
GPIO67	GPIO67	-
GPIO68	GPIO68	GPIO68
GPIO69	GPIO69	GPIO69
GPIO70	GPIO70	GPIO70
GPIO71	GPIO71	GPIO71
GPIO72	GPIO72	GPIO72
GPIO73	GPIO73	GPIO73
GPIO74	GPIO74	GPIO74
GPIO75	GPIO75	GPIO75
GPIO76	GPIO76	GPIO76
GPIO77	GPIO77	GPIO77
GPIO78	GPIO78	GPIO78
GPIO79	GPIO79	GPIO79
GPIO80	GPIO80	GPIO80
GPIO81	GPIO81	-
GPIO82	GPIO82	GPIO82
GPIO83	GPIO83	GPIO83
GPIO84	GPIO84	GPIO84
GPIO85	GPIO85	GPIO85
GPIO86	GPIO86	GPIO86
GPIO87	GPIO87	GPIO87
GPIO88	GPIO88	GPIO88
GPIO89	GPIO89	GPIO89
GPIO90	GPIO90	GPIO90
GPIO91	GPIO91	GPIO91
GPIO92	GPIO92	GPIO92
GPIO93	GPIO93	GPIO93
GPIO94	GPIO94	GPIO94
GPIO95	GPIO95	-
GPIO96	GPIO96	-
GPIO97	GPIO97	-
GPIO98	GPIO98	-
GPIO99	GPIO99	GPIO99
GPIO100	GPIO100	-
GPIO101	GPIO101	-

Table 2-8. F2837x and F28P65x BGA Digital Channel Comparison (continued)

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
GPIO102	GPIO102	-
GPIO103	GPIO103	GPIO103
GPIO104	GPIO104	GPIO104
GPIO105	GPIO105	GPIO105
GPIO106	GPIO106	-
GPIO107	GPIO107	-
GPIO108	GPIO108	-
GPIO109	GPIO109	-
GPIO110	GPIO110	-
GPIO111	GPIO111	-
GPIO112	GPIO112	-
GPIO113	GPIO113	-
GPIO114	GPIO114	-
GPIO115	GPIO115	-
GPIO116	GPIO116	-
GPIO117	-	-
GPIO118	-	-
GPIO119	GPIO119	-
GPIO120	GPIO120	-
GPIO121	-	-
GPIO122	GPIO122	-
GPIO123	GPIO123	-
GPIO124	GPIO124	-
GPIO125	GPIO125	-
GPIO126	GPIO126	-
GPIO127	GPIO127	-
GPIO128	GPIO128	-
GPIO129	GPIO129	-
GPIO130	GPIO130	-
GPIO131	GPIO131	-
GPIO132	GPIO132	-
GPIO133	GPIO133	GPIO133
GPIO134	GPIO134	-
GPIO135	-	-
GPIO136	-	-
GPIO137	-	-
GPIO138	-	-
GPIO139	-	-
GPIO140	-	-
GPIO141	GPIO141	-
GPIO142	GPIO142	-
GPIO143	-	-
GPIO144	-	-
GPIO145	GPIO145	-
GPIO146	GPIO146	-
GPIO147	GPIO147	-
GPIO148	GPIO148	-

Table 2-8. F2837x and F28P65x BGA Digital Channel Comparison (continued)

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
GPIO149	GPIO149	-
GPIO150	GPIO150	-
GPIO151	GPIO151	-
GPIO152	GPIO152	-
GPIO153	GPIO153	-
GPIO154	GPIO154	-
GPIO155	GPIO155	-
GPIO156	GPIO156	-
GPIO157	GPIO157	-
GPIO158	GPIO158	-
GPIO159	GPIO159	-
GPIO160	GPIO160	-
GPIO161	GPIO161	-
GPIO162	GPIO162	-
GPIO163	GPIO163	-
GPIO164	GPIO164	-
GPIO165	GPIO165	-
GPIO166	GPIO166	-
GPIO167	GPIO167	-
GPIO168	GPIO168	-
-	GPIO198	GPIO198
-	GPIO199	GPIO199
-	GPIO200	GPIO200
-	GPIO201	GPIO201
-	GPIO202	GPIO202
-	GPIO203	GPIO203
-	GPIO204	GPIO204
-	GPIO205	GPIO205
-	GPIO206	GPIO206
-	GPIO207	GPIO207
-	GPIO208	GPIO208
-	GPIO209	GPIO209
-	GPIO210	GPIO210
-	GPIO211	GPIO211
-	GPIO212	GPIO212
-	GPIO213	GPIO213
-	GPIO214	GPIO214
-	GPIO215	GPIO215
-	GPIO216	GPIO216
-	GPIO217	GPIO217
-	GPIO218	GPIO218
-	GPIO219	-
-	GPIO220/X1	GPIO220/X1
-	GPIO221/X2	GPIO221/X2
-	GPIO222	GPIO222
-	GPIO223	GPIO223

Table 2-8. F2837x and F28P65x BGA Digital Channel Comparison (continued)

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
-	GPIO224	GPIO224

Table 2-9. F2837x and F28P65x BGA Analog Channel Comparison

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
ADCIN14	A14/B14/C14/AIO225	A14/B14/C14/AIO225
ADCIN15	A15/B15/C15/AIO226	A15/B15/C15/AIO226
A0/DACA_OUT	A0/DACA_OUT/AIO277	A0/DACA_OUT/AIO277
A1/DACB_OUT	A1/AIO228	A1/AIO228
A2	A2/AIO229	A2/AIO229
A3	A3/AIO230	A3/AIO230
A4	A4/AIO231	A4/AIO231
A5	A5/AIO232	A5/AIO232
-	A6/GPIO209	A6/GPIO209
-	A7/GPIO210	A7/GPIO210
-	A8/GPIO211	A8/GPIO211
-	A9/GPIO212	A9/GPIO212
-	A10/GPIO213	A10/GPIO213
-	A11/GPIO214	A11/GPIO214
B0/VDAC	B0/VDAC/AIO233	B0/VDAC/AIO233
B1/DACC_OUT	B1/DACC_OUT/AIO234	B1/DACC_OUT/AIO234
B2	B2/AIO235	B2/AIO235
B3	B3/AIO236	B3/AIO236
B4	B4/GPIO215	B4/GPIO215
B5	B5/GPIO216	B5/GPIO216
-	B6/GPIO207	B6/GPIO207
-	B7/GPIO208	B7/GPIO208
-	B8/GPIO217	B8/GPIO217
-	B9/GPIO218	B9/GPIO218
-	B10/GPIO219	-
-	B11/AIO240	-
-	B13/AIO238	-
-	C0/GPIO199	C0/GPIO199
-	C1/GPIO198	C1/GPIO198
C2	C2/AIO237	C2/AIO237
C3	C3/GPIO206	C3/GPIO206
C4	C4/GPIO205	C4/GPIO205
C5	C5/GPIO204	C5/GPIO204
-	C6/GPIO203	C6/GPIO203
-	C7/GPIO202	C7/GPIO202
-	C8/GPIO201	C8/GPIO201
-	C9/GPIO200	C9/GPIO200
-	C10/AIO241	-
-	C11/AIO242	-
-	C13/AIO239	-
D0	-	-
D1	-	-
D2	-	-

Table 2-9. F2837x and F28P65x BGA Analog Channel Comparison (continued)

F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
D3	-	-
D4	-	-
D5	-	-
VREFHIA	VREFHIA	VREFHIA
VREFHIB	VREFHIB	VREFHIB
VREFHIC	VREFHIC	VREFHIC
VREFHID	-	-
VREFLOA	VREFLOA	VREFLOA
VREFLOB	VREFLOB	VREFLOB
VREFLOC	VREFLOC	VREFLOC
VREFLOD	-	-

Table 2-10. F2837x and F28P65x Pin Summaries

Description	F2837x 337 ZWT	F28P65x 256 ZEJ	F28P65x 169 NMR
Total Analog Pins (excluding VREFHI/LO)	24	40	34
Number of analog channels with digital input (AIO)	0	18	13
Number of Flexible Analog/Digital Pins (AGPIO)	0	22	21
Total Digital Pins (excluding X1/X2)	169	183	117

3 Feature Differences for System Consideration

The differences and similarities that exist when moving between the F2837x and F28P65x devices is explored in this section.

3.1 New Features in F28P65x

This section outlines features that only exist in the F28P65x device. For details on each of these new features, see the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* (SPRUIZ1).

3.1.1 Lock-step Compare Module (LCM)

CPU2 instance, including PIE and DMA will be supported by lock-step mode configuration to detect permanent and transient faults for safety-critical applications. CPU2 will be able to work in lock-step or or single-CPU mode. The lock-step feature is only available on certain device variants. Refer to the datasheet device comparison table for the device variants that can support lock-step. Consult the F28P65x Technical Reference Manual for the full details of the Lock-step Comparator Module

3.1.2 Expanded Analog Channels

The F28P65x ADC input multiplex has been expanded from 16 to 32 channels internally, allowing for more analog channels. With this expansion, several analog inputs are routed to the ADC input multiplex on different ADC modules, which can be used for redundant conversions on another ADC for safety applications.

3.1.3 Firmware Update (FWU)

The F28P65x device has in-built hardware to facilitate firmware updates. It supports fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

3.1.4 Flexible GPIO and Digital Input Pins

The F28P65x device has up to 22 General-Purpose Input/Output (GPIO) pins that are shared with analog channels. There are 14 analog channels that can be used as digital input channels.

3.1.5 ADC Hardware Redundancy Safety Checker

Configurable hardware tiles snoop on selected ADC results registers and compare these with a values set in tolerance registers with out-of-tolerance events aggregated by the CPU and mapped to the ePIE for interrupt events. Events from individual tiles are also routed to the XBAR. ADC Safety Checker runs in the background and does not require extra CPU cycles to execute.

3.1.6 Flexible Memory Sharing between CPU Subsystems

In F2837x, device variants have fixed FLASH and RAM sizes allocated per CPU. In F28P65x, FLASH and RAM size allocation per CPU is configurable.

3.1.7 Increased RAM Program Memory on CLA

In F2837x and other devices, RAM program memory on CLA is limited to 32KB. In F28P65x, there is an additional program memory of 32KB that is only accessible to CLA making the overall CLA program memory to 64KB.

3.2 Communication Module Changes

Communication module changes between the F2837x and F28P65x devices affect the number of modules. Module functionality is maintained for both devices. Table 3-1 shows the module instances and differences which should be considered when migrating applications between F2837x and F28P65x.

Table 3-1. Communication Module Instances

Module	Category	F2837x	F28P65x	Notes
SCI	Number	4 - SCIA, SCIB, SCIC, SCID	2 - SCIA, SCIB	
I2C	Number	2 - I2CA, I2CB	2 - I2CA, I2CB	
LIN	Number	not present	2 - LINA, LINB	
CAN	Number	2 - CANA, CANB	1 - CANA	
CAN-FD	Number	not present	1 - MCANA	
McBSP	Number	2 -MCBSPA, MCBSPB	not present	
SPI	Number	4 - SPIA, SPIB, SPIC, SPID	4 - SPIA, SPIB, SPIC, SPID	
EMIF	Number	2 - EMIF1, EMIF2	1 - EMIF1	
USB	Number	1 - USBA	1 - USBA	
uPP	Number	1 - uPP	not present	
FSI	Number	not present	4 - FSIRXA..D,2 - FSITXA, FSITXB	

3.3 Control Module Changes

There are changes in the control modules between the F2837x and F28P65x devices. The biggest changes come from the EPWM and ECAP on the F28P65x device. Table 3-2 shows the module instances differences which should be considered when migrating applications between F2837x and F28P65x.

Table 3-2. Control Module Differences

Module	Category	F2837x	F28P65x	Notes
SDFM	Number	8 - SD1_D1C1..D4C4, SD2_D1C1..D4C4	16 - SD1_D1C1..D4C4, SD2_D1C1..D4C4, SD3_D1C1..D4C4,SD4_D1C1..D4C4	
	Registers	SDIFLG.MIF		MIF description updated to "Main" Interrupt Flag on F28P65x
		SDIFLGCLR.MIF		MIF description updated to "Main" Interrupt Flag on F28P65x
		SDCTL.MIE		MIE description updated to "Main" SDy_ERR Interrupt enable on F28P65x
		SDMFILEN.MFE		SDMFILEN description updated to SD "Main" Filter Enable on F28P65x. MFE description updated to "Main" Filter Enable on F28P65x
eQEP	Number	3 - EQEP1..3	6 - EQEP1..6	
	Registers	REV.MINOR=1	REV.MINOR=2	
		QEPSRCSEL		More input options on F28P65x
eCAP	Number	6- ECAP1..6	7 - ECAP1..7	
	Registers	ECCTL0.INPUTSEL[0..6]	ECCTL0.INPUTSEL[0..7]	
		-	ECCTL0.QUALPRD	Qualification period for noise filtering
		-	ECCTL0.SOCEVTSEL	ADC SOC event select
		ECCTL2.DMAEVTSEL		APWM mode triggering added on F28P65x
		-	ECEINT.MUNIT_1..2_ERROR_EVT1..2	Monitoring unit error event interrupt enable
		-	ECFLG.MUNIT_1..2_ERROR_EVT1..2	Monitoring unit error event interrupt flag
		-	ECCLR.MUNIT_1..2_ERROR_EVT1..2	Monitoring unit error event interrupt flag clear
		-	ECFRC.MUNIT_1..2_ERROR_EVT1..2	Monitoring unit error event interrupt flag force
		ECAPSYNCINSEL		More input options on F28P65x
	Other	-	Additional signal monitoring functionality with new registers : ECAP_SIGNAL_MONITORING	
HRCAP	Number	2 - HRCAP5, HRCAP6	2 - HRCAP6, HRCAP7	

Table 3-2. Control Module Differences (continued)

Module	Category	F2837x	F28P65x	Notes
ePWM	Number	12 - EPWM1..12	18 - EPWM1..18	
	Registers	EPWMSYNCINSEL		More EPWMxSYNCI options on F28P65x
		-	CMPCTL.LINKDUTYHR	CMPAHR, CMPBHR Register Linking
		GLDCTL.GLDMODE		Extra options on F28P65x=> 1000:Load on Counter=CMPCU, 1001:Load on Counter=CMPCD, 1010:Load on Counter=CMPDU, 1011:Load on Counter=CMPDD
		EPWMXLINK		4-bit fields on F2837x to corresponding 5-bit fields on F28P65x
		-	TZEINT.CAPEVT	Capture Event Interrupt Enable
		-	TZFLG.CAPEVT	Capture Event Flag
		-	TZCBCFLG.CAPEVT	Cycle-By-Cycle Capture Event Flag
		-	TZOSTFLG.CAPEVT	One-Shot Capture Event Flag
		-	TZCLR.CAPEVT	Capture Event Clear
		-	TZCBCCLR.CAPEVT	Cycle-By-Cycle Capture Event Clear
		-	TZOSTCLR.CAPEVT	One-Shot Capture Event Clear
		-	TZFRC.CAPEVT	Force Capture Event
		ETSEL.INTSEL		Value 011 is ETINTMIX on F28P65x and TBCTR=0| PRD on F2837x
		ETSEL.SOCASEL		Value 011 is ETSOCAMIX on F28P65x and TBCTR=0| PRD on F2837x
		ETSEL.SOCBSEL		Value 011 is ETSOCBMIX on F28P65x and TBCTR=0| PRD on F2837x
		DCFCTL.PULSESEL		Value 11 is BLANKPULSEMIX on F28P65x
		-	HRCNFG.HRLOAD	Value 11 is CMPA_EQ on F28P65x
		-	HRCNFG.HRLOADB	Value 11 is CMPB_EQ on F28P65x
		EPWM_REGS.HRPWR	OTTOCAL_REGS.HRPWR	HRPWM Power Register
		EPWM_REGS.HRMSTEP	OTTOCAL_REGS.HRMSTEP	HRPWM MEP Step Register
		-	EPWMXLINK2	EPWMx Link 2 Register
		-	TZSEL2	Trip Zone Select Register 2
		-	TZTRIPOUTSEL	Trip Out Select Register
		-	ETINTMIXEN	Event-Trigger Mixed INT Selection Register
		-	ETSOCAMIXEN	Event-Trigger Mixed SOCA Selection Register
		-	ETSOCBMIXEN	Event-Trigger Mixed SOCB Selection Register
		-	BLANKPULSEMIXSEL	Blanking Window Trigger Pulse Selec Register
		-	DCCAPMIXSEL	Capture Event Pulse Select Register
		-	CAPCTL	Event Capture Control Register
		-	CAPGATETRIPSEL	Event Capture Gate Trip Input Select Register
		-	CAPINTRIPSEL	Event Catpure Trip Input Select Register
		-	CAPTRIPSEL	Event Capture Signal Select Register
		-	EPWM_XCMP_REGS	XCMP Registers
		-	DE_REGS	Diode Emulation Registers
		-	MINDB_LUT_REGS	Minimum Dead Band and Look-Up Table Registers
HRPWM	Number	8 - HRPWM1..8	18 - HRPWM1..18	
	Clock Source	EPWM1CLK	Respective EPWM	

3.4 Analog Module Differences

This section outlines the analog differences between F2837x and F28P65x. The ADC on F28P65x has a lot of new features compared to the ADC on F2837x. Table 3-3 shows the differences.

Table 3-3. Analog Module Differences

Module	Category	F2837x	F28P65x	Notes
ASUBSYS	Registers	ANAREFTRIMD	-	Analog Reference Trim D Register
		-	ANAREFCTL	Analog Reference Control Register
		-	VMONCTL	Voltage Monitor Control Register
		-	CMPHPMXSEL	Comparator High Positive Mux Select Register
		-	CMPLPMXSEL	Comparator Low Positive Mux Select Register
		-	CMPHNMXSEL	Comparator High Negative Mux Select Register
		-	CMPLNMXSEL	Comparator Low Negative Mux Select Register
		-	ADCDACLOOPBACK	DAC to ADC Loopback Register
		-	AGPIOCTRLG	AGPIO Control Register
		-	AGPIOCTRLH	AGPIO Control Register
		-	CMPHPMXSEL1	Comparator High Positive Mux Select Register
		-	CMPLPMXSEL1	Comparator Low Positive Mux Select Register
		-	ADCSOCFRCGB	ADC Global SOC Force Register
		-	ADCSOCFRCGBSEL	ADC Global SOC Force Select Register
		LOCK		Additional Lock Fields for New Registers in F28P65x

Table 3-3. Analog Module Differences (continued)

Module	Category	F2837x	F28P65x	Notes
ADC [1]	Number	4 - ADCA to ADCD	3 - ADCA to ADCC	
	Max Speed	50 MHz		
	Registers	-	ADCCTL1.EXTMUXPRESELECTEN	External Mux Preselect Enable
		-	ADCCTL1.TDMAEN	Enable Alternate DMA Timings
		-	ADCCTL2.OFFTRIMMODE	Offset Trim Mode
		ADCBURSTCTL.BURSTTRIGSEL[5..0]	ADCBURSTCTL.BURSTTRIGSEL[6..0]	
		-	ADCINTFLG.ADCINTxRESULT	ADC Interrupt Results Ready
		ADCINTFLGCLR		Clears respective flag bit in ADCINTFLG register on F28P65x
		ADCINTSEL1N2.INT1SEL[3..0]	ADCINTSEL1N2.INT1SEL[4..0]	New OSINT Options on F28P65x
		ADCINTSEL1N2.INT2SEL[3..0]	ADCINTSEL1N2.INT2SEL[4..0]	
		ADCINTSEL3N4.INT1SEL[3..0]	ADCINTSEL3N4.INT1SEL[4..0]	
		ADCINTSEL3N4.INT2SEL[3..0]	ADCINTSEL3N4.INT2SEL[4..0]	
		ADCSOCxCTL.CHSEL[18..15]	ADCSOCxCTL.CHSEL[19..15]	
		ADCSOCxCTL.TRIGSEL[25..20]	ADCSOCxCTL.TRIGSEL[26..20]	
		-	ADCSOCxCTL.EXTCHSEL	SOC External Channel Mux Select
		ADCOFFTRIM.OFFTRIM		F28P65x - ADC Offset Trim 12B SE Even
		-	ADCOFFTRIM.OFFTRIM12BSEODD	ADC Offset Trim 12B SE Odd
		-	ADCPPBxCONFIG.ABSEN	ADC Post Processing Block Absolute Enable
		ADCPPBxOFFCAL		F28P65x - OFFCAL of the lowest numbered PPB will be applied if multiple PPBs point to the same SOC.
		ADCPPBxTRIPHI.LIMITHI[15..0]	ADCPPBxTRIPHI.LIMITHI[23..0]	
		ADCPPBxTRIPHI.HSIGN	-	High Limit Sign Bit
		-	ADCPPBxTRIPLO.LIMITLO2EN	Extended Low Limit 2 Enable

Table 3-3. Analog Module Differences (continued)

Module	Category	F2837x	F28P65x	Notes
ADC (1)	Registers	ADCPPBxRESULT		Updates related to ADCINTFLG on F28P65x
		-	ADCOFFTRIM2	ADC Offset Trim Register
		-	ADCOFFTRIM3	ADC Offset Trim Register
		-	ADCSAFECHECKRESEN	ADC Safe Check Result Enable Register
		-	ADCREV2	ADC Wrapper Revision Register
		-	REPxCTL	ADC Trigger Repeater Control Register
		-	REPxN	ADC Trigger Repeater N Select Register
		-	REPxPHASE	ADC Trigger Repeater Phase Select Register
		-	REPxSPREAD	ADC Trigger Repeater Spread Select Register
		-	REPxFRC	ADC Trigger Repeater Software Force Register
		-	ADCPPBxLIMIT	ADC PPB Conversion Count Limit Register
		-	ADCPPBPxPCOUNT	ADC PPB Partial Conversion Count Register
		-	ADCPPBxCONFIG2	ADC PPB Sum Shift Register
		-	ADCPPBxPSUM	ADC PPB Partial Sum Register
		-	ADCPPBxPMAX	ADC PPB Partial Max Register
		-	ADCPPBxPMAXI	ADC PPB Partial Max Index Register
		-	ADCPPBxPMIN	ADC PPB Partial Min Register
		-	ADCPPBxPMINI	ADC PPB Partial Min Index Register
		-	ADCPPBxTRIPLO2	ADC PPB Extended Trip Low Register
		-	ADCPPBxSUM	ADC PPB Final Sum Result Register
		-	ADCPPBxCOUNT	ADC PPB Final Conversion Count Register
		-	ADCPPBxMAX	ADC PPB Final Max Result Register
		-	ADCPPBxMAXI	ADC PPB Final Max Index Result Register
		-	ADCPPBxMIN	ADC PPB Final Min Result Register
		-	ADCPPBxMINI	ADC PPB Final Min Index Result Register
		-	ADC_SAFECHECK_REGS	ADC Safety Check Registers
		-	ADC_SAFECHECK_INTEVT_REGS	ADC Safety Check Interrupt & Event Registers
GPDAC	Number	3 - GPDACA, GPDACB, GPDACC	2 - GPDACA, GPDACC	
	Registers	-	DACCTL.MODE	Gain Mode Select
		DACCTL.SYNCSEL[7..4]	DACCTL.SYNCSEL[8..4]	

Table 3-3. Analog Module Differences (continued)

Module	Category	F2837x	F28P65x	Notes
CMPSS (1)	Number	8 - CMPSS1 to CMPSS8	11 - CMPSS1 to CMPSS11	
	Registers	-	COMPDACHCTL.RAMPDIR	High Ramp Generator Direction
		COMPDACCTL	COMPDACHCTL	Name change on F28P65x to accommodate dual up/down ramp generators.
		RAMPMAXREFA	RAMPHREFA	
		RAMPMAXREFA.RAMPMAXREF	RAMPHREFA.RAMPHREF	
		RAMPMAXREFS	RAMPHREFS	
		RAMPMAXREFS.RAMPMAXREF	RAMPHREFS.RAMPHREF	
		RAMPDECVALA	RAMPHSTEPVALA	
		RAMPDECVALA.RAMPDECVAL	RAMPHSTEPVALA.RAMPHSTEPVAL	
		RAMPDECVALS	RAMPHSTEPVALS	
		RAMPDECVALS.RAMPDECVAL	RAMPHSTEPVALS.RAMPHSTEPVAL	
		RAMPSTS	RAMPHSTS	
		RAMPSTS.RAMPVALUE	RAMPHSTS.RAMPHVALUE	
		CTRIPxFILCLKCTL.CLKPRESCALE[9..0]	CTRIPxFILCLKCTL.CLKPRESCALE[15..0]	CMPSS filter prescaling size increased on F28P65x
		CTRIPxFILCTL.SAMPWIN[8..4]	CTRIPxFILCTL.SAMPWIN[8..3]	CMPSS filter sample window size increased on F28P65x
		CTRIPxFILCTL.THRESH[13..9]	CTRIPxFILCTL.THRESH[14..9]	CMPSS filter threshold size increased on F28P65x
		-	CTRIPxFILCTL.FILTINSEL	Filter input mux select
		-	COMPDACHCTL2	CMPSS High DAC Control Register 2
		-	RAMPHCTLA	CMPSS High Ramp Control Active Register
		-	RAMPHCTLS	CMPSS High Ramp Control Shadow Register
		-	DACHVALS2	CMPSS High DAC Value Shadow Register 2
		-	DACLVALS2	CMPSS Low DAC Value Shadow Register 2
		-	COMPDACLCTL	CMPSS Low DAC Control Register
		-	COMPDACLCTL2	CMPSS Low DAC Control Register 2
		-	RAMPLREFA	CMPSS Low Ramp Reference Active Register
		-	RAMPLREFS	CMPSS Low Ramp Reference Shadow Register
		-	RAMPLSTEPVALA	CMPSS Low Ramp Step Value Active Register
		-	RAMPLCTLA	CMPSS Low Ramp Control Active Register
		-	RAMPLSTEPVALS	CMPSS Low Ramp Step Value Shadow Register
CMPSS (1)	Registers	-	RAMPLCTLS	CMPSS Low Ramp Control Shadow Register
		-	RAMPLSTS	CMPSS Low Ramp Status Register
		-	RAMPLDLYA	CMPSS Low Ramp Delay Active Register
		-	RAMPLDLYS	CMPSS Low Ramp Delay Shadow Register
		-	CTRIPLFILCLKCTL2	CTRIPL Filter Clock Control Register 2
		-	CTRIPHFILCLKCTL2	CTRIPH Filter Clock Control Register 2
Temp Sensor	Number	1 - (in ADCA ch 13)	1 - (in ADCB ch 18)	

(1) In porting software from F2837x to F28P65x (or the other way around), care must be taken to ensure that the correct ADC channels are used because of a difference in channel assignment, see Section 3.9.

3.5 Other Device Changes

This section describes feature differences between F2837x and F28P65x that were not covered in the previous sections, as such the changes identified below must be considered when migrating applications between devices.

3.5.1 PIE Channel Mapping

Pie channel mapping between F2837x and F28P65x is different due to peripheral module changes between these devices. Section 3.5.1.1summarizes the common and unique pie channel assignments on these two devices.

3.5.1.1 F2837x vs F28P65x PIE Channel Mapping Comparison

Table 3-4. Pie Overlay Legend

Color	Description
	common for both devices
	applicable only for F2837x
	applicable only for F28P65x
	different between devices, F2837x listed on first row and F28P65x in second row

Table 3-5. Pie Channel Mapping Overlay

	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT1.y	ADCA1	ADCB1	ADCC1	XINT1	XINT2	ADCD1	TIMER0	WAKE --> WAKE/WDINT	I2CA	SYS_ERR	ECATSYNC0	ECATINTn	CIPC0	CIPC1	CIPC2	CIPC3
INT2.y	EPWM1_TZ	EPWM2_TZ	EPWM3_TZ	EPWM4_TZ	EPWM5_TZ	EPWM6_TZ	EPWM7_TZ	EPWM8_TZ	EPWM9_TZ	EPWM10_TZ	EPWM11_TZ	EPWM12_TZ	EPWM13_TZ	EPWM14_TZ	EPWM15_TZ	EPWM16_TZ
INT3.y	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	EPWM7	EPWM8	EPWM9	EPWM10	EPWM11	EPWM12	EPWM13	EPWM14	EPWM15	EPWM16
INT4.y	ECAP1	ECAP2	ECAP3	ECAP4	ECAP5	ECAP6	ECAP7		FSITXA1	FSITXA2	FSITXB1	FSITXB2	FSIRXA1	FSIRXA2	FSIRXB1	FSIRXB2
INT5.y	EQEP1	EQEP2	EQEP3	EQEP4	CLB1	CLB2	CLB3	CLB4	SDFM1	SDFM2	ECATRST	ECATSYNC1	SDFM1DR1	SDFM1DR2	SDFM1DR3	SDFM1DR4
INT6.y	SPIA_RX	SPIA_TX	SPIB_RX	SPIB_TX	MCBSPA_RX --> LINA_0	MCBSPA_TX --> LINA_1	MCBSPB_RX --> LINB_0	MCBSPB_TX --> LINB_1	SPIC_RX	SPIC_TX	SPID_RX	SPID_TX	SDFM2DR1	SDFM2DR2	SDFM2DR3	SDFM2DR4
INT7.y	DMA_CH1	DMA_CH2	DMA_CH3	DMA_CH4	DMA_CH5	DMA_CH6	EQEP5	EQEP6	FSIRXC1	FSIRXC2	FSIRXD1	FSIRXD2	SDFM3DR1	SDFM3DR2	SDFM3DR3	SDFM3DR4
INT8.y	I2CA	I2CA_FIFO	I2CB	I2CB_FIFO	SCIC_RX --> UART0_INT	SCIC_TX --> UART1_INT	SCID_RX --> EPWM17_TZ	SCID_TX --> EPWM18_TZ			SDFM3	SDFM4	CLB5	CLB6	UPPA	
INT9.y	SCIA_RX	SCIA_TX	SCIB_RX	SCIB_TX	CANA_0 --> CANA0	CANA_1 --> CANA1	CANB_0 --> EPWM17	CANB_1 --> EPWM18	MCANSS-A0	MCANSS-A1	MCANSS-A_ECC_CORR_PLS	MCANSS-A_WAKE_AND_TS_PLS	PMBUSA	AESINT	USBA	
INT10.y	ADCA_EVT	ADCA2	ADCA3	ADCA4	ADCB_EVT	ADCB2	ADCB3	ADCB4	ADCC_EVT	ADCC2	ADCC3	ADCC4	ADCD_EVT	ADCD2	ADCD3	ADCD4 --> ADCCHECKINT
INT11.y	CLA1_1	CLA1_2	CLA1_3	CLA1_4	CLA1_5	CLA1_6	CLA1_7	CLA1_8	MCANSS-B0	MCANSS-B1	MCANSS-B_ECC_CORR_PLS	MCANSS-B_WAKE_AND_TS_PLS	SDFM4DR1	SDFM4DR2	SDFM4DR3	SDFM4DR4

Table 3-5. Pie Channel Mapping Overlay (continued)

	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT12.y	XINT3	XINT4	XINT5	MPOST	FLSS_INT	VCU	FPU_OFLOW	FPU_UFLOW	EMIF_ERROR	RAM_CORRECTABLE_ERROR --> ECAP6_2	FLASH_CORRECTABLE_ERROR --> ECAP7_2	RAM_ACCESS_VIOLATION	SYS_PLL_SLIP --> CPUCRC	AUX_PLL_SLIP --> CLA1CRC	CLA_OVERFLOW	CLA_UNDERFLOW

3.5.2 Bootrom

For bootrom similarities and differences between F2837x and F28P65x see Table 3-6 and Table 3-9.

Table 3-6. Bootrom Comparison Table

		F2837x	F28P65x
Initiate Boot Process		CPU1: Device Reset; CPU2: CPU1 Application	
GPIO Boot Mode Selection		Supported only in CPU1	
IPC Boot Mode selection		Supported in CPU2	Supported in CPU2
Boot Modes	Flash	Supported in CPU1,CPU2	Supported in CPU1, CPU2
	Secure Flash	Supported in CPU1,CPU2	Supported in CPU1, CPU2
	RAM	Supported in CPU1,CPU2	Supported in CPU1, CPU2
	OTP	Supported in CPU2	Supported in CPU2
	Copy from IPC message RAM to local RAM	CPU1: No CPU2: CPU1TOCPU2MSGRAM1 CM: CPU1TOCMMSGRAM1	CPU1: No CPU2: CPU1TOCPU2MSGRAM1
Boot Loader Support		CPU1: I2C,CAN,SPI,SCI,Parallel,USB	CPU1: I2C,CAN,MCAN,SPI,SCI,Parallel, USB, and FWU
ROM Contents		AES tables and Motor Control Library is included	AES tables and Motor Control Library are excluded
PLL Option		No option to switch PLL during CPU1 boot	Option to switch PLL during CPU1 boot
Lockstep Initialization		Lockstep not available	Lockstep initialization performed in CPU2 boot code
MPOST		Can execute at 110MHz, 80MHz and 60MHz PLL output clock	Can execute at 150MHz, 75MHz PLL output clock as well as INTOSC clock

Table 3-7. Boot Options Legend

Color	Description
	Options common for both devices but BOOTDEFx values may differ
	Options applicable only for F2837x
	Options applicable only for F28P65x

Table 3-8. Bootloaders and GPIO Assignment Comparison

Bootloader	Option	BOOTDEFx	F2837x	F28P65x
Parallel	0	0x00	D0-D7=89,90,58-62,88; DSP=91; Host=92	D0-D7=0 to 7; DSP=10; Host=11
	1	0x20	n/a	D0-D7=89,90,58-62,88; DSP=91; Host=92
SCIA	0	0x01	TX=29; RX=28	TX=12; RX=13
	1	0x21	TX=84; RX=85	TX=84; RX=85
	2	0x41	TX=36; RX=35	TX=36; RX=35
	3	0x61	TX=42; RX=43	TX=42; RX=43
	4	0x81	TX=65; RX=64	TX=65; RX=64
	5	0xA1	TX=135; RX=136	TX=29; RX=28
	6	0xC1	TX=8; RX=9	TX=8; RX=9
CAN	0	0x02	TX=37; RX=36	TX=4; RX=5
	1	0x22	TX=71; RX=70	TX=19; RX=18
	2	0x42	TX=63; RX=62	TX=31; RX=30
	3	0x62	TX=19; RX=18	TX=37; RX=36
	4	0x82	TX=4; RX=5	TX=63; RX=62
	5	0xA2	TX=31; RX=30	TX=71; RX=70

Table 3-8. Bootloaders and GPIO Assignment Comparison (continued)

Bootloader	Option	BOOTDEFx	F2837x	F28P65x
MCAN	0	0x08	n/a	TX=4; RX=5
	1	0x18	n/a	TX=8; RX=10
	2	0x28	n/a	TX=19; RX=18
	3	0x38	n/a	TX=71; RX=70
	4	0x48	n/a	TX=74; RX=75
SPI	0	0x06	SIMO=58; SOMI=59; CLK=60; STE=61	PICO=58; POCI=55; CLK=56; PTE=57
	1	0x26	SIMO=16; SOMI=17; CLK=18; STE=19	PICO=202; POCI=203; CLK=204; PTE=205
	2	0x46	SIMO=32; SOMI=33; CLK=34; STE=35	PICO=16; POCI=17; CLK=18; PTE=19
	3	0x66	SIMO=16; SOMI=17; CLK=56; STE=57	PICO=58; POCI=59; CLK=34; PTE=35
	4	0x86	SIMO=54; SOMI=55; CLK=56; STE=57	n/a
I2C	0	0x07	SDA=91; SCL=92	SDA=0; SCL=1
	1	0x27	SDA=32; SCL=33	SDA=42; SCL=43
	2	0x47	SDA=42; SCL=43	SDA=91; SCL=92
	3	0x67	SDA=0; SCL=1	SDA=104; SCL=105
	4	0x87	SDA=104; SCL=105	n/a
USB	0	0x09	DM=42; DP=43	DM=42; DP=43

Table 3-9. Boot Modes Comparison

Boot Mode	Option	BOOTDEFx	F2837x	F28P65x
Flash	0	0x03	CPU1: Entry=0x00080000;	CPU1/CPU2: Entry=0x00080000;
	1	0x23	CPU1: Entry=0x00088000;	CPU1/CPU2: Entry=0x0009FFF0;
	2	0x43	CPU1: Entry=0x000A8000;	CPU1/CPU2: Entry=0x000A0000;
	3	0x63	CPU1: Entry=0x000BE000;	CPU1/CPU2: Entry=0x000C0000;
	4	0x83	-	CPU1/CPU2: Entry=0x000E0000;
	5	0xA3	-	CPU1/CPU2: Entry=0x00100000;
	6	0xC3	-	CPU1/CPU2: Entry=0x0011FFF0;
Secure Flash	0	0x0A	CPU1: Entry=0x00080000;	CPU1/CPU2: Entry=0x00080000;
	1	0x2A	CPU1: Entry=0x00088000; Bank/ Sector=0/4	-
	2	0x4A	CPU1: Entry=0x000A8000;	CPU1/CPU2: Entry=0x000A0000;
	3	0x6A	CPU1: Entry=0x000BE000;	CPU1/CPU2: Entry=0x000C0000;
	4	0x8A	-	CPU1/CPU2: Entry=0x000E0000;
	5	0xAA	-	CPU1/CPU2: Entry=0x00100000;
CPU1 FWU Flash	0	0x0B	-	Entry=0x00080000; Bank=0 Entry=0x000A0000; Bank=1 Entry=0x000C0000 Bank=2 Entry=0x000E0000 Bank=3 Entry=0x00100000 Bank=4
	1	0x2B	-	Entry=0x0008FFF0; Bank=0 Entry=0x000AFFF0; Bank=1 Entry=0x000CFFF0 Bank=2 Entry=0x000EFFF0 Bank=3 Entry=0x0010FFF0 Bank=4
	2	0x4B	-	Entry=0x00090000; Bank=0 Entry=0x000B0000; Bank=1 Entry=0x000D0000 Bank=2 Entry=0x00F0000 Bank=3 Entry=0x00110000 Bank=4
	3	0x6B	-	Entry=0x0009FFF0; Bank=0 Entry=0x000BFFF0; Bank=1 Entry=0x000DFFF0 Bank=2 Entry=0x000FFFF0 Bank=3 Entry=0x0011FFF0 Bank=4

Table 3-9. Boot Modes Comparison (continued)

Boot Mode	Option	BOOTDEFx	F2837x	F28P65x
CPU2 FWU Flash	0	0x06	-	Entry=0x00080000; Bank=0 Entry=0x000A0000; Bank=1 Entry=0x000C0000 Bank=2 Entry=0x000E0000 Bank=3 Entry=0x00100000 Bank=4
	1	0x26	-	Entry=0x0008FFF0; Bank=0 Entry=0x000AFFF0; Bank=1 Entry=0x000CFFF0 Bank=2 Entry=0x000EFFF0 Bank=3 Entry=0x0010FFF0 Bank=4
	2	0x46	-	Entry=0x00090000; Bank=0 Entry=0x000B0000; Bank=1 Entry=0x000D0000 Bank=2 Entry=0x00F0000 Bank=3 Entry=0x00110000 Bank=4
	3	0x66	-	Entry=0x0009FFF0; Bank=0 Entry=0x000BFFF0; Bank=1 Entry=0x000DFFF0 Bank=2 Entry=0x000FFFF0 Bank=3 Entry=0x0011FFF0 Bank=4
Wait	0	0x04	Watchdog enabled	Watchdog enabled
	1	0x24	Watchdog disabled	Watchdog disabled
RAM	0	0x05	Entry=0x00000000	Entry=0x00000000

3.5.3 AGPIO Filter

F28P65x has 11 channels on 100PZ and 22 channels on the higher pin count packages that support both normal GPIO and AGPIO (analog) pin functionality. AGPIO functionality is not available on F2837x. Table 3-10 summarizes how to configure the AGPIO channels on the F28P65x device.

Table 3-10. AGPIO Configuration for GPIOy

AGPIO\GPIO Register Settings	GPxAMSEL.GPIOy='0'	GPIOxAMSEL.GPIOy='1'<default setting>
AGPIOCTRLx.GPIOy='0'<default setting>	GPIOy	-
AGPIOCTRLx.GPIOy='1'	GPIOy	Analog

In order to help reduce noise for the analog portion of AGPIO pins, a configurable filter is available. This filter can be enabled and configured in two banks. For more details on the two groups of AGPIO filters and configuration options available, please see the AGPIO and ANALOG_SUBSYS_REGS section in the device Technical Reference Manual.

3.6 Power Management

This section describes the power management differences and similarities between the two devices.

3.6.1 VREGENZ

F2837x and F28P65x supports both external and internal VREG mode which is selectable with VREGENZ pin. VREGENZ pin in F2837x device has an internal pulldown resistor. Left floating, the VREGENZ in F2837x device activates the internal VREG. In F28P65x device, the VREGENZ has an internal pullup resistor which disables the internal VREG and sets up the device for external VREG operation.

3.6.2 POR/BOR

There are no functional changes for the POR on F2837x and F28P65x. BOR (I/O BOR) is a new feature in F28P65x.

3.6.3 Power Consumption

There is not a significant difference in power consumption between F2837x and F28P65x if the same number of peripherals are being utilized while F28P65x is operating in external VREG mode..

3.7 Memory Module Changes

RAM and FLASH memories in F2837x and F28P65x devices have some similarities and differences. Table 3-11 summarizes the memory features including error-checking and security assignment.

Table 3-11. RAM and FLASH Memory Changes

Memory		F2837x			F28P65x		
		Size	**Parity/ ECC**	**Secured**	**Size**	**Parity/ ECC**	**Secured**
RAM	Dedicated RAM	24KB	ECC		104KB	Parity	
	Local Shared RAM	48KB	ECC	Yes	64KB	Parity	
	Global Shared RAM	128KB	Parity		80KB	Parity	
	CPU1,2 & Message RAM	4KB	ECC		4KB	Parity	
	C28 CPUs/CLA Message RAM	1KB	Parity		512B	Parity	
	DMA/CLA Message RAM	1KB	Parity		512B	Parity	
	Total RAM	**206KB**			**249KB**		
FLASH	Per C28 Bank	256KB(2 banks per CPU x 2 C28 CPUs)	ECC	DCSM-controlled	256KB(5 banks mappable between 2 C28 CPUs)	ECC	DCSM-controlled
	Total FLASH	**1.0MB**			**1.28MB**		

3.8 GPIO Multiplexing Changes

Section 3.8 outlines the differences and similarties that exist in the GPIO mux between F2837x and F28P65x. Section 3.8.1 outlines the GPIO changes.

3.8.1 F2837x vs F28P65x GPIO Mux Comparison

Table 3-12. GPIO Mux Legend

Color	Description
	common for both devices
	applicable only for F2837x
	applicable only for F28P65x
	different between devices, F2837x listed on first row and F28P65x in second row

Table 3-13. GPIO Mux Overlay Table

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1_A			CLB_OUTPUTXBAR1	I2CA_SDA		EMIF1_A13	ESC_GPI0		FSITXA_D0			
GPIO1	EPWM1_B		MFSRB	CLB_OUTPUTXBAR2	I2CA_SCL		EMIF1_A14	ESC_GPI1		FSITXA_D1			
GPIO2	EPWM2_A			OUTPUTXBAR1	I2CB_SDA	UARTA_TX	EMIF1_A15	ESC_GPI2		FSITXA_CLK			
GPIO3	EPWM2_B	OUTPUTXBAR2	MCLKRB	OUTPUTXBAR2	I2CB_SCL	UARTA_RX		ESC_GPI3		FSIRXA_D0			
GPIO4	EPWM3_A			OUTPUTXBAR3	CANA_TX		MCANA_TX	ESC_GPI4		FSIRXA_D1			
GPIO5	EPWM3_B	MFSRA	OUTPUTXBAR3	CLB_OUTPUTXBAR3	CANA_RX		MCANA_RX	ESC_GPI5		FSIRXA_CLK			
GPIO6	EPWM4_A	OUTPUTXBAR4	EXTSYNCOUT	EQEP3_A	CANB_TX --> MCANB_TX	LINA_TX	EMIF1_DQM0	ESC_GPI6		FSITXB_D0			
GPIO7	EPWM4_B	MCLKRA	OUTPUTXBAR5	EQEP3_B	CANB_RX --> MCANB_RX	LINA_RX	EMIF1_DQM1	ESC_GPI7		FSITXB_D1			
GPIO8	EPWM5_A	CANB_TX --> EMIF1_RAS	ADCSOCAO	EQEP3_STROBE	SCIA_TX	CLB_OUTPUTXBAR4	MCANA_TX	ESC_GPO0		FSITXB_CLK	FSITXA_D1	FSIRXA_D0	
GPIO9	EPWM5_B	SCIB_TX	OUTPUTXBAR6	EQEP3_INDEX	SCIA_RX			ESC_GPO1		FSIRXB_D0	FSITXA_D0	FSIRXA_CLK	
GPIO10	EPWM6_A	CANB_RX --> EMIF1_CAS	ADCSOCBO	EQEP1_A	SCIB_TX	SD4_C1	MCANA_RX	CLB_OUTPUTXBAR5	ESC_TX0_DATA0	FSIRXB_D1	FSITXA_CLK	UPP-WAIT --> FSIRXA_D1	
GPIO11	EPWM6_B	SCIB_RX	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SD4_D1		ESC_GPO3	ESC_TX0_DATA1	FSIRXB_CLK	FSIRXA_D1	UPP-START --> PMBUSA_ALERT	
GPIO12	EPWM7_A	CANB_TX --> CLB_OUTPUTXBAR6	MDXB --> ADCSOCAO	EQEP1_STROBE	SCIC_TX --> SCIA_TX	SD4_C2	EMIF1_A1	ESC_GPO4	ESC_TX0_DATA2	FSIRXC_D0	FSIRXA_D0	UPP-ENA --> PMBUSA_CTL	
GPIO13	EPWM7_B	CANB_RX --> CLB_OUTPUTXBAR7	MDRB --> EQEP5_STROBE	EQEP1_INDEX	SCIC_RX --> SCIA_RX	SD4_D2	EMIF1_CS0n	ESC_GPO5	ESC_TX0_DATA3	FSIRXC_D1	FSIRXA_CLK	UPP-D7 --> PMBUSA_SDA	
GPIO14	EPWM8_A	SCIB_TX	MCLKXB --> EQEP5_INDEX	LINA_TX	OUTPUTXBAR3	OUTPUTXBAR8		ESC_GPO6	ESC_PHY1_LINK STATUS	FSIRXC_CLK	EMIF1_D17	UPP-D6 --> PMBUSA_SCL	

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO15	EPWM8_B	SCIB_RX	MFSXB	LINA_RX	OUTPUTXBAR4	CLB_OUTPUTXBAR8		ESC_GPO7	EQEP5_A	FSIRXD_D0		UPP-D5 --> EMIF1_DQM2	
GPIO16	SPIA_SIMO --> SPIA_PICO	CANB_TX	OUTPUTXBAR7	EPWM9_A		SD1_D1			EQEP5_B	FSIRXD_D1		UPP-D4 --> ESC_RX1_CLK	
GPIO17	SPIA_SOMI --> SPIA_POCI	CANB_RX	OUTPUTXBAR8	EPWM9_B		SD1_C1			EQEP5_STROBE	FSIRXD_CLK		UPP-D3 --> ESC_RX1_DV	
GPIO18	SPIA_CLK	SCIB_TX	CANA_RX	EPWM10_A		SD1_D2	MCANA_RX	EMIF1_CS2n	EQEP5_INDEX			UPP-D2 --> ESC_RX1_ERR	
GPIO19	SPIA_STE --> SPIA_PTE	SCIB_RX	CANA_TX	EPWM10_B		SD1_C2	MCANA_TX	EMIF1_CS3n				UPP-D1 --> ESC_TX1_DATA3	
GPIO20	EQEP1_A	MDXA	CANB_TX	EPWM11_A		SD1_D3	MCANB_RX	EMIF1_BA0			SPIC_PICO	UPP-D0 --> ESC_TX1_DATA2	
GPIO21	EQEP1_B	MDRA	CANB_RX	EPWM11_B		SD1_C3	MCANB_TX	EMIF1_BA1			SPIC_POCI	UPP-CLK --> ESC_TX1_DATA1	
GPIO22	EQEP1_STROBE	MCLKXA	SCIB_TX	EPWM12_A	SPIB_CLK	SD1_D4	MCANA_TX	EMIF1_RAS			SPIC_CLK	ESC_TX1_DATA0	
GPIO23	EQEP1_INDEX	MFSXA	SCIB_RX	EPWM12_B	SPIB_STE --> SPIB_PTE	SD1_C4	MCANA_RX	EMIF1_CAS			SPIC_PTE	ESC_PHY_RESETn	
GPIO24	OUTPUTXBAR1	EQEP2_A	MDXB	LINB_TX	SPIB_SIMO --> SPIB_PICO	SD2_D1	PMBUSA_SCL	EMIF1_DQM0		EPWM13_A	ESC_RX0_DATA1	ESC_RX0_CLK	
GPIO25	OUTPUTXBAR2	EQEP2_B	MDRB	LINB_RX	SPIB_SOMI --> SPIB_POCI	SD2_C1	PMBUSA_SDA	EMIF1_DQM1	EQEP5_B	EPWM13_B	FSITXA_D1	ESC_RX0_DV	
GPIO26	OUTPUTXBAR3	EQEP2_INDEX	MCLKXB	OUTPUTXBAR3	SPIB_CLK	SD2_D2	PMBUSA_ALERT	EMIF1_DQM2	ESC_MDIO_CLK	EPWM14_A	FSITXA_D0	ESC_RX0_ERR	
GPIO27	OUTPUTXBAR4	EQEP2_STROBE	MFSXB	OUTPUTXBAR4	SPIB_STE --> SPIB_PTE	SD2_C2	PMBUSA_CTL	EMIF1_DQM3	ESC_MDIO_DATA	EPWM14_B	FSITXA_CLK	ESC_RX0_DATA0	
GPIO28	SCIA_RX	EMIF1_CS4n		OUTPUTXBAR5	EQEP3_A	SD2_D3	EMIF1_CS2n			EPWM15_A		ESC_RX0_DATA1	
GPIO29	SCIA_TX	EMIF1_SDCKE		OUTPUTXBAR6	EQEP3_B	SD2_C3	EMIF1_CS3n	ESC_LATCH0	ESC_I2C_SDA	EPWM15_B	ESC_SYNC0	ESC_RX0_DATA2	
GPIO30	CANA_RX	EMIF1_CLK	MCANA_RX	OUTPUTXBAR7	EQEP3_STROBE	SD2_D4	EMIF1_CS4n	ESC_LATCH1	ESC_I2C_SCL	EPWM16_A	ESC_SYNC1	SPID_PICO	
GPIO31	CANA_TX	EMIF1_WEn	MCANA_TX	OUTPUTXBAR8	EQEP3_INDEX	SD2_C4	EMIF1_RNW	I2CA_SDA		EPWM16_B		SPID_POCI	
GPIO32	I2CA_SDA	EMIF1_CS0n	SPIA_PICO	EQEP4_A	LINB_TX	CLB_OUTPUTXBAR1	EMIF1_OEn	I2CA_SCL				SPID_CLK	

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO33	I2CA_SCL	EMIF1_RNW	SPIA_POCI	EQEP4_B		CLB_OUTPUTXBAR2	EMIF1_BA0		ESC_LED_ERR			SPID_PTE	
GPIO34	OUTPUTXBAR1	EMIF1_CS2n	SPIA_CLK	EQEP4_STROBE	I2CB_SDA	CLB_OUTPUTXBAR3	EMIF1_BA1	ESC_LATCH0	EPWM18_A	SCIA_TX	ESC_SYNC0		
GPIO35	SCIA_RX	EMIF1_CS3n	SPIA_PTE	EQEP4_INDEX	I2CB_SCL	CLB_OUTPUTXBAR4	EMIF1_A0	ESC_LATCH1	EPWM18_B	SCIA_RX	ESC_SYNC1		
GPIO36	SCIA_TX	EMIF1_WAIT			CANA_RX	CLB_OUTPUTXBAR5	EMIF1_A1	MCANA_RX		SD1_D1	EMIF1_WEn		
GPIO37	OUTPUTXBAR2	EMIF1_OEn	EPWM18_A		CANA_TX	CLB_OUTPUTXBAR6	EMIF1_A2	MCANA_TX		SD1_D2	EMIF1_D24		
GPIO38		EMIF1_A0	EPWM18_B	SCIC_TX --> UARTA_TX	CANB_TX --> SCIB_TX	CLB_OUTPUTXBAR7	EMIF1_A3			SD1_D3	EMIF1_CS2n		
GPIO39		EMIF1_A1		SCIC_RX --> UARTA_RX	CANB_RX --> SCIB_RX	CLB_OUTPUTXBAR8	EMIF1_A4	ESC_MDIO_DATA	ESC_LED_RUN	SD1_D4	FSIRXD_CLK		
GPIO40		EMIF1_A2	EPWM13_A	MCANB_RX	I2CB_SDA	SD4_C3	ESC_GPO2	CLB_OUTPUTXBAR1		SD2_C1	ESC_I2C_SDA		
GPIO41		EMIF1_A3	EPWM13_B	MCANB_TX	I2CB_SCL	SD4_D3		CLB_OUTPUTXBAR2		SD2_D1	ESC_I2C_SCL	FSIRXD_CLK	
GPIO42			EPWM14_A	EQEP4_A	I2CA_SDA	SD4_C4		CLB_OUTPUTXBAR5	UARTA_TX		FSIRXD_D0	SCIA_TX	USB0DM
GPIO43			EPWM14_B	EQEP4_B	I2CA_SCL	SD4_D4		CLB_OUTPUTXBAR6	UARTA_RX		FSIRXD_D1	SCIA_RX	USB0DP
GPIO44	SPID_POCI	EMIF1_A4	MCANB_RX		SD3_C4	UARTB_TX		CLB_OUTPUTXBAR6		FSIRXD_CLK	ESC_TX1_CLK		
GPIO45	SPID_PTE	EMIF1_A5	MCANB_TX		SD3_D4	UARTB_RX		CLB_OUTPUTXBAR7			ESC_TX1_ENA		
GPIO46	EPWM4_A	EMIF1_A6	EPWM14_A		SCID_RX --> SCIA_RX	SD3_C4					ESC_MDIO_CLK		
GPIO47	EPWM4_B	EMIF1_A7	EPWM14_B		SCID_TX --> SCIA_TX	SD4_C3					ESC_MDIO_DATA		
GPIO48	OUTPUTXBAR3	EMIF1_A8			SCIA_TX	SD1_D1				SD2_C2	ESC_PHY_CLK		
GPIO49	OUTPUTXBAR4	EMIF1_A9			SCIA_RX	SD1_C1	EMIF1_A5			SD2_D1	FSITXA_D0		
GPIO50	EQEP1_A	EMIF1_A10	EPWM15_A		SPIC_SIMO --> SPIC_PICO	SD1_D2	EMIF1_A6		ESC_LATCH0	SD2_D2	FSITXA_D1		
GPIO51	EQEP1_B	EMIF1_A11	EPWM15_B		SPIC_SOMI --> SPIC_POCI	SD1_C2	EMIF1_A7		ESC_LATCH1	SD2_D3	FSITXA_CLK		
GPIO52	EQEP1_STROBE	EMIF1_A12	EPWM16_A		SPIC_CLK	SD1_D3	EMIF1_A8		ESC_MDIO_CLK	SD2_D4	FSIRXA_D0		
GPIO53	EQEP1_INDEX	EMIF1_D31	EMIF2_D15		SPIC_STE --> SPIC_PTE	SD1_C3	EMIF1_A9		ESC_MDIO_DATA	SD1_C1	FSIRXA_D1		
GPIO54	SPIA_SIMO --> SPIA_PICO	EMIF1_D30	EMIF2_D14	EQEP2_A	SCIB_TX	SD1_D4	EMIF1_A10		ESC_PHY_CLK	SD1_C2	FSIRXA_CLK		
GPIO55	SPIA_SOMI --> SPIA_POCI	EMIF1_D29	EMIF2_D13 --> EPWM16_B	EQEP2_B	SCIB_RX	SD1_C4	EMIF1_D0		ESC_PHY0_LINK STATUS	SD1_C3	FSITXB_D0		

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO56	SPIA_CLK	EMIF1_D28	EMIF2_D12 --> EPWM17_A	EQEP2_STROBE	SCIC_TX	SD2_D1	EMIF1_D1	I2CA_SDA	ESC_TX0_ENA	SD1_C4	FSITXB_CLK		
GPIO57	SPIA_STE --> SPIA_PTE	EMIF1_D27	EMIF2_D11 --> EPWM17_B	EQEP2_INDEX	SCIC_RX	SD2_C1	EMIF1_D2	I2CA_SCL	ESC_TX0_CLK	SD3_D3	FSITXB_D1		
GPIO58	MCLKRA --> SPIA_PICO	EMIF1_D26	EMIF2_D10 --> EPWM8_A	OUTPUTXBAR1	SPIB_CLK	SD2_D2	EMIF1_D3	ESC_LED_LINK0_ACTIVE	CANA_RX	SD2_C2	FSIRXB_D0	SPIA_SIMO --> SPIA_PICO	
GPIO59	MFSRA --> EPWM5_A	EMIF1_D25	EMIF2_D9 --> EPWM8_B	OUTPUTXBAR2	SPIB_STE --> SPIB_PTE	SD2_C2	EMIF1_D4	ESC_LED_LINK1_ACTIVE	CANA_TX	SD2_C3	FSIRXB_D1	SPIA_SOMI --> SPIA_POCI	
GPIO60	MCLKRB --> EPWM3_B	EMIF1_D24	EMIF2_D8 --> ESC_LATCH0	OUTPUTXBAR3	SPIB_SIMO --> SPIB_PICO	SD2_D3	EMIF1_D5	ESC_LED_ERR		SD2_C4	FSIRXB_CLK	SPIA_CLK	
GPIO61	MFSRB --> EPWM17_B	EMIF1_D23	EMIF2_D7 --> ESC_LATCH1	OUTPUTXBAR4	SPIB_SOMI --> SPIB_POCI	SD2_C3	EMIF1_D6	ESC_LED_RUN			CANA_RX	SPIA_STE --> SPIA_PTE	
GPIO62	SCIC_RX --> SCIA_RX	EMIF1_D22	EMIF2_D6 --> ESC_MDIO_CLK	EQEP3_A	CANA_RX	SD2_D4	EMIF1_D7	ESC_LED_STATE_RUN			CANA_TX		
GPIO63	SCIC_TX --> SCIA_TX	EMIF1_D21	EMIF2_D5 --> EPWM9_A	EQEP3_B	CANA_TX	SD2_C4	EMIF1_RNW	EMIF1_BA0		SD1_D1	ESC_RX1_DATA0	SPIB_SIMO --> SPIB_PICO	
GPIO64		EMIF1_D20	EMIF2_D4 --> EPWM9_B	EQEP3_STROBE	SCIA_RX		EMIF1_WAIT	EMIF1_BA1		SD1_C1	ESC_RX1_DATA1	SPIB_SOMI --> SPIB_POCI	
GPIO65		EMIF1_D19	EMIF2_D3 --> EPWM10_A	EQEP3_INDEX	SCIA_TX		EMIF1_WEn		FSITXB_CLK	SD1_D2	ESC_RX1_DATA2	SPIB_CLK	
GPIO66	EQEP6_B	EMIF1_D18	EMIF2_D2 --> EPWM10_B		I2CB_SDA		EMIF1_OEn		FSITXB_D1	SD1_C2	ESC_RX1_DATA3	SPIB_STE --> SPIB_PTE	
GPIO67		EMIF1_D17	EMIF2_D1 --> EPWM17_A	LINB_TX					ESC_I2C_SDA	SD1_D3			
GPIO68		EMIF1_D16	EMIF2_D0 --> EPWM17_B	LINB_RX					ESC_I2C_SCL	SD1_C3	ESC_PHY1_LINK STATUS		
GPIO69		EMIF1_D15	EPWM11_A		I2CB_SCL				FSITXB_D0	SD1_D4	ESC_RX1_CLK	SPIC_SIMO --> SPIC_PICO	
GPIO70		EMIF1_D14	EPWM11_B	CANA_RX	SCIB_TX	UARTB_TX	MCANA_RX		FSIRXB_D0	SD1_C4	ESC_RX1_DV	SPIC_SOMI --> SPIC_POCI	
GPIO71		EMIF1_D13	EPWM12_A	CANA_TX	SCIB_RX	UARTB_RX	MCANA_TX			SD3_D1	ESC_RX1_ERR	SPIC_CLK	
GPIO72	EQEP6_STROBE	EMIF1_D12	EPWM12_B	CANB_TX --> OUTPUTXBAR8	SCIC_TX --> UARTA_TX		MCANB_RX			SD3_C1	ESC_TX1_DATA3	SPIC_STE --> SPIC_PTE	
GPIO73	EQEP6_INDEX	EMIF1_D11	XCLKOUT	CANB_RX --> OUTPUTXBAR6	SCIC_RX --> UARTA_RX	EPWM5_B	MCANB_TX	SD4_D4		SD2_D2	ESC_TX1_DATA2		
GPIO74	EPWM8_A	EMIF1_D10			EQEP5_A		MCANA_TX	SD1_D4		SD2_C2	ESC_TX1_DATA1		

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO75	EPWM8_B	EMIF1_D9			EQEP5_B	SPID_CLK	MCANA_RX	CLB_OUTPUTXBAR8		SD2_D3	ESC_TX1_DATA0		
GPIO76	EPWM9_A	EMIF1_D8			SCID_TX --> EQEP5_STROBE	SD3_C1		SD4_D4		SD2_C3	ESC_PHY_RESETn		
GPIO77	EPWM9_B	EMIF1_D7			SCID_RX --> EQEP5_INDEX	SD3_D1		SD1_D4		SD2_D4	ESC_RX0_CLK		
GPIO78	EPWM10_A	EMIF1_D6			EQEP2_A	SD3_C2		SD4_D4		SD2_C4	ESC_RX0_DV		
GPIO79	EPWM10_B	EMIF1_D5		ERRORSTS	EQEP2_B	SD3_D2				SD2_D1	ESC_RX0_ERR		
GPIO80	EPWM11_A	EMIF1_D4		ERRORSTS	EQEP2_STROBE	SD3_C3		SD1_D4		SD2_C1	ESC_RX0_DATA0		
GPIO81	EPWM11_B	EMIF1_D3			EQEP2_INDEX	SD3_D3					ESC_RX0_DATA1		
GPIO82	EPWM12_A	EMIF1_D2								SD3_C2	ESC_RX0_DATA2		
GPIO83	EPWM12_B	EMIF1_D1								SD3_D2	ESC_RX0_DATA3		
GPIO84	EPWM12_B	EMIF1_D1	EMIF1_CS4n	SCIA_TX	MDXB --> EQEP6_A		SD3_D2		UARTA_TX	SD3_C2	ESC_TX0_ENA	MDXA --> ESC_RX0_DATA3	
GPIO85	EPWM13_A	EMIF1_D0		SCIA_RX	MDRB --> EQEP6_B	SD3_D1			UARTA_RX	SD3_D3	ESC_TX0_CLK	MDRA --> EMIF1_DQM2	
GPIO86	EPWM13_B	EMIF1_A13	EMIF1_CAS	SCIB_TX	MCLKXB --> EQEP6_STROBE					SD3_C3	ESC_PHY0_LINKSTATUS	MCLKXA	
GPIO87	EPWM14_A	EMIF1_A14	EMIF1_RAS	SCIB_RX	MFSXB --> EQEP6_INDEX		EMIF1_DQM3			SD3_D4	ESC_TX0_DATA0	MFSXA	
GPIO88	EPWM14_B	EMIF1_A15	EMIF1_DQM0				EMIF1_DQM1			SD3_C4	ESC_TX0_DATA1		
GPIO89	EPWM15_A	EMIF1_A16	EMIF1_DQM1		SCIC_TX	SD1_D3	EMIF1_CAS			SD4_D1	ESC_TX0_DATA2	SPID_PTE	
GPIO90	EPWM15_B	EMIF1_A17	EMIF1_DQM2		SCIC_RX	SD1_C3	EMIF1_RAS			SD4_C1	ESC_TX0_DATA3	SPID_CLK	
GPIO91	EPWM16_A	EMIF1_A18	EMIF1_DQM3		I2CA_SDA	SD4_D2	EMIF1_DQM2	PMBUSA_SCL			CLB_OUTPUTXBAR1	SPID_PICO	
GPIO92	EPWM16_B	EMIF1_A19	EMIF1_BA1		I2CA_SCL	SD4_C2	EMIF1_DQM0	PMBUSA_SDA	FSIRXD_CLK		CLB_OUTPUTXBAR2	SPID_POCI	
GPIO93	EPWM17_A		EMIF1_BA0		SCID_TX	SD4_D3		PMBUSA_ALERT	ESC_TX1_CLK		CLB_OUTPUTXBAR3	SPID_CLK	
GPIO94	EPWM17_B				SCID_RX	SD4_C3	EMIF1_BA1	PMBUSA_CTL	ESC_TX1_ENA		CLB_OUTPUTXBAR4	SPID_PTE	
GPIO95	EPWM18_A	EQEP4_A			SD1_D1			ESC_GPO10			CLB_OUTPUTXBAR5		
GPIO96	EPWM18_B	EQEP4_B	EMIF2_DQM1	EQEP1_A	SD1_C1			ESC_GPO11			CLB_OUTPUTXBAR6		
GPIO97		EQEP4_STROBE	EMIF2_DQM0	EQEP1_B	SD1_D2			ESC_GPI17			CLB_OUTPUTXBAR7		

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO98		EQEP4_INDEX	EMIF2_A0	EQEP1_STROBE	SD1_C2			ESC_GPI18			CLB_OUTPUTXBAR8		
GPIO99		EMIF1_DQM3	EMIF2_A1 --> EPWM8_A	EQEP1_INDEX		SD4_D4		ESC_GPI21			EMIF1_D17		
GPIO100	SPIA_PICO	EMIF1_BA1	EMIF2_A2 --> EPWM9_A	EQEP2_A	SPIC_SIMO --> SPIC_PICO	SD4_C4	SD1_D1	ESC_GPI0	FSIRXD_D1	FSITXA_D0	EMIF1_D24		
GPIO101	EPWM18_A		EMIF2_A3	EQEP2_B	SPIC_SOMI --> SPIC_POCI			ESC_GPI1	EMIF1_A5	FSITXA_D1			
GPIO102	EPWM18_B		EMIF2_A4	EQEP2_STROBE	SPIC_CLK			ESC_GPI2	EMIF1_A6	FSITXA_CLK			
GPIO103		EMIF1_BA0	EMIF2_A5 --> EPWM8_B	EQEP2_INDEX	SPIC_STE --> SPIC_PTE	SD4_C4		ESC_GPI3		FSIRXA_D0			
GPIO104	I2CA_SDA	EPWM18_A	EMIF2_A6	EQEP3_A	SCID_TX --> SD3_D1			ESC_GPI4		FSIRXA_D1	ESC_SYNC0		
GPIO105	I2CA_SCL	EPWM18_B	EMIF2_A7	EQEP3_B	SCID_RX --> SD3_C1			ESC_GPI5		FSIRXA_CLK	ESC_SYNC1		
GPIO106	EPWM16_A	EMIF1_A10	EMIF2_A8	EQEP3_STROBE	SCIC_TX --> SD3_D2			ESC_GPI6		FSITXB_D0			
GPIO107	EPWM16_B		EMIF2_A9	EQEP3_INDEX	SCIC_RX --> SD3_C2			ESC_GPI7		FSITXB_D1			
GPIO108	EPWM17_A	EMIF1_A12	EMIF2_A10	EQEP5_A	SD3_D3			ESC_GPI8		FSITXB_CLK			
GPIO109	EPWM17_B	EMIF1_A11	EMIF2_A11	EQEP5_B	SD3_C3			ESC_GPI9					
GPIO110	EMIF1_D31		EMIF2_WAIT	EQEP5_STROBE	SD3_D4			ESC_GPI10		FSIRXB_D0			
GPIO111	EMIF1_D30		EMIF2_BA0	EQEP5_INDEX	SD3_C4			ESC_GPI11		FSIRXB_D1			
GPIO112	EMIF1_D29		EMIF2_BA1			SD1_D3		ESC_GPI12		FSIRXB_CLK			
GPIO113	EMIF1_D28		EMIF2_CAS			SD1_C3		ESC_GPI13					
GPIO114	EMIF1_D27		EMIF2_RAS			SD1_D4		ESC_GPI14					
GPIO115	EMIF1_D26		EMIF2_CS0n	OUTPUTXBAR5		SD1_C4		ESC_GPI15		FSIRXC_D0			
GPIO116			EMIF2_CS2n	OUTPUTXBAR6				ESC_GPI16		FSIRXC_D1			
GPIO117			EMIF2_SDCKE					ESC_GPI17		FSIRXC_CLK			
GPIO118			EMIF2_CLK					ESC_GPI18		FSIRXD_D0			
GPIO119	EMIF1_D25		EMIF2_RNW	MCANB_TX				ESC_GPI19		FSIRXD_D1			
GPIO120	EMIF1_D24		EMIF2_WEn	MCANB_RX				ESC_GPI20		FSIRXD_CLK		USB0PFLT	
GPIO121			EMIF2_OEn					ESC_GPI21				USB0EPEN	

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO122	EMIF1_D23				SPIC_SIMO --> SPIC_PICO	SD1_D1		ESC_GPI22					
GPIO123	EMIF1_D22				SPIC_SOMI --> SPIC_POCI	SD1_C1		ESC_GPI23					
GPIO124	EMIF1_D21				SPIC_CLK	SD1_D2		ESC_GPI24					
GPIO125	EMIF1_D20				SPIC_STE --> SPIC_PTE	SD1_C2		ESC_GPI25			ESC_LATCH0		
GPIO126	EMIF1_D19				SPID_PICO	SD1_D3		ESC_GPI26			ESC_LATCH1		
GPIO127	EMIF1_D18				SPID_POCI	SD1_C3		ESC_GPI27			ESC_SYNC0		
GPIO128	EMIF1_D17				SPID_CLK	SD1_D4		ESC_GPI28			ESC_SYNC1		
GPIO129	EMIF1_D16				SPID_PTE	SD1_C4		ESC_GPI29			ESC_TX1_ENA		
GPIO130	EPWM13_A					SD2_D1		ESC_GPI30			ESC_TX1_CLK		
GPIO131	EPWM13_B					SD2_C1		ESC_GPI31			ESC_TX1_DATA0		
GPIO132	EPWM14_A					SD2_D2		ESC_GPO0			ESC_TX1_DATA1		
GPIO133	EMIF1_A11	EPWM9_A				SD2_C2			ESC_LED_STATE_RUN				
GPIO134	EPWM14_B					SD2_D3		ESC_GPO1		SD2_C1	ESC_TX1_DATA2		
GPIO135					SCIA_TX	SD2_C3		ESC_GPO2	SD2_C1		ESC_TX1_DATA3		
GPIO136					SCIA_RX	SD2_D4		ESC_GPO3			ESC_RX1_DV		
GPIO137					SCIB_TX	SD2_C4		ESC_GPO4			ESC_RX1_CLK		
GPIO138					SCIB_RX			ESC_GPO5			ESC_RX1_ERR		
GPIO139					SCIC_RX --> SCIA_TX			ESC_GPO6			ESC_RX1_DATA0		
GPIO140					SCIC_TX --> SCIA_RX			ESC_GPO7			ESC_RX1_DATA1		
GPIO141	EPWM15_A				SCID_RX --> SCIB_TX			ESC_GPO8			ESC_RX1_DATA2		
GPIO142	EPWM15_B				SCID_TX --> SCIB_RX			ESC_GPO9			ESC_RX1_DATA3		
GPIO143								ESC_GPO10			ESC_LED_LINK0_ACTIVE		
GPIO144								ESC_GPO11			ESC_LED_LINK1_ACTIVE		
GPIO145	EPWM1_A				MCANB_TX			ESC_GPO12			ESC_LED_ERR		
GPIO146	EPWM1_B				MCANB_RX			ESC_GPO13			ESC_LED_RUN		
GPIO147	EPWM2_A				EQEP5_A			ESC_GPO14			ESC_LED_STATE_RUN		
GPIO148	EPWM2_B				EQEP5_B			ESC_GPO15			ESC_PHY0_LINK STATUS		
GPIO149	EPWM3_A				EQEP5_STROBE			ESC_GPO16			ESC_PHY1_LINK STATUS		
GPIO150	EPWM3_B				EQEP5_INDEX			ESC_GPO17			ESC_I2C_SDA		

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO151	EPWM4_A				PMBUSA_SCL			ESC_GPO18		FSITXA_D0	ESC_I2C_SCL		
GPIO152	EPWM4_B				PMBUSA_SDA			ESC_GPO19		FSITXA_D1	ESC_MDIO_CLK		
GPIO153	EPWM5_A				PMBUSA_ALERT			ESC_GPO20		FSITXA_CLK	ESC_MDIO_DATA		
GPIO154	EPWM5_B				PMBUSA_CTL			ESC_GPO21		FSIRXA_D0	ESC_PHY_CLK		
GPIO155	EPWM6_A							ESC_GPO22		FSIRXA_D1	ESC_PHY_RESETn		
GPIO156	EPWM6_B							ESC_GPO23		FSIRXA_CLK	ESC_TX0_ENA		
GPIO157	EPWM7_A							ESC_GPO24		FSITXB_D0	ESC_TX0_CLK		
GPIO158	EPWM7_B							ESC_GPO25		FSITXB_D1	ESC_TX0_DATA0		
GPIO159	EPWM8_A							ESC_GPO26		FSITXB_CLK	ESC_TX0_DATA1		
GPIO160	EPWM8_B							ESC_GPO27		FSIRXB_D0	ESC_TX0_DATA2		
GPIO161	EPWM9_A							ESC_GPO28		FSIRXB_D1	ESC_TX0_DATA3		
GPIO162	EPWM9_B							ESC_GPO29		FSIRXB_CLK	ESC_RX0_DV		
GPIO163	EPWM10_A							ESC_GPO30		FSIRXC_D0	ESC_RX0_CLK		
GPIO164	EPWM10_B							ESC_GPO31		FSIRXC_D1	ESC_RX0_ERR		
GPIO165	EPWM11_A									FSIRXC_CLK	ESC_RX0_DATA0		
GPIO166	EPWM11_B									FSIRXD_D0	ESC_RX0_DATA1		
GPIO167	EPWM12_A									FSIRXD_D1	ESC_RX0_DATA2		
GPIO168	EPWM12_B									FSIRXD_CLK	ESC_RX0_DATA3		
GPIO169													
GPIO170													
GPIO171													
GPIO172													
GPIO173													
GPIO174													
GPIO175													
GPIO176													
GPIO177													
GPIO178													
GPIO179													
GPIO180													

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO181													
GPIO182													
GPIO183													
GPIO184													
GPIO185													
GPIO186													
GPIO187													
GPIO188													
GPIO189													
GPIO190													
GPIO191													
GPIO192													
GPIO193													
GPIO194													
GPIO195													
GPIO196													
GPIO197													
GPIO198	EQEP1_A	EPWM9_B	SPIA_PICO								ESC_PDI_UC_IRQ		
GPIO199	EQEP1_STROBE	EPWM17_A	SCIB_TX	EPWM12_A	SPIB_CLK	SD1_D4	MCANA_TX	EMIF1_RAS			SPIC_CLK		
GPIO200	EQEP1_INDEX	EPWM17_B	SCIB_RX	EPWM12_B	SPIB_PTE	SD1_C4	MCANA_RX	EMIF1_CAS	ESC_TX1_DATA1		SPIC_PTE		
GPIO201	OUTPUTXBAR1	EQEP2_A	EPWM18_A	LINB_TX	SPIB_PICO	SD2_D1	PMBUSA_SCL	EMIF1_DQM0	ESC_TX1_DATA2	EPWM13_A			
GPIO202	OUTPUTXBAR2	EQEP2_B	EPWM18_B	LINB_RX	SPIB_POCI	SD2_C1	PMBUSA_SDA	EMIF1_DQM1	ESC_TX1_DATA3	EPWM13_B	FSITXA_D1		
GPIO203	OUTPUTXBAR3	EQEP2_INDEX	SPIA_POCI	OUTPUTXBAR3	SPIB_CLK	SD3_D1	PMBUSA_ALERT	EMIF1_DQM2	ESC_MDIO_CLK	EPWM14_A	FSITXA_D0	EPWM8_B	
GPIO204	OUTPUTXBAR4	EQEP2_STROBE	SPIA_CLK	OUTPUTXBAR4	SPIB_PTE	SD2_C2	PMBUSA_CTL	EMIF1_DQM3	ESC_MDIO_DATA	EPWM14_B	FSITXA_CLK	SD1_D3	
GPIO205	EQEP1_INDEX	EPWM10_A	SPIA_PTE						OUTPUTXBAR1			SD1_C3	
GPIO206	EMIF1_A11	EPWM10_B	EMIF1_WEn						OUTPUTXBAR2		ESC_PHY_CLK	ESC_LED_STATE_RUN	
GPIO207	EQEP2_A	EPWM11_A	EXTSYNCOUT	CANA_TX	SD4_D1	SCIA_RX	LINA_RX	I2CB_SCL	OUTPUTXBAR3		ESC_RX1_CLK	PMBUSA_ALERT	
GPIO208	EQEP2_B	EPWM11_B	EMIF1_D13	SPIB_PICO	SD4_C1	SCIA_TX			OUTPUTXBAR4		ESC_RX1_DV	PMBUSA_CTL	
GPIO209	EQEP2_STROBE	EPWM12_A	EMIF1_D14	SPIB_POCI	SD4_D2	EPWM12_B		LINB_RX	OUTPUTXBAR5		ESC_RX1_ERR	PMBUSA_SDA	
GPIO210	EQEP2_INDEX	EPWM12_B	EMIF1_D15		SD4_C2			LINB_TX	OUTPUTXBAR6		ESC_RX0_DATA2	PMBUSA_SCL	
GPIO211	EQEP6_A	EPWM14_A			SD4_D3				OUTPUTXBAR7		ESC_LED_LINK0_ACTIVE		
GPIO212	EQEP6_B	EPWM14_B			SD4_C3						ESC_LED_LINK1_ACTIVE		
GPIO213	EQEP6_STROBE	EPWM8_A			SD4_D4			LINB_TX			ESC_LED_ERR		

Table 3-13. GPIO Mux Overlay Table (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO214	CANA_RX	EMIF1_CLK	MCANA_RX	OUTPUTXBAR7	EQEP3_STROBE	SD2_D4	EMIF1_CS4n	ESC_LATCH1	ESC_I2C_SCL	EPWM16_A	ESC_SYNC1	SPID_PICO	
GPIO215	SCIA_RX	EMIF1_CS4n	CANA_RX	OUTPUTXBAR5	EQEP3_A	SD2_D3	EMIF1_CS2n	I2CB_SDA	SPIC_POCI	EPWM15_A	LINA_TX	EMIF1_D12	
GPIO216	SCIA_TX	EMIF1_SDCKE	SPID_CLK	OUTPUTXBAR6	EQEP3_B	SD2_C3	EMIF1_CS3n	ESC_LATCH0	ESC_I2C_SDA	EPWM15_B	ESC_SYNC0	EMIF1_D13	
GPIO217	CANA_TX	EMIF1_WEn	MCANA_TX	OUTPUTXBAR8	EQEP3_INDEX	SD2_C4	EMIF1_RNW	I2CA_SDA	SPID_PTE	EPWM16_B	LINB_TX	SPID_POCI	
GPIO218	I2CA_SDA	EMIF1_CS0n	SPIA_PICO	EQEP4_A	LINB_TX	CLB_OUTPUTXBAR1	EMIF1_OEn	I2CA_SCL				SPID_CLK	
GPIO219	EQEP6_INDEX	EPWM8_B			SD4_C4						ESC_LED_RUN		
GPIO220		EPWM6_A	SPID_POCI	OUTPUTXBAR2	SCIB_TX	MCANA_TX						PMBUSA_ALERT	X1
GPIO221		EPWM6_B	SPID_PTE	OUTPUTXBAR3	SCIB_RX	MCANA_RX						PMBUSA_CTL	X2
GPIO222	TDI	EPWM7_A	SPIA_PICO	OUTPUTXBAR4	SCIA_RX	UARTB_TX	I2CA_SDA	SPIC_CLK			ESC_PDI_UC_IRQ	PMBUSA_SDA	GPIO222
GPIO223	TDO	EPWM7_B	EMIF1_A11	OUTPUTXBAR5	SCIA_TX	UARTB_RX	I2CA_SCL	SPIC_PTE				PMBUSA_SCL	GPIO223
GPIO224	ERRORSTS	EMIF1_SDCKE	XCLKOUT	OUTPUTXBAR1						SD2_C1	ESC_PDI_UC_IRQ		

3.9 Analog Multiplexing Changes

Section 3.9.1 outlines the differences and similarities that exist in the analog mux between F2837x and F28P65x for the 176-Pin PTP devices. The main changes are the absence of ADCD and the increase in the number of CMPSS modules in F28P65x from the eight that exist in F2837x to eleven.

3.9.1 F2837x_176PTP vs F28P65x_176PTP Analog Connections Comparison

Table 3-14. Analog Mux Legend

Color	Description
	common for both devices
	applicable only for F2837x
	applicable only for F28P65x
	different between devices, F2837x listed on first row and F28P65x in second row

Table 3-15. Analog Mux Overlay Table

Pin	Name	ADCA	ADCB	ADCC	ADCD	DAC	High Positive	High Negative	Low Positive	Low Negative	AIO
22	C0			C0			CMP6_HP1	CMP6_HN1	CMP6_LP1	CMP6_LN1	
23	C1			C1			CMP6_HP2		CMP6_LP2		
24	C9			C9			CMP11_HP2		CMP11_LP2		
25	C8			C8			CMP10_HP2		CMP10_LP2		
26	C7			C7			CMP11_HP1		CMP11_LP1		
27	C6			C6			CMP10_HP1		CMP10_LP1		
28	C5			C5				CMP5_HN0	CMP2_LP3	CMP5_LN0	
29	C4/CMPIN5P --> C4			C4			CMP5_HP0	CMP10_HN1	CMP5_LP0	CMP10_LN1	
30	C3/CMPIN6N --> C3			C3				CMP6_HN0	CMP3_LP3	CMP6_LN0	
31	C2/CMPIN6P --> C2			C2			CMP6_HP0		CMP6_LP0		AIO237
32	VREFLOC										
33	VREFLOA										
35	VREFHIC										
37	VREFHIA										
38	A5/CMPIN2N --> A5	A5					CMP2_HP3	CMP2_HN0	CMP9_LP2	CMP2_LN0	AIO232
39	A4/CMPIN2P --> A4	A4					CMP2_HP0		CMP2_LP0		AIO231
40	A3/CMPIN1N --> A3	A3					CMP1_HP3	CMP1_HN0		CMP1_LN0	AIO230
41	A2/CMPIN1P --> A2	A2					CMP1_HP0	CMP2_HN1	CMP1_LP0	CMP2_LN1	AIO229
42	A1/DACB_OUT --> A1	A1				DACB_OUT	CMP1_HP2	CMP1_HN1	CMP1_LP2	CMP1_LN1	AIO228
43	A0/DACA_OUT	A0				DACA_OUT	CMP1_HP1	CMP9_HN0	CMP1_LP1	CMP9_LN0	AIO227

Table 3-15. Analog Mux Overlay Table (continued)

Pin	Name	ADCA	ADCB	ADCC	ADCD	DAC	High Positive	High Negative	Low Positive	Low Negative	AIO
44	A14/B14/C14/D14/CMPIN4P --> A14/B14/C14	A14	B14	C14	D14		CMP4_HP0		CMP4_LP0		AIO225
45	A15/B15/C15/D15/CMPIN4N --> A15/B15/C15	A15	B15	C15	D15		CMP4_HP3	CMP4_HN0		CMP4_LN0	AIO226
46	B0/VDAC		B0			VDAC	CMP3_HP1	CMP11_HN0	CMP3_LP1	CMP11_LN0	AIO233
47	B1/DACC_OUT		B1			DACC_OUT	CMP3_HP2		CMP3_LP2		AIO234
48	B2/CMPIN3P --> B2		B2				CMP3_HP0		CMP3_LP0		AIO235
49	B3/CMPIN3N --> B3		B3					CMP3_HN0	CMP1_LP3	CMP3_LN0	AIO236
50	VREFLOB										
51	VREFLOD --> B11		B11				CMP4_HP2		CMP4_LP2		AIO240
53	VREFHIB										
55	VREFHID --> B6		B6				CMP7_HP1	CMP7_HN1	CMP7_LP1	CMP7_LN1	
56	D0/CMPIN7P --> B7		B7		D0		CMP7_HP0 --> CMP7_HP2	CMP3_HN1	CMP7_LP0 --> CMP7_LP2	CMP3_LN1	
57	D1/CMPIN7N --> A6	A6			D1		CMP7_HP0	CMP7_HN0	CMP7_LP0	CMP7_LN0	
58	D2/CMPIN8P --> A7	A7			D2		CMP8_HP0 --> CMP9_HP2	CMP7_HN0	CMP8_LP0 --> CMP4_LP3	CMP7_LN0	
59	D3/CMPIN8N --> A8	A8			D3		CMP8_HP0	CMP8_HN0	CMP8_LP0	CMP8_LN0	
60	D4 --> A9	A9			D4			CMP8_HN0	CMP5_LP3	CMP8_LN0	
61	B10		B10				CMP4_HP1	CMP4_HN1	CMP4_LP1	CMP4_LN1	
62	A10	A10					CMP8_HP1	CMP8_HN1	CMP8_LP1	CMP8_LN1	
63	A11	A11					CMP8_HP2		CMP8_LP2		
64	B4		B4				CMP5_HP1	CMP5_HN1	CMP5_LP1	CMP5_LN1	
65	B5		B5				CMP5_HP2		CMP5_LP2		
66	B8		B8				CMP2_HP1	CMP10_HN0	CMP2_LP1	CMP10_LN0	
67	B9		B9				CMP2_HP2	CMP9_HN1	CMP2_LP2	CMP9_LN1	
INT1	TEMP SENSOR	A13	B18								

4 Application Code Migration From F2837x to F28P65x

The following section describes code changes when migrating from F2837x to F28P65x. C2000Ware drivers and examples for the F28P65x will be updated to support the new features as described in Section 3.1.

4.1 C2000Ware Header Files

Header files for both F2837x and F28P65x devices are available in C2000Ware under the device_support sub directory for bit field and driverlib sub directory for Driverlib.

4.2 Linker Command Files

Linker command files for both F2837x and F28P65x devices are available in C2000Ware under the device_support sub directory.

4.3 C2000Ware Examples

C2000Ware has examples specific for both F2837x and F28P65x devices.

5 EABI Support

In the past, F2837x applications have always supported the Common Object File Format (COFF) binary executable output. COFF has several limitations. One of which is that the symbolic debugging information is not capable of supporting C/C++. There is also a limit on the maximum number of sections and length of section names and source files, among other things. COFF is also not an industry standard. For these reasons, C2000 is now migrating to Embedded Application Binary Interface (EABI) format. EABI and COFF are incompatible and conversion between the two formats is not possible. This section provides summary of COFF and EABI differences and useful links that provide more guidelines in migrating applications from COFF to EABI.

- EABI key differences with COFF:
  - Direct initialization
    - Uninitialized data is zero by default in EABI.
    - Initialization of RW data is accomplished via linker-generated compressed copy tables in EABI.
  - C++ language support
    - C++ inline function semantics: In COFF, inline functions are treated as static inline and this causes issues for functions that cannot be inlined or have static data. In EABI, inline functions without the ‘static’ qualifier have external linkage.
    - Better template instantiation: COFF uses a method called late template instantiation and EABI uses early template instantiation. Late template instantiation can run into issues with library code and can result in long link times. Early instantiation uses ELF COMDAT to guarantee templates are always instantiated properly and at most one version of each instantiation is present in the final executable.
    - Table-Driven Exception Handling (TDEH): Almost zero impact on code performance as opposed to COFF which uses setjmp/longjmp to implement C++ exceptions Features enabled by EABI.
  - Features enabled by EABI
    - Location attribute: Specify the run-time address of a symbol in C-source code.
    - Noinit/persistent attribute: Specify if a symbol should not be initialized during C auto initialization.
    - Weak attribute: Weak symbol definitions are pre-empted by strong definitions. Weak symbol references are not required to be resolved at link time. Unresolved weak symbols resolve to 0.
    - External aliases: In COFF, the compiler will make A an alias to B if all calls to A can be replaced with B. A and B must be defined in the same file. In EABI, the compiler will make A an alias to B even if B is external.
  - Calling convention
    - Scalar calling convention is identical between COFF and EABI
    - Struct calling convention (EABI)
      - Single field structs are passed/returned by value corresponding to the underlying scalar types.
      - For FPU32, homogenous float structs with size less than 128 bits will be passed by value.
      - Passed in R0H-R3H, then by value on the stack.
      - Structs that are passed by value are also candidates for register allocation.
      - For FPU64, the same applies for 64-bit doubles(R0-R3).

  - Double memory size
    - In EABI, double is 64-bit size while in COFF, double is still represented as 32-bit size.
    - C/C++ requires that double be able to represent integer types with at least 10 decimal digits, which effectively requires 64-bit double precision.
- Sections overview:

  Table 5-1 summarizes the section names for COFF and EABI. These are compiler-generated sections.

Table 5-1. Section Names

Description	COFF	EABI
Read-Only Sections		
Const data	.econst	.const
Const data above 22-bits	.farconst	.farconst
Code	.text	.text
Pre-main constructors	.pinit	.init_array
Exception handling	N/A	.c28xabi.exidx/.c28xabi.extab
Read-Write Sections		
Uninitialized data	.ebss	.bss
Initialized data	N/A	.data
Uninitialized data above 22-bits	.farbss	.farbss
Initialized data above 22-bits	N/A	.fardata
Heap	.esysmem	.sysmem
Stack	.stack	.stack
CIO Buffer	.cio	.bss:cio

- Resources:
  For more information regarding EABI and the migration process, see the resources on the links below:
  - Wiki: http://processors.wiki.ti.com/index.php/EABI
  - Wiki: http://processors.wiki.ti.com/index.php/C2000_EABI_Migration
  - C28 EABI Specifications: *C28x embedded application binary interface* (SPRAC71)

5.1 NoINIT Struct Fix (Linker Command)

With EABI, the SECTIONS area of a linker command file has to be modified as shown in the example below in order for the registers or memory areas to not be initialized to a zero value. This is important as failure to make this modification can result to unintended behavior when register bits are forced to zero during start up. By default, EABI initializes registers or memory areas defined in the SECTIONS part of the linker to zero.

Linker modification example:

```
SECTIONS
{
:
Regs1File :> REG1_ADDR, type=NOINIT
Regs2File :> REG2_ADDR, type=NOINIT
:
}
```

5.2 Pre-Compiled Libraries

All F28P65x libraries supplied by TI will be released as EABI. Future F28P65x libraries created by customers should be generated and compiled as EABI as well.

References

- Texas Insruments: *TMS320F28P65x Microcontrollers Technical Reference Manual*
- Texas Insruments: *TMS320F2837x Microcontrollers Technical Reference Manual*
- Texas Insruments: *TMS320F28P65x Microcontrollers Data Sheet*

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