Application Report
SWCA081–June 2009

TPS65920/30 Schematic Checklist

ABSTRACT

This application note for TPS65920/30, a power companion device for OMAP processors, lists the connection details for each pin. The ball details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each ball on a system schematic.

Table 1. TPS65920/30 Schematic Checklist

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
ADC	ADCIN0	Battery type	I/O	H2	H2	Internal current source. Limited input voltage 1.5 V. No prescaler. Grounded if not used.	GND
	ADCIN2	General-purpose ADC input	I	F2	F2	Prescaler integrated. Limited input voltage 2.5 V. Grounded if not used.	GND
Charger	PCHGAC	AC precharge sense signal. Also used for EEPROM.	I	M5	M5	Ac path, power FET power dissipation limitation, check TRM for calculation. Common value are in the 700K range.	GND
	VPRECH	Precharge regulator output	O	N1	N1	Capacitor of 1uF to ground. Cap to ground if BCI not used.	1uF cap to GND
	VBAT	Battery voltage sensing	Power	N5	N5	Add 10 F Filtering capacitor. VBAT level sense.	VBAT
GPIOs/JTAG	GPIO0/CD1	GPIO0/card detection 1	I/O	F7	F7	Can be left floating as internal PD	Floating
		JTAG test data output	I/O			Connected to TDI next chip if used	
	GPIO1/CD2	GPIO1/card detection 2	I/O	E7	E7	Can be left floating as internal PD	Floating
		JTAG test mode state	I			Connected to general TMS if used.	
	GPIO2	GPIO2	I/O	P2	P2	Can be left floating as internal PD	Floating
		TEST1 pin used in test mode only	I/O			Can be left floating as internal PD. TP.	
	GPIO15	GPIO15	I/O	P13	P13	Can be left floating as internal PD	Floating
		TEST2 pin used in test mode only	I/O			Can be left floating as internal PD. TP.	
	GPIO6	GPIO6	I/O	L5	L5	Can be left floating as internal PD	Floating
		Pulse width driver 0	O			Can be left floating as internal PD	
		TEST3 pin used in test mode only (controlled by JTAG)	I/O			Can be left floating as internal PD. TP	
	GPIO7	GPIO7	I/O	J7	J7	Can be left floating as internal PD	Floating
		Vibrator on-off synchronization	I			Can be left floating as internal PD or PU.	
		Pulse width driver	O			Can be left floating as output.	
		TEST4 pin used in test mode only (controlled by JTAG)	I/O			Can be left floating as internal PD or PU. TP.	

Table 1. TPS65920/30 Schematic Checklist (continued)

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
CONTROL	SYSEN	System enable output	Open drain/I	D8	D8	Control slave power IC in master mode or force T2 in Wai-on if low in slave mode. TP required.	Floating
	CLKEN	Clock enable	O	A4	A4	Clock enable, TP	Floating
	CLKREQ	Clock request	I	B13	B13	NSLEEP3. Associated with processor3.TP. Grounded if not used.	GND
	INT1	Output interrupt line 1	O	C10	C10	output interrupt for processor 1. TP.	Floating
	NRESPWRON	Output control the NRESPWRON of the application processor	O	C8	C8	Control of host processor reset. TP.	Floating
	NRESWARM	Input; detect user action on the reset button	I	B9	B9	User reset. TP. PU required if connected to button. GND if not used.	GND
	PWRON	Input; detect a control command to start or stop the system	I	D10	D10	Switch on control. TP (secondary general reset after 8 slow state and battery removal). Need external PU of 5KW.	VBAT
	NSLEEP1	Sleep request from device 1	I	G5	G5	Sleep request from processor 1. TP.	GND
	CLK256FS	Clock rate = 256*FS	O	E10	E10	Audio clock 256 FS. TP. Valid for TPS65930 only	Floating
	VMODE1	Digital voltage scaling linked with VDD1	I	E4	E4	Digital voltage scaling. Ground if not used.	GND
	BOOT0	Boot pin 0	I	E8	E8	Boot selection. TP. 4 possibilities.	
	BOOT1	Boot pin 1	I	D7	D7	Boot selection. TP. 4 possibilities.	
	REGEN	Enable signal for external LDO	Open drain	B8	B8	External LDO control. TP.	Floating
	MSECURE	Security and digital rights management	I	H4	H4	Secure mode: 1 to be active (RW of secure registers possible). Unsecure mode: 0. Only read is possible.	
VREF	VREF	Reference voltage	Power	L13	L13	Bandgap voltage. 1 uF cap between VREF and AGND.	
	AGND	Analog ground for reference voltage	Power GND	K13	K13	Clean analog ground connected to 1 plane	
I2C SmartReflex	I2C.SR.SDA	SmartReflex I2C data	I/O	B3	B3	Floating if not used	Floating
	VMODE2	Digital voltage scaling linked with VDD2	I	C5	C5	Digital voltage scaling. GND If not used.	GND
	I2C.SR.SCL	SmartReflex I2C clock	I			GND if not used.	
I2C	I2C.CNTL.SDA	General-purpose I2C data	I/O	C3	C3		
	I2C.CNTL.SCL	General-purpose I2C clock	I	B4	B4		

Table 1. TPS65920/30 Schematic Checklist (continued)

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
TDM	I2S.CLK	Clock signal (audio port)	I/O		H3	All audio I2S signals must be routed symetrically. TP.	Floating
	I2S.SYNC	Synchronization signal (audio port)	I/O		K2	All audio I2S signals must be routed symetrically. TP.	Floating
	I2S.DIN	Data receive (audio port)	I		K4	All audio I2S signals must be routed symetrically. TP. Grounded if not used.	GND
	I2S.DOUT	Data transmit (audio port)	O		K3	All audio I2S signals must be routed symetrically. TP.	Floating
ANA.MIC	MIC.MAIN.P	Main microphone left input (P)	I		D1	"Route symmetrically with MIC.MAIN.M, shielded, with TDMA filtering cap and coupling capacitor. Only for TPS65930"	Floating
	MIC.MAIN.M	Main microphone left input (M)	I		E1	"Route symmetrically with MIC.MAIN.P, shielded, with TDMA filtering cap and coupling capacitor. Only for TPS65930"	Floating
Hands-Free	VBAT.RIGHT	Battery voltage input	Power	A10	A10	Filtering capacitor of 1 uF. Connected to VBAT if not used.	VBAT
Headset	PreDriv.Left	Predriver output left P for external class-D amplifier	O		A7	Audio output to connect external device through coupling capacitor of at least 1uF.	Floating
	VMID		Power			Headset output common mode voltage for specific applicative case without coupling cap. Controlled by Predriv.LEFT register.	
	PreDriv.Right	Predriver output right P for external class-D amplifier	O		A8	Audio output to connect external device through coupling capacitor of at least 1uF	GND
	ADCIN7	General-purpose ADC input 7	I			General-purpose. Prescaler integrated. Limited input voltage 2.5 V. Grounded if not used.	
AUX Input	AUXR	Auxiliary audio input right	I		G1	Add TDMA filtering capacitor and 100 nF coupling cap.	Floating
VMIC BIAS	MICBIAS1.OUT	Analog microphone bias 1	Power		E2	Serial resistor required for filtering cap higher than 200 pF	Floating
	MICBIAS.GND	Dedicated ground for microphones	Power GND		D2	Connected to AGND	GND
	AVSS1	Analog ground	Power GND	G2	G2	Analog ground connected to 1 plane	
	AVSS2			L7	L7	Analog ground connected to 1 plane	
	AVSS3			N14	N14	Analog ground connected to 1 plane	
	AVSS4			C7	C7	Analog ground connected to 1 plane	

Table 1. TPS65920/30 Schematic Checklist (continued)

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
CLOCK	32KCLKOUT	Buffered output of the 32-kHz digital clock	O	M10	M10	No more than 30-pF load	Floating
	32KXIN	Input of the 32-kHz oscillator	I	L14	L14	CXIN = CXOUT = Cosc*2 – (Cint + Cpin), Cint - Internal foot capacitance (refer oscillator data sheet) Cpin - Parasitic pin capacitance (refer oscillator data sheet) Generally, Cpin and Cint will be negligible	
	32KXOUT	Output of the 32-kHz oscillator	O	K14	K14	CXIN = CXOUT = Cosc*2 – (Cint + Cpin), Cint - Internal foot capacitance (refer oscillator data sheet) Cpin - Parasitic pin capacitance (refer oscillator data sheet) Generally, Cpin and Cint will be negligible	
	HFCLKIN	Input of the digital (or sine) HS clock	I	A11	A11	For sine wave, no more than 1.45 Vpp amplitude	
	HFCLKOUT	HS clock output	O	M11	M11	No more than 40-pF load programmable	Floating
USB PHY	VBUS	VBUS power rail	Power	P8	P8	Directly connected to USB connector without resistive add. 4.7 uF cap connected between VBUS and VSSP.	GND
	DP/UART3.RXD	USB data P/USB carkit receive data/universal asynchronous receiver/transmitter (UART)3 receive data	I/O	N10	N10	Directly connected to USB symetrically with TXD	Floating
	DN/UART3.TXD	USB data N/USB carkit transmit data/UART3 transmit data	I/O	P10	P10	Directly connected to USB symetrically with RXD	Floating
	ID	USB ID	I/O	G6	G6	Connected to VUSB3P1 if not used	Connected to VUSB3P1
ULPI	UCLK	HS USB clock	I/O	K11	K11	Connected to OMAP. Floating if not used.	Floating
	STP	HS USB stop	I	H12	H12	Connected to OMAP. Floating if not used.	Floating
		GPIO9	I/O				
	DIR	HS USB direction	O	H11	H11	Connected to OMAP. Floating if not used.	Floating
		GPIO10	I/O				
	NXT	HS USB next	O	J8	J8	Connected to OMAP. Floating if not used.	Floating
		GPIO11	I/O				
	DATA0	HS USB Data0	I/O	L10	L10	Connected to OMAP. Floating if not used.	Floating
		UART4.TXD	I				
	DATA1	HS USB Data1	I/O	K10	K10	Connected to OMAP. Floating if not used.	Floating
		UART4.RXD	O				

Table 1. TPS65920/30 Schematic Checklist (continued)

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
	DATA2	HS USB Data2	I/O	G11	G11	Connected to OMAP. Floating if not used.	Floating
		UART4.RTSI	I				
	DATA3	HS USB Data3	I/O	G10	G10	Connected to OMAP. Floating if not used.	Floating
		UART4.CTSO	O				
		GPIO12	I/O				
	DATA4	HS USB Data4	I/O	E12	E12	Connected to OMAP. Floating if not used.	Floating
		GPIO14	I/O				
	DATA5	HS USB Data5	I/O	G9	G9	Connected to OMAP. Floating if not used.	Floating
		GPIO3	I/O				
	DATA6	HS USB Data6	I/O	G12	G12	Connected to OMAP. Floating if not used.	Floating
		GPIO4	I/O				
	DATA7	HS USB Data7	I/O	E11	E11	Connected to OMAP. Floating if not used.	Floating
		GPIO5	I/O				
TEST	TEST.RESET	Reset T2 device (except power state-machine)	I	P14	P14	PD, cannot be used for application !	GND
	TESTV1	Analog test	I/O	P1	P1	TP or floating if not used	Floating
	TESTV2	Analog test	I/O	A14	A14	TP or floating if not used	Floating
	TEST	Selection between JTAG mode and application mode for JTAG/GPIOs (with PU or PD)	I	A1	A1	Connected to VIO for JTAG use or floating as internal PD if JTAG not used	Floating
	JTAG.TDI/ BERDATA	JTAG.TDI/BERDATA	I	A13	A13	Grounded if not used	GND
	JTAG.TCK/ BERCLK	JTAG.TCK/BERCLK	I	B14	B14	Grounded if not used	GND
USB CP	CP.IN	Charge pump input voltage	Power	P7	P7	Cap of 10 uF. Cap must be as close as possible to device.	VBAT
	CP.CAPP	Charge pump flying capacitor P	O	N7	N7	Connected to CP.CAPM by a cap of 2.2 uF	Floating
	CP.CAPM	Charge pump flying capacitor M	O	N6	N6	Connected to CP.CAPP by a cap of 2.2 uF	Floating
	CP.GND	Charge pump ground	Power GND	P5	P5	Connected to ground	GND
VBAT.USB	VBAT.USB	USB LDOs (VINTUSB1P5, VINTUSB1P8, VUSB.3P1) VBAT	Power	N9	N9	Cap of 1 uF. Cap must be as close as possible to device.	VBAT
USB.LDO	VUSB.3P1	USB LDO output	Power	M8	M8	Cap of 1 uF. Do not use externally.	

Table 1. TPS65920/30 Schematic Checklist (continued)

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
VAUX1	VAUX12S.IN	VAUX1/VAUX2/VSIM LDO input voltage	Power	L1	L1	Cap of 1 uF. Cap must be as close as possible to device.	VBAT
VAUX2	VAUX2.OUT	VAUX2 LDO output voltage	Power	N2	N2	Cap of 1 uF	Floating
VPLLA3R	VPLLA3R.IN	Input for VPLL1, VPLL2, VAUX3, and VRTC LDOs	Power	H14	H14	Cap of 1 uF. Important to get separate filtering.Cap must be as close as possible to device.	VBAT
VRTC	VRTC.OUT	VRTC internal LDO output (internal use only)	Power	K12	K12	Cap of 1 uF. Do not use externally.	
VPLL1	VPLL1.OUT	LDO output voltage	Power	G14	G14	Cap of 1 uF	Floating
VMMC1	VMMC1.IN	VMMC1 LDO input voltage	Power	A2	A2	Cap of 1 uF. Cap must be as close as possible to device.	VBAT
	VMMC1.OUT	VMMC1 LDO output voltage	Power	B1	B1	Cap of 1 uF	Floating
VINTUSB1P5	VINTUSB1P5. OUT	VINTUSB1P5 internal LDO output (internal use only)	Power	M7	M7	Cap of 1 uF. Do not use externally.	Floating
VINTUSB1P8	VINTUSB1P8. OUT	VINTUSB1P8 internal LDO output (internal use only)	Power	N8	N8	Cap of 1 uF. Do not use externally.	Floating
Video DAC	VDAC.IN	Input for VDAC, VINTANA1, and VINTANA2 LDOs	Power	K1	K1	Cap of 1 uF. Cap must be as close as possible to device.	VBAT
	VDAC.OUT	Output voltage of the regulator	Power	L2	L2	Cap of 1 uF	Floating
VINT	VINT.IN	Input for VINTDIG LDO	Power	H13	H13	Cap of 1 uF. Cap must be as close as possible to device.	VBAT
VINTANA1	VINTANA1.OUT	VINTANA1 internal LDO output (internal use only)	Power	H1	H1	Cap of 1 uF. Do not use externally.	
VINTANA2	VINTANA2.OUT	VINTANA2 internal LDO output (internal use only)	Power	J2	J2	Cap of 1 uF. Do not use externally. Connect both VINANA2 pins to a common capacitor	
	VINTANA2.OUT	VINTANA2 internal LDO output (internal use only)	Power	A5	A5	Cap of 1 uF. Do not use externally. Connect both VINANA2 pins to a common capacitor	
VINTDIG	VINTDIG.OUT	VINTDIG internal LDO output (internal use only)	Power	J13	J13	Cap of 1 uF. Do not use externally.	

Table 1. TPS65920/30 Schematic Checklist (continued)

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
VDD1	VDD1.IN	VDD1 dc-dc input voltage	Power	D13	D13	Cap of 10 uF. Cap must be as close as possible to device.	VBAT
	VDD1.IN	VDD1 dc-dc input voltage	Power	D12	D12		
	VDD1.IN	VDD1 dc-dc input voltage	Power	D14	D14		
	VDD1.SW	VDD1 dc-dc switch	O	C11	C11	L= 1uH to the device pad and C = 10 uF on the other end of inductor.	Floating
	VDD1.SW	VDD1 dc-dc switch	O	C12	C12		
	VDD1.SW	VDD1 dc-dc switch	O	C13	C13		
	VDD1.FB	VDD1 dc-dc output voltage (feedback)	I	E14	E14	Connect to the LC circuit (capacitor end).	GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	A12	A12	Connected to ground	GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	B11	B11		
	VDD1.GND	VDD1 dc-dc ground	Power GND	B12	B12		
VDD2	VDD2.IN	VDD2 dc-dc input voltage	Power	M13	M13	Cap of 10 uF. Cap must be as close as possible to device.	VBAT
	VDD2.IN	VDD2 dc-dc input voltage	Power	M12	M12		
	VDD2.FB	VDD2 dc-dc output voltage (feedback)	I	N13	N13	Connect to the LC circuit (capacitor end).	GND
	VDD2.SW	VDD2 dc-dc switch	O	N11	N11	L= 1uH to the device pad and C = 10 uF on the other end of inductor.	Floating
	VDD2.SW	VDD2 dc-dc switch	O	P11	P11		
	VDD2.GND	VDD2 dc-dc ground	Power GND	N12	N12	Connected to ground	GND
	VDD2.GND	VDD2 dc-dc ground	Power GND	P12	P12		
VIO	VIO.IN	VIO dc-dc input voltage	Power	M2	M2	Cap of 10 uF. Cap must be as close as possible to device.	VBAT
	VIO.IN	VIO dc-dc input voltage	Power	M3	M3		
	VIO.FB	VIO dc-dc output voltage (feedback)	I	M4	M4	Connect to the LC circuit (capacitor end).	GND
	VIO.SW	VIO dc-dc switch	O	N4	N4	L= 1uH to the device pad and C = 10 uF on the other end of inductor	Floating
	VIO.SW	VIO dc-dc switch	O	P4	P4		
	VIO.GND	VIO dc-dc ground	Power GND	N3	N3	Connected to ground	GND
	VIO.GND	VIO dc-dc ground	Power GND	P3	P3		
Backup battery	BKBAT	Backup battery	Power	H9	H9	2.5- to 3.2-V backup battery. Grounded if not used.	GND
Digital VDD	IO.1P8	TPS65920/TPS65930 device I/O input	Power	B7	B7	To connect to VIO. Add filtering cap.	

Table 1. TPS65920/30 Schematic Checklist (continued)

Module	Default Config	Description	Type	TPS65920 Ball	TPS65930 Ball	Recommended Connectivity	Connectivity When Function is not Used
Digital ground	DGND	Digital ground	Power GND	H10	H10	Connected to ground	GND
LED driver	LEDGND	LED driver ground	Power GND	F13	F13	Connected to ground	GND
	GPIO13	GPIO13	I/O	B10	B10	Can be left floating if not used	Floating
	LEDSYNC	LED synchronization input	I			TP. Can be left floating if not used.	
	LEDA	LED leg A	Open drain	E13	E13	Do not connect to LEDB. 2.5 times LED drive.	Floating
	VIBRA.P	H-bridge vibrator P				Connected differentially with VIBRA.M. Floating if not used.	
	LEDB	LED leg B	Open drain	G13	G13	Do not connect to LEDA.	Floating
	VIBRA.M	H-bridge vibrator M				Connected differentially with VIBRA.P. Floating if not used.	
Keypad	KPD.C0	Keypad column 0	Open drain	G4	G4	Floating if not used	Floating
	KPD.C1	Keypad column 1	Open drain	G3	G3	Floating if not used	Floating
	KPD.C2	Keypad column 2	Open drain	E5	E5	Floating if not used	Floating
	KPD.C3	Keypad column 3	Open drain	B2	B2	Floating if not used	Floating
	KPD.C4	Keypad column 4	Open drain	E3	E3	Floating if not used	Floating
	KPD.C5	Keypad column 5	Open drain	D5	D5	Floating if not used	Floating
	KPD.R0	Keypad row 0	I	K7	K7	Floating if not used	Floating
	KPD.R1	Keypad row 1	I	H5	H5	Floating if not used	Floating
	KPD.R2	Keypad row 2	I	K5	K5	Floating if not used	Floating
	KPD.R3	Keypad row 3	I	H6	H6	Floating if not used	Floating
	KPD.R4	Keypad row 4	I	K8	K8	Floating if not used	Floating
	KPD.R5	Keypad row 5	I	L8	L8	Floating if not used	Floating

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