TPS659119-Q1 Schematic Checklist

ABSTRACT

This application note for TPS659119-Q1, a power companion device for application processors (see the device data sheet) lists the connection details for each pin. The ball details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each ball on a system schematic.

In addition to this list, customers are advised to use the information in the data sheet, (TI literature number SWCS062A).

NOTE: Customer must ensure that the power-up sequence for the application processor is met. This document does not cover the details of the power-up sequence for TPS659119-Q1 or the application processor. Refer to the device data sheet and the reference designs for the application processors for the correct power-up sequence requirements.

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Table 1. TPS659119-Q1 Schematic Checklist

Name	LQFP Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
VDDIO	19	Power	I	Digital I/Os supply	Connect to system I/O supply: an external I/O supply or I/O supply provided by TPS659119-Q1 (usually VIO).	N/A
SDA_SDI	15	Digital	I/O	I^2C bidirectional data signal/serial peripheral interface data input (multiplexed)	1.2-k pullup to I/O supply	N/A
SCL_SCK	16	Digital	I/O	I^2C bidirectional clock signal/serial peripheral interface clock input (multiplexed)	1.2-k pullup to I/O supply	N/A
SLEEP	62	Digital	I	ACTIVE-to-SLEEP state transition control signal	Connected to processor control pin (that is, GPIO or any other low-power mode control pin)	GND
PWRHOLD	2	Digital	I	Switch on, switch off control signal/GPI, mode defined in EEPROM	Switch-on, switch-off mode: Can be connected to an external signal for PMIC power-up/power-down control or If control is not required, then can be tied to VRTC	Floating (internal pulldown)
					GPI: Connect based on system requirement	Floating
PWRON	55	Digital	I	External switch-on control (on button)	Push-button. PWRON transition low will power up PMIC	Floating (internal pullup)
NRESPWRON	66	Digital	O	Power off reset	Connect to reset input of the processor or any other similar function to show device power up is complete	N/A
INT1	75	Digital	O	Interrupt flag	Connect to the processor interrupt pin or a GPIO (optional)	Floating
NRESPWRON2	44	Digital	O, OD	Second NRESPWRON output	Pullup to I/O supply	Floating
BOOT1	33	Digital	I	Power-up sequence selection	Connect to VRTC for the EEPROM boot up sequence	N/A
CLK32KOUT	64	Digital	O	32-kHz clock output	To processor 32K clock input	Floating
OSC16MIN	35	Analog	I	16-MHz crystal oscillator	To crystal (if used)	Can be floating if using internal RC (defined in EEPROM)
OSC16MOUT	36	Analog	I	16-MHz crystal oscillator	To crystal (if used)	Can be floating if using internal RC (defined in EEPROM)
OSCEXT32K	37	Digital	I	Input external 32-kHz clock	To 32-kHz clock (if used)	GND
VREF	31	Analog	O	Bandgap voltage	Connect to 0.1-µF capacitor to REFGND. Capacitor close to device	N/A
REFGND	30	Analog	I/O	Reference ground	Connect to AGND (clean ground), same as 32K crystal GND	N/A

(1) I = Input; O = Output; OD = Open Drain

(2) VBAT is the battery or any input source other than preregulation. The maximum level is 5.5 V.

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Table 1. TPS659119-Q1 Schematic Checklist (continued)

Name	LQFP Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
TESTV	42	Analog	O	Analog test output (DFT)	Floating	Floating
VBACKUP	45	Power	I	Backup battery input	Backup battery - supercap or rechargeable coincell	Connected to GND (preferred) or VCC7
VCC1	61	Power	I	VDD1 DC-DC power input	Connect to VBAT with a 10-µF capacitor	Connected to VCC7 or GND
GND1	56, 57	Power	I/O	VDD1 DC-DC power ground	GND	GND
SW1	58, 59	Power	O	VDD1 DC-DC switched output	Connected to a 2.2-µH inductor and a 10-µF capacitor to ground	Floating
VFB1	54	Analog	I	VDD1 feedback voltage	Connected to a 2.2-µH inductor (other node that is away from the device)	GND or floating
VCC2	67,68	Power	I	VDD2 DC-DC power input	Connec to VBAT with a 10-µF capacitor	Connected to VCC7 or GND
GND2	71, 72	Power	I/O	VDD2 DC-DC power ground	GND	GND
SW2	69, 70	Power	O	VDD2 DC-DC switched output	Connected to a 2.2-µH inductor and a 10-µF capacitor to ground	Floating
VFB2	74	Analog	I	VDD2 DC-DC feedback voltage	Connected to a 2.2-µH inductor (other node that is away from the device)	GND or floating
VCCIO	21, 22	Power	I	VIO DC-DC power Input	Connec to VBAT with a 10-µF capacitor	Connected to VCC7 or GND
GNDIO	25, 26	Power	I/O	VIO DC-DC power ground	GND	GND
SWIO	23, 24	Power	O	VIO DC-DC switched output	Connected to a 2.2-µH inductor and a 10-µF capacitor to ground	Floating
VFBIO	28	Analog	I	VIO feedback voltage	Connected to a 2.2-µH inductor (other node that is away from the device)	GND or floating
VCC3	6	Power	I	LDO6, LDO7, and LDO8 power input	Connec to VBAT with a 4.7-µF capacitor	GND if other LDOs are not used (LDO6, LDO7, and LDO8 share this as a common input)
LDO8	1	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO7	7	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO6	4	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VCC4	79	Power	I	LDO5 power input	Connec to VBAT with a 4.7-µF capacitor	GND if LDO5 is not used
LDO5	77, 78	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VCC5	40	Power	I	LDO3 and LDO4 power input	Connec to VBAT with a 4.7-µF capacitor	GND if not used by LDO3 or LDO4
LDO3	38	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO4	41	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VRTC	48	Power	O	LDO regulator output	2.2 µF to GND	N/A

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Table 1. TPS659119-Q1 Schematic Checklist (continued)

Name	LQFP Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
VCC6	11, 12	Power	I	LDO1 and LDO2 power input	3.6-V (maximum) input. Needs external input or preregulated output from TPS659119-Q1	GND if LDO output is not used (LDO1 and LDO2)
LDO1	13, 14	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO2	9, 10	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VCC7	47	Power	I	VRTC power input and analog references supply	VBAT (5.5-V maximum) or other preregulated supply. Must be first supply provided for TPS659119-Q1.	N/A
AGND	46	Power	I/O	Analog ground	AGND	N/A
AGND2	20	Power	I/O	Analog ground	AGND	N/A
DGND	53	Power	I/O	Digital ground	GND	N/A
EN2	17	Digital	I/O	Enable for supplies/voltage scaling dedicated I^2C data	Processor I^2C for SmartReflex™ control with external pullup to VIO or connected to GPIO for DC-DC/LDO control	Floating
EN1	18	Digital	I/O	Enable for supplies/voltage scaling dedicated I^2C clock	Processor I^2C for SmartReflex control with external pullup to VIO or connected to GPIO for DC-DC/LDO control	Floating
GPIO0	8	Digital	I/O	GPIO, push-pull/OD as output. Default: defined in EEPROM	Connect to 120-kΩ PU to VDDIO (if configured as push-pull then pullup not required)	Floating
GPIO1	34	Digital	I/O, OD	GPIO/LED1 output. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO2	76	Digital	I/O, OD	GPIO/DC-DC clock synchronization. Default: defined in EEPROM	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO3	43	Digital	I/O, OD	GPIO/LED2 output. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO4	27	Digital	I/O, OD	GPIO. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO5	32	Digital	I/O, OD	GPIO. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO6	65	Digital	I/O; OD	GPIO. Default: defined in EEPROM	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO7	73	Digital	I/O, OD	GPIO. Default: defined in EEPROM	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO8	63	Digital	I/O, OD	GPIO. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
PWRDN	3	Analog	I	Reset input; that is, for thermal reset	Test point or optionally a jumper connected to GND for a reset. Can be floating on production platform.	Floating or based on implementation. That is, if PWRDN is active low in EEPROM then tie to VRTC to avoid device reset.

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Table 1. TPS659119-Q1 Schematic Checklist (continued)

Name	LQFP Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
HDRST	29	Digital	I	Cold reset	Test point or optionally a 3-pin test point to connect to GND and VRTC.	Floating
VCCS	39	Analog	I/O	Input for two comparators	Main supply of TPS659119-Q1 or multiple-cell battery through resistive divider	N/A
AGNDEX	49	Analog	Power	EXTCTRL resistive divider ground	Connect to GND	GND
EN	51	Digital	O	EXTCTRL enable signal for external converter	Connect to enable pin for external converter. Use voltage divider if enable pin breakdown voltage is less than 5V	Floating
VSENSE	50	Analog	I	EXTCTRL resistive divider output	Connect to external converter VSENSE pin.	GND
VOUT	52	Analog	I	EXTCTRL resistive divider input	Connect to external converter output voltage.	GND

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