User's Guide

CC33xx Hardware Integration

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ABSTRACT

This document provides the necessary WLAN and *Bluetooth*® Low Energy hardware operation information to aid in system design. This is a review of the integration process of TI's CC330x into final product PCB. When designing your own system around the TI chipset, it is recommended to step through the guidelines outlined below.

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1 Introduction

1.1 Overview

The SimpleLink™ Wi-Fi™ CC33xx family of devices is where affordability meets reliability, enabling engineers to connect more applications with confidence. CC33xx devices are single-chip integrating both Wi-Fi 6 and Bluetooth Low Energy (BLE) 5.4. The following two devices from the CC33XX family are also pin to pin compatible:

- CC3300: A 2.4GHz Wi-Fi 6 companion IC.
- CC3301: A 2.4GHz Wi-Fi 6 and Bluetooth Low Energy 5.4 companion IC.

This guide walks through the hardware requirements and recommendations for integrating CC33xx devices.

2 Schematic Considerations

The CC33xx devices are designed to integrate easily within any system and require very few external components. The digital interface to the host processor (MPU/MCU) is highly flexible based on end application: users can decide to use any combination of secure digital I/O (SDIO), serial peripheral interface (SPI) or universal asynchronous receiver/transmitter (UART) for shared Wi-Fi and Bluetooth Low Energy communication.

The minimum requirements for optimized engine area schematic is explained in this section.

2.1 Schematic Reference Design

It is recommended to follow the provided CC33xx reference design and guidelines as close as possible to achieve the capabilities of the CC33xx listed in the device-specific data sheet as well as to pass certification. The recommended schematic design is shown from the CC330x Reference Design Files.

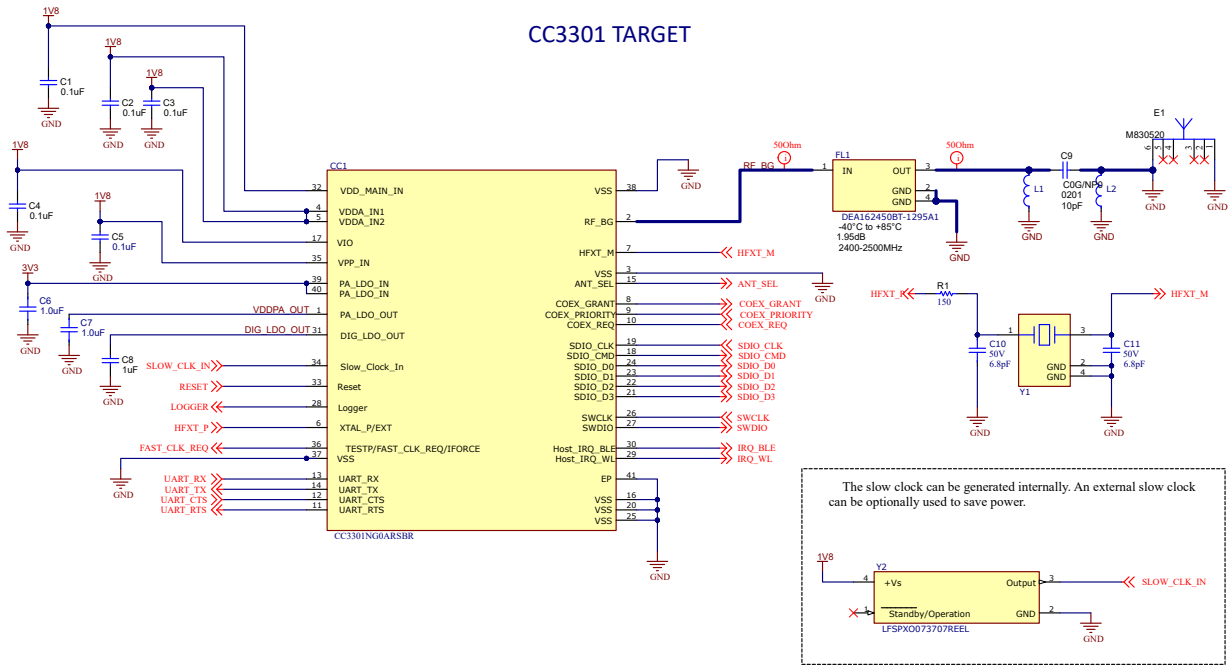

Figure 2-1. Reference Schematic of Engine Area

Table 2-1. Bill of Materials

Item	Designator of Reference	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
1	C_1, C_2, C_3, C_4, C_5	5	0.1 µF	GRM033C71A104KE14D	Murata	CAP, CERM, 0.1 µF, 10 V, ±10%, X7S, 0201 Matching component: CAP, CERM, 10 pF, 50 V, ± 5%, C0G/NP0, 0201	0201
2	C_6, C_7	2	1 µF	GRM033D70J105ME01D	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 1.0µF, X7T, +22%/-33%, 20%, 6.3V	0201
3	C_8	1	1 µF	GRM155R70J105MA12D	Murata	CAP, CERM, 1 µF, 6.3 V, ± 20%, X7R, 0402	0402
4	C_9	1	10 pF	GJM0335C1E100JB01D	Murata	CAP, CERM, 10 pF, 25 V, ± 5%, C0G/NP0, 0201	0201
5	C_{10}, C_{11}	2	6.8 pF	GJM0335C1H6R8BB01	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 6.8pF, C0G, 30ppm/°C, 0.25pF, 50V	0201
6	R1	1	150 Ω	RC0201FR-7D150RL	YAGEO	RES, 150, 1%, 0.05 W, 0201	0201

Table 2-1. Bill of Materials (continued)

Item	Designator of Reference	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
7	CC1	1		CC3301NG0ARSBR	Texas Instruments	CC3301NG0ARSBR-2.4GHz Wi-Fi 6 and Bluetooth Low Energy 5.2 Combo Transceiver	WQFN40
8	Y2	1		TZ3877AAAO44	Tai-Saw Technology	Crystal Unit SMD 2.0x1.6 40.0MHz	SMT4_2MM05_1MM65
9	FL1	1		DEA162450BT-1295A1	TDK	2.45 GHz Center Frequency Band Pass RF Filter, 100 MHz Bandwidth, 1.8 dB 0603, 3 PC Pad	SMT_FILTER_1MM60_0MM80
10	**Optional:** Y1 1	1		LFSPX0073707REEL	IQD Frequency Products	**Optional:** 32.768 kHz XO (Standard) CMOS Oscillator 1.8V Enable/Disable 4-SMD, No Lead	SMT4_2MM0_1MM6

1. The slow clock can be generated internally. An external slow clock can be optionally used to consume less power than sourcing the slow clock internally.

2.2 Power Supply

There are two power rails that must be routed to the CC33xx devices:

- 1.8 V: VDD_MAIN_IN, VDDA_IN1, VDDA_IN2, VIO, and VPP_IN
- 3.3V: PA_LDO_IN

The CC33xx device has internal LDO's for regulating the digital core, memory, and power amplifier supplies. The output of the LDO can be measured from DIG_LDO_OUT and PA_LDO_OUT. Please note that the output of PA_LDO_OUT is not enabled until firmware has been loaded onto the device.

For further information on the operating conditions for the supply pins, see Table 2-2.

Table 2-2. Required Device Power

Pin	Signal	Dir (I/O)	Required Voltage (Typical)
1	PA_LDO_OUT	O	N/A
31	DIG_LDO_OUT	O	N/A
17	VIO	I/O	1.8V
32	VDD_MAIN_IN	I	1.8V
4	VDDA_IN1	I	1.8V
5	VDDA_IN2	I	1.8V
35	VPP_IN	I	1.8V
39 and 40	PA_LDO_IN	I	3.3V

2.2.1 Power Input/Output Requirements

Supply connections are listed in descending order of criticality. Prioritize the bypass capacitor placements in this order to maximize RF performance.

- PA_LDO_OUT (pin 1) : Provide de-coupling capacitor (1.0uF)
- VDDA_IN1 (pin 4): Provide de-coupling capacitor (0.1uF)
- VDDA_IN2 (pin 5): Provide de-coupling capacitor (0.1uF)
- DIG_LDO_OUT (pin 31): Provide de-coupling capacitor (1.0uF)
- VPP_IN (pin 35): Provide de-coupling capacitor (0.1uF).
- VIO (pin 17): Provide de-coupling capacitor (0.1uF)
- VDD_MAIN_IN (pin 32): Provide de-coupling capacitor (0.1uF)

2.2.2 Power-Up Sequence

A crucial point of CC33xx device integration is that proper power-up and power-down sequences must be followed to avoid damage to the device.

- VDD_MAIN_IN and VIO must be supplied from the same source to prevent glitches on the IO during power up.
- VDDA_IN1/IN2 and PA_LDO_IN can be supplied independently of all other supplies.
- All supplies (VDD_MAIN_IN, VIO, VDDA_IN1/2, and PA_LDO_IN) must be available before Reset is deasserted (high).
- Reset pin should be held low for ~10 µs after stabilization of all external power supplies.
- When having an external slow clock, ensure that the clock is stable before Reset is deasserted (high).

2.2.2.1 SOP Modes

The Logger (pin 28) and Host_IRQ_WL (pin 29) signals are considered to be Sense on Power pins. When connecting these pins to host, ensure Host_IRQ_WL (pin 29) stay at logic level Low during power-up, and Logger (pin 28) stays at logic level High during power-up.

If the SOP pins are connected to a host that may affect the logic level of these lines, consider adding an optional pull-down/pull-up resistor(s).

2.3 Clock Source

The CC33xx device uses two clocks for operation:

- A fast clock running at 40 MHz for WLAN/BLE functions
- A slow clock running at 32.768 kHz for low power modes

The fast clock must be generated externally. The slow clock can be generated internally by the device or externally by an oscillator.

It is important to note that a deviation in clock frequency is reflected as a deviation in radio frequency. For more information on doing frequency tuning with careful selection of external loading capacitors (C_L) depending on the layout, see *Simplelink Frequency Tuning*.

2.3.1 Fast Clock

The CC330x device supports a crystal-based fast clock (XTAL). The crystal is fed directly between HFXT_P and HFXT_M pins with appropriate loading capacitors and a 150Ω resistor. See the design requirements below:

1. Provide 150Ω resistor on HFXT_P (pin 6) close to the device and before the XTAL.
2. XTAL must be connected across HFXT_P (pin 6) and HFXT_M (pin 7).
3. Provide load capacitors (6.8pF) at both the pins of the XTAL. Note that the recommended load capacitor of 6.8pF is based on TI board layout.
4. Tuning of the load capacitance may be required depending on customer board layout.

   For further guidance on this topic, see *Simplelink Frequency Tuning*.

The Fast Clock component must meet the requirements shown in Table 2-3.

Table 2-3. External Fast Clock XTAL Specifications

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Supported frequencies			40		MHz
Frequency accuracy	Initial + temperature + aging			± 25	ppm
Load Capacitance, C_L (1)		5		13	pF
Equivalent series resistance, ESR				30	Ω
Drive level			100		µW

(1) Load capacitance, C_L= [C1*C2] / [C1 + C2] + C_P, where C1, C2 are the capacitors connected on HFXT_P and HFXT_M, respectively, and C_P is the parasitic capacitance (typically 1 to 2 pF). For example, for C1 = C2 = 6.2pF and C_P = 2pF, then C_L = 5pF.

2.3.2 Slow Clock

The slow clock is generated by the device internal oscillator, but an external oscillator may be used as well.

2.3.2.1 Slow Clock Generated Internally

In order to minimize external components, the slow clock can be generated by an internal oscillator. However, this clock is less accurate and consumes more power than sourcing the slow clock externally. For this scenario the Slow_CLK_IN pin should be left not connected.

2.3.2.2 Slow Clock Using an External Oscillator

For optimal power consumption, the slow clock can be generated externally by an oscillator or sourced from elsewhere in the system. The external source must meet the requirements shown in Table 2-4. This clock should be fed into the CC330x pin Slow_CLK_IN and should be stable before nReset is deasserted and device is enabled.

Table 2-4. External Slow Clock Requirements

Parameter		Description	MIN	TYP	MAX	Unit
	Input slow clock frequency	Square wave		32768		Hz
	Frequency accuracy	Inital + temperature + aging			±250	ppm
	Input Duty cycle		30	50	70	%
T_r/T_f	Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level			100	ns
V_{IL}	Input low level		0		0.35 x V_{IO}	V
V_{IH}	Input high level		0.65 x V_{IO}		1.95	V
	Input impedence		1			MΩ
	Input capacitance				5	pF

2.4 Radio Frequency (RF)

For the CC330x family of devices, it is required to route out RF_BG (pin 2) for any radio frequency (RF) functionality. A band pass filter (BPF) is required along this path before reaching any radiative or conductive component. For the recommended BPF, see Table 2-1. It is also recommended to implement an impedance matching network (such as a 'PI' or 'L' network) for optimal RF performance. Table 2-2 is an example of schematic design for the RF path. Any deviation from these recommendations can cause performance to diverge from the data sheet specifications.

If implementing a RF switch (for utilizing antenna diversity), ensure that the RF_BG (pin 2) signal is routed through the band pass filter before the switch. The output of the band pass filter should be routed to the common port of the switch. ANT_SEL (pin 15) may be routed and used as the switching signal.

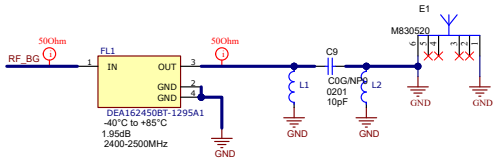

Figure 2-2. Reference Schematic for RF Section

2.5 Digital Interfaces

All IO signals on CC33xx operate at 1.8V (typical). Take in consideration the use of level shifters if utilizing a higher voltage in your system.

2.5.1 Reset

Reset (pin 33), an active low signal, should be connected and controlled by the host. If using an unhosted setup, Reset should be pulled High after power supplies are stable. For further information on power-up sequence, see Section 2.2.2.

When Reset is low, the device enters an active shutdown mode. After the device is re-enabled, firmware must be re-downloaded for proper operation.

2.5.2 Secure Digital Input Output (SDIO)

SDIO is the main host interface for wireless communication. The CC33xx device also supports shared SDIO interface for both Wi-Fi and Bluetooth Low Energy protocols.

As per the SDIO specification, the host expects these data lines to be pulled up (SDIO_D0, SDIO_D1, SDIO_D2, SDIO_03, SDIO_CMD). It is recommended to take care that any component (for example, level shifters) on the SDIO data lines do not change the state to logic-low.

2.5.2.1 SDIO Timing Diagram - Default Speed

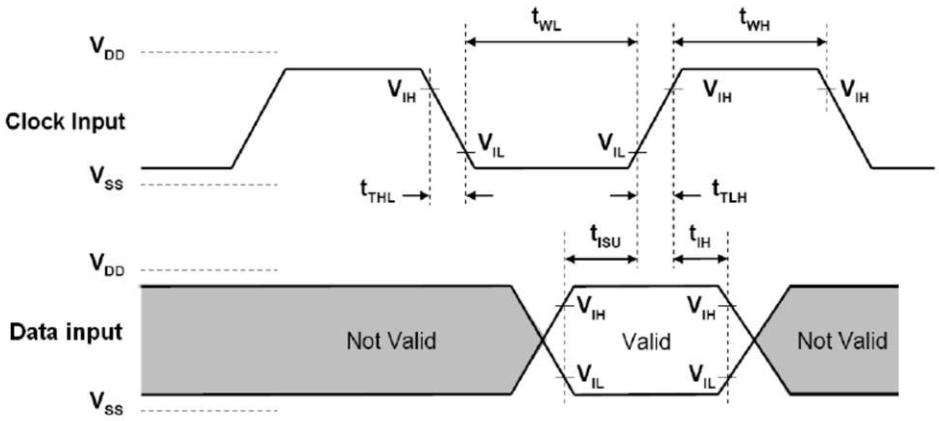

Figure 2-3. SDIO Default Input Timing

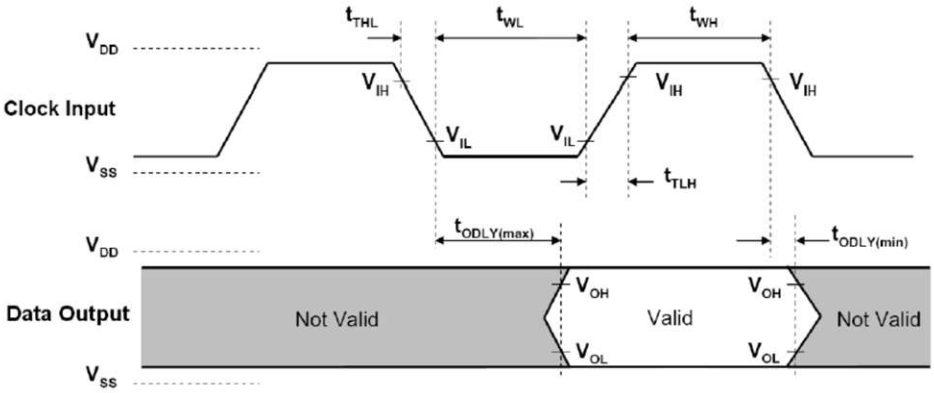

Figure 2-4. SDIO Default Output Timing

Table 2-5. SDIO Timing Parameters - Default Speed

Parameter	Description	MIN	MAX	Unit
f_{clock}	Clock frequency, CLK		26	MHz
t_{High}	High Period	10		ns
t_{Low}	Low Period	10		
t_{TLH}	Rise time, CLK		10	
t_{THL}	Fall time, CLK		10	
t_{ISU}	Setup time, input valid before CLK ↑	5		
t_{IH}	Hold time, input valid after CLK ↑	5		
t_{ODLY}	Delay time, CLK ↓ to output valid	2	14	
C_L	Capacitive load on outputs	15	40	pF

2.5.2.2 SDIO Timing Diagram - High Speed

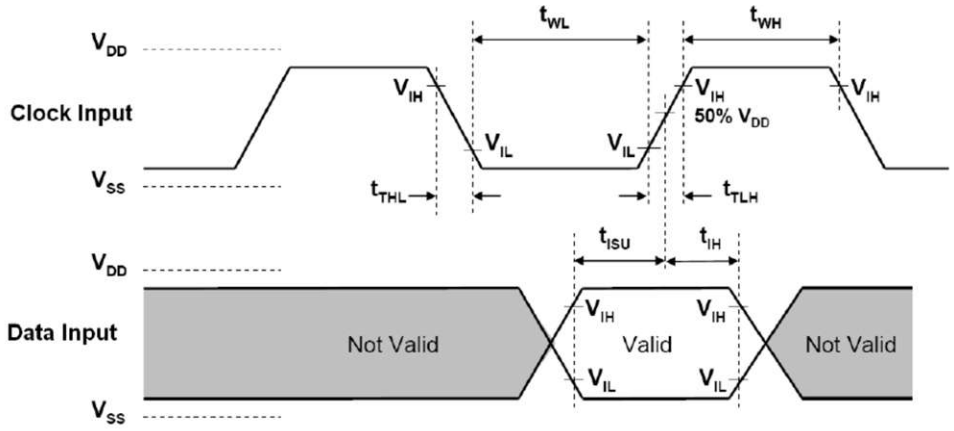

Figure 2-5. SDIO HS Input Timing

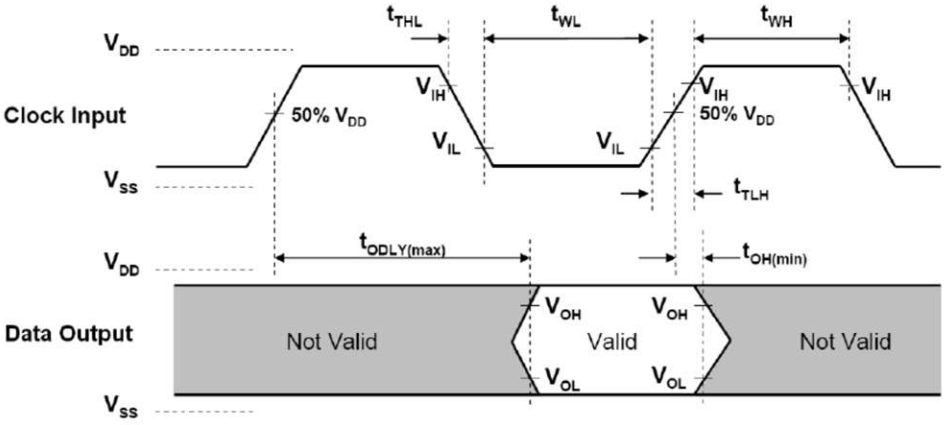

Figure 2-6. SDIO HS Output Timing

Table 2-6. SDIO Timing Parameters - High Speed

Parameter	Description	MIN	MAX	Unit
f_{clock}	Clock frequency, CLK		52	MHz
t_{High}	High Period	7		ns
t_{Low}	Low Period	7		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{ISU}	Setup time, input valid before CLK ↑	6		
t_{IH}	Hold time, input valid after CLK ↑	2		
t_{ODLY}	Delay time, CLK ↓ to output valid	2	14	
C_L	Capacitive load on outputs	15	40	pF

2.5.3 Serial Peripheral Interface (SPI)

The SPI signal lines can be used as a host interface for wireless communication. The CC330x device also supports shared SPI interface for both BLE and WLAN. The SPI lines on CC33xx include:

- SDIO_CMD (SPI PICO)
- SDIO_CLK (SPI clock)
- SDIO_D3 (SPI CS)
- SDIO_D0 (SPI POCI)

2.5.3.1 SPI Timing Diagram

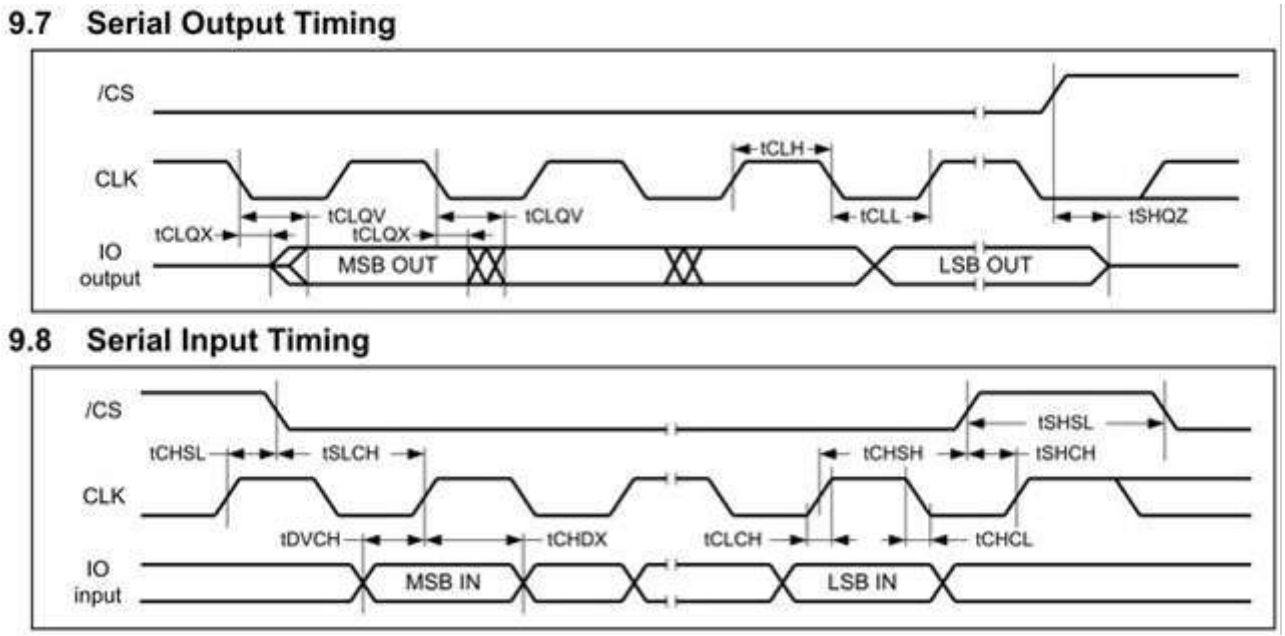

Figure 2-7. SPI Timing

Table 2-7. SPI Timing Parameters

Parameter	Description	MIN	MAX	Unit
f_{clock}	Clock frequency, CLK		26	MHz
t_{High}	High Period	10		ns
t_{Low}	Low Period	10		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{CSsu}	CS Setup time, CS valid before CLK ↑	3		
t_{ISU}	PICO, input valid before CLK ↑	3		
t_{IH}	PICO Hold time, input valid after CLK ↑	3		
t_{Dr}, t_{Df} - Active	Delay time, CLK ↑/↓ to output valid	2	10	
t_{Dr}, t_{Df} - Sleep	Delay time, CLK ↑/↓ to output valid		12	
C_L	Capacitive load on outputs	15	40	pF

2.5.4 Universal Asynchronous Receiver-Transmitter (UART)

UART is the main host interface for BLE, which supports host controller interface (HCI) transport layer. When UART is to be used with a host, take care to connect them correctly:

- Pin 14 is the UART_TX of the device, and must be connected to Host side RX
- Pin 13 is the UART_RX of the device, and must be connected to Host side TX
- Pin 12 is the UART_CTS of the device, and must be connected to Host side RTS
- Pin 13 is the UART_RTS of the device, and must be connected to Host side CTS

Table 2-8. UART Timing Parameters

Parameter	Condition	MIN	TYP	MAX	Unit
Baud rate		37.5		4364	kbps
Baud rate accuracy per byte	Receive/Transmit	-2.5		+1.5	%
Baud rate accuracy per bit	Receive/Transmit	-12.5		+12.5	%
CTS low to TX_DATA on		0	2		ms
CTS high to TX_DATA off	Hardware flow control			1	Byte
CTS high pulse width		1			bit
RTS low to RX_DATA on		0	2		ms
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	Byte

2.5.5 Serial Wire Debug (SWD)

The two serial wire debug pins on CC33xx include SWCLK (pin 26) and SWDIO (pins 27). These signals are used for various types of debug (such as RF testing) and should be routed to test points for troubleshooting.

2.5.6 Coexistence

The coexistence feature is a means to organize wireless packet traffic for communication protocols operating in the same frequency band. CC33xx behaves as the Coex primary device and communicates to the Coex secondary device. CC33xx supports a three-wire Packet Traffic Arbitration (PTA) interface for coexistence. The coexistence signals on CC33xx include:

- COEX_GRANT (pin 8) - an input signal, controlled by the Coex primary device. Indicates the response of the PTA decision.
- COEX_PRIORITY (pin 9) - an output signal, controlled by the Coex secondary device. Indicates the priority of a request signal.
- COEX_REQ (pin 10) - an output signal, controlled by the Coex secondary device. Indicates a request to use the shared frequency band.

These three signals on CC33xx should be routed to the matching coexistence pins on the Coex secondary device. Coexistence is enabled by default and can be configured between internal and external in the INI file. Coexistence can be implemented with either one antenna (for both the primary and secondary device) or two antennas for each device. Figure 2-8 and Figure 2-9 provide visual examples of utilizing the coexistence feature with a Bluetooth Low Energy device.

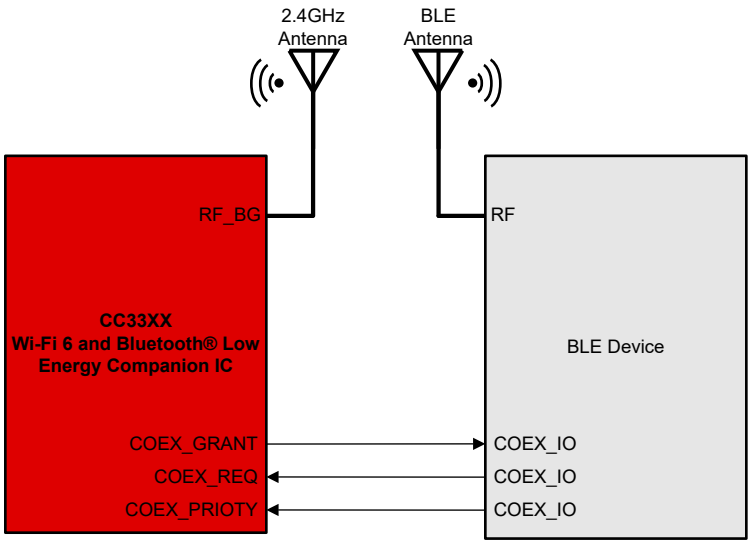

Figure 2-8. CC33xx Coexistence With Dual Antennas

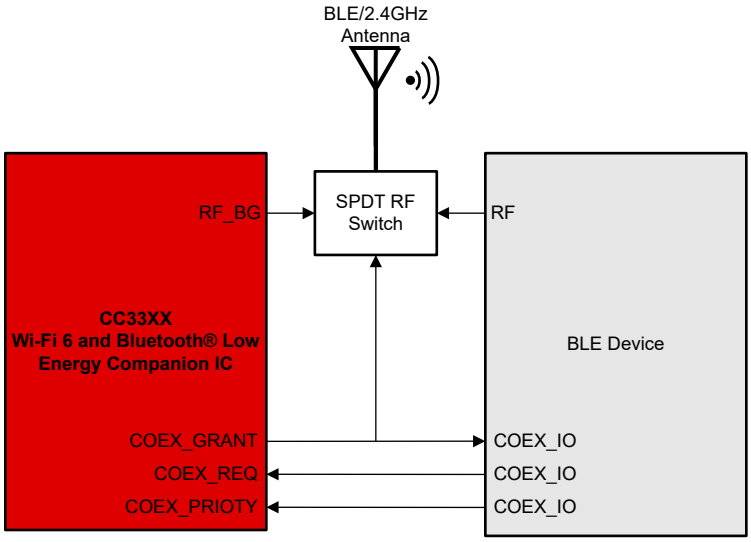

Figure 2-9. CC33xx Coexistence With Single Antenna

3 Layout Considerations

The CC33xx devices are designed to integrate easily within any system and require very few external components. The digital interface to the host processor (MPU/MCU) is highly flexible based on end application: users can decide to use any combination of SDIO, SPI or UART for shared Wi-Fi and BLE communication.

The minimum requirements for optimized engine area layout is explained in this section.

3.1 Layout Reference Design

It is recommended to follow the provided reference design and guidelines as close as possible in order to achieve the capabilities of the CC33xx listed in the data sheet as well as to pass certification. These layout guidelines are especially important in the engine area, which includes the sensitive RF components and traces.

The following designs incorporate the layout guidelines given throughout this document. Refer to these as reference sources:

- CC330x Reference Design
- BP-CC3301
- M2-CC3301

The figures below include the engine area of CC33xx on the top layer (layer 1) and ground layer (layer 2) for all three designs.

Before proceeding with any hardware build involving the CC33xx, it is recommended to submit the design for review. Note that the engine area as shown in the reference design can be rotated as necessary according to the design requirements.

3.1.1 Reference Design Layout

Figure 3-1 is sampled from the CC330x reference design files.

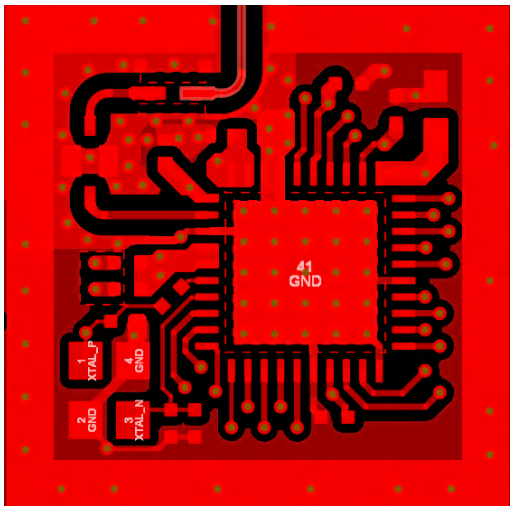

Figure 3-1. Reference Design, Top (Layer 1)

Figure 3-2 is sampled from the CC330x reference design files.

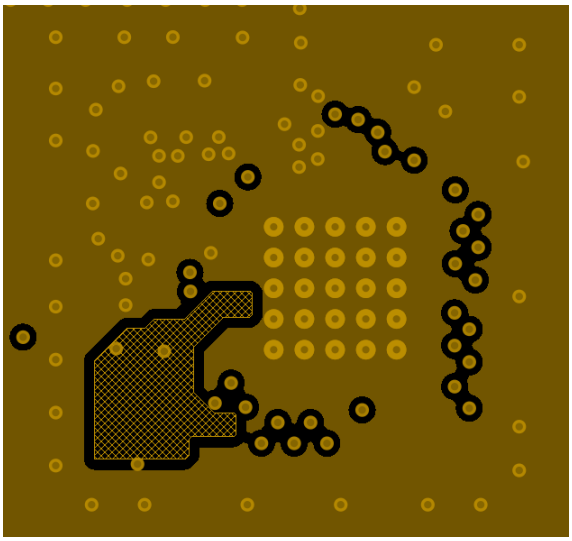

Figure 3-2. Reference Design, Ground (Layer 2)

3.1.2 BP-CC3301 Design Layout

Figure 3-3 is sampled from the BP-CC3301 design files.

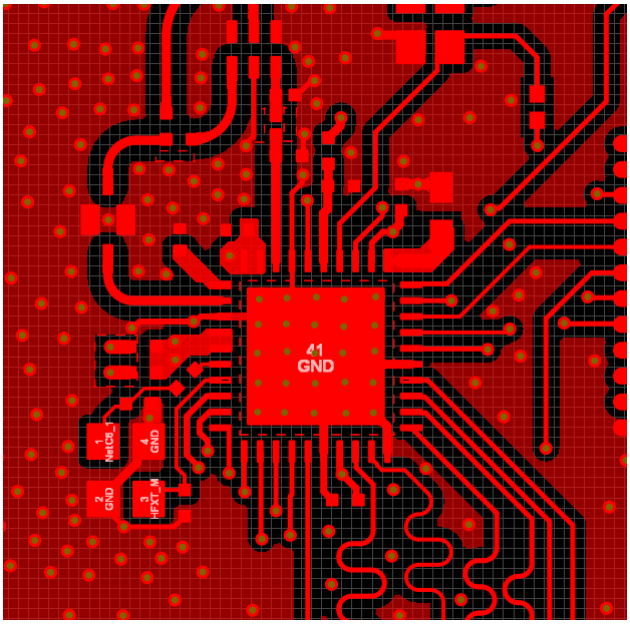

Figure 3-3. BP-CC3301 Layout , Top (Layer 1)

Figure 3-4 is sampled from the BP-CC3301 design files.

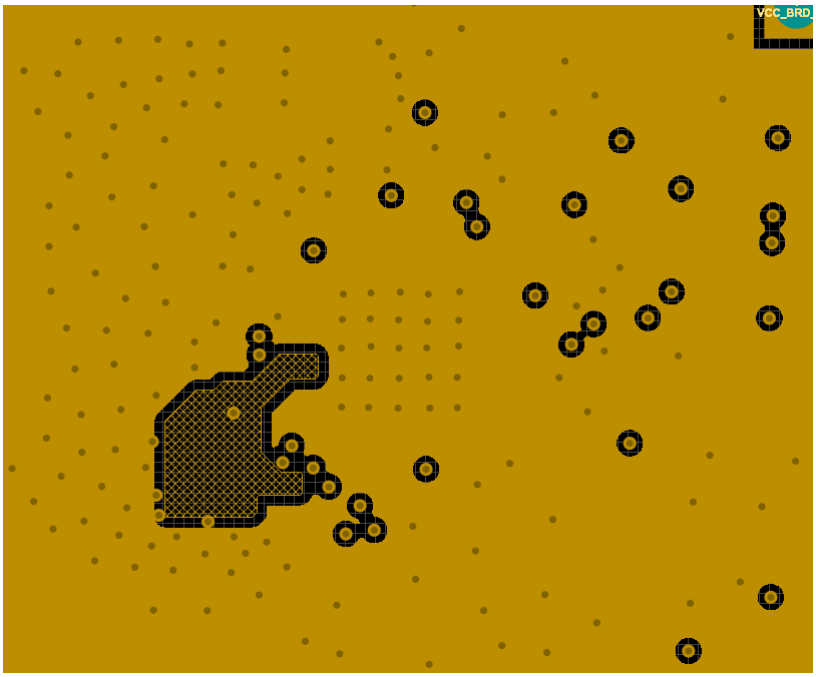

Figure 3-4. BP-CC3301 Layout, Ground (Layer 2)

3.1.3 M2-CC3301 Design Layout

Figure 3-5 is sampled from the M2-CC3301 design files.

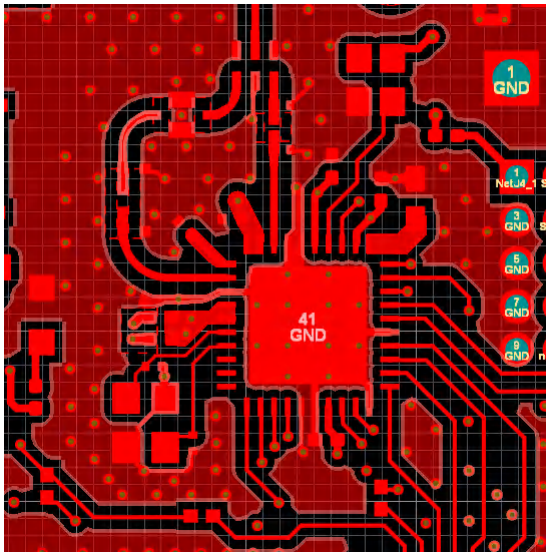

Figure 3-5. M2-CC3301 Layout, Top (Layer 1)

Figure 3-6 is sampled from the M2-CC3301 design files.

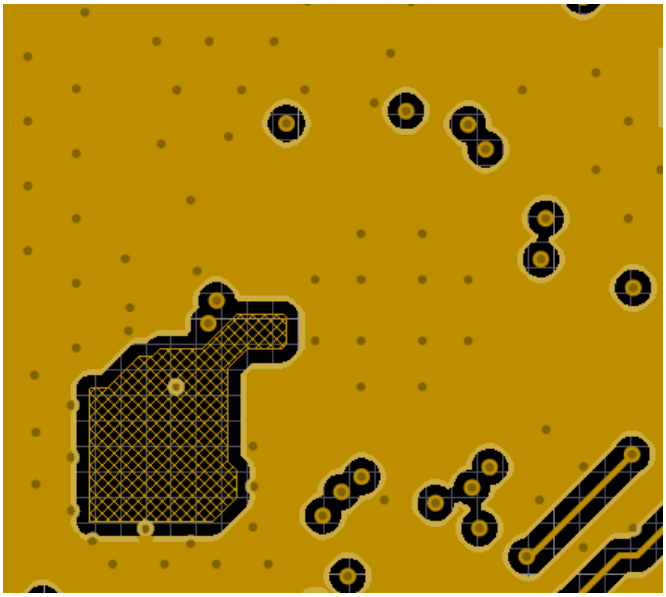

Figure 3-6. M2-CC3301 Layout, Bottom (Layer 2)

3.2 IC Thermal Pad

Underneath the IC, there should be one continuous ground plane on the top layer with 25 vias evenly distributed as shown in the Figure 3-7. This is important for thermal dissipation and optimal RF performance.

Figure 3-7 is sampled from the CC330x reference design files.

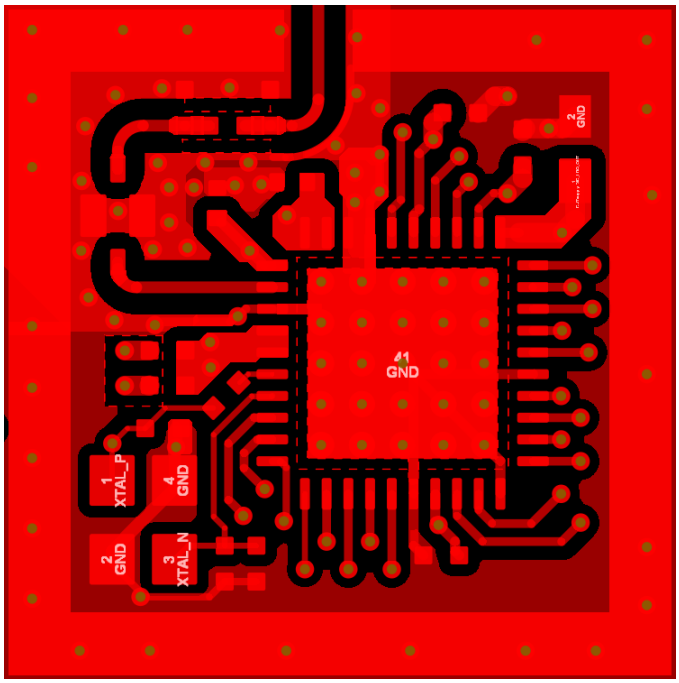

Figure 3-7. Reference Design Thermal Pad

3.3 Radio Frequency (RF)

Figure 3-8 below shows the RF section as it appears on the reference design. Special care must be taken when designing this area of the layout in order to achieve peak performance. A poor layout can cause performance degradation for the output power, EVM, sensitivity, and spectral mask.

Figure 3-8 is sampled from the CC330x reference design files.

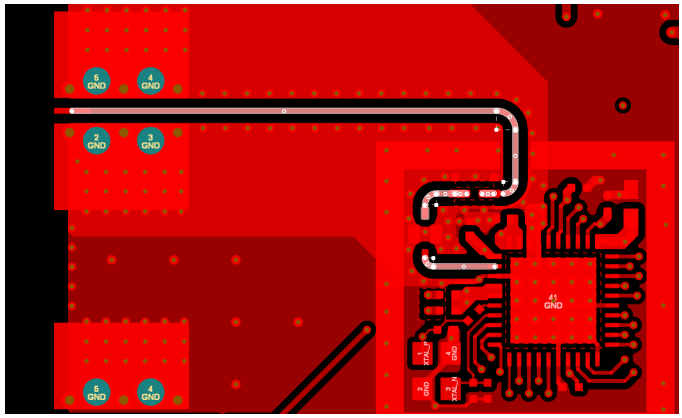

Figure 3-8. Reference Design RF Path

In addtion to following the reference design as close as possible, please comply with the guidelines listed below.

- The RF trace should have a constant 50 Ω characteristic impedance. This is achieved by matching the CPWG based on the dielectric, layer stackup, ground plane spacing, and trace thickness. These parameters should be consistent throughout the length of the trace.

- The entire RF trace should only be on the top layer of the PCB, and the layer immediately underneath should be one constant ground plane (with the exception of the XTAL cutout) for the trace reference.
- The RF trace should be as clean and straight as possible with no components besides the band pass filter and matching filter before the antenna. This is to avoid unwanted component to component coupling. If a straight RF trace is not possible, rounded curves are acceptable.
- The RF trace should be as isolated as possible from other components to decrease noise. Ground planes should surround the RF trace, and distance between ground via stitching should be less than 1/8th of the minimum wavelength.
- The band pass filter should be as far as possible (within design space limits) from the RF_BG pin (pin 2) and the VDDA decoupling capacitors on pins 4 and 5.
- A ground via should be placed between the two ground pads for the band pass filter (BPF). The ground plane on both sides of the BPF should be connected to enable one common ground plane for the entire area. There should be increased ground via stitching in the ground plane between the BPF and the PA_LDO_OUT decoupling capacitor (pin 1).
- There should be no high frequency signal traces or test points close to the RF trace.

Another impactful factor in RF performance is the stackup. As an example, Table 3-1 contains the stackup (from top to bottom) used in the BP-CC3301 design.

Table 3-1. Stackup (from top to bottom) Used in all CC33xx EVMs

Layer	Name	Thickness	ε_r
	Top Soldermask		
	Top Solder	1.00 mil	3.5
1	Top Layer	1.85 mil	
	Dielectric 1	5.48 mil	4.2
2	L02_GND	1.26 mil	
	Dielectric 2	42.82 mil	4.2
3	L03_PWR	1.26 mil	
	Dielectric 3	5.48 mil	4.2
4	Bottom Layer	1.85 mil	
	Bottom Solder	1.00 mil	3.5
	Bottom Soldermask		

The RF signal from the device is routed to the antenna using a coplanar waveguide (CPW-G) structure. This structure offers the maximum isolation across the filter gap, and the best possible shielding to the RF lines. It is imperative to take in account the stackup and trace measurements in order to achieve a 50 ohm impedance. Figure 3-9 and Figure 3-10 illustrate examples of calculating trace impedance using the BP-CC3301 EVM as an example.

This image is sampled from the BP-CC3301 design files.

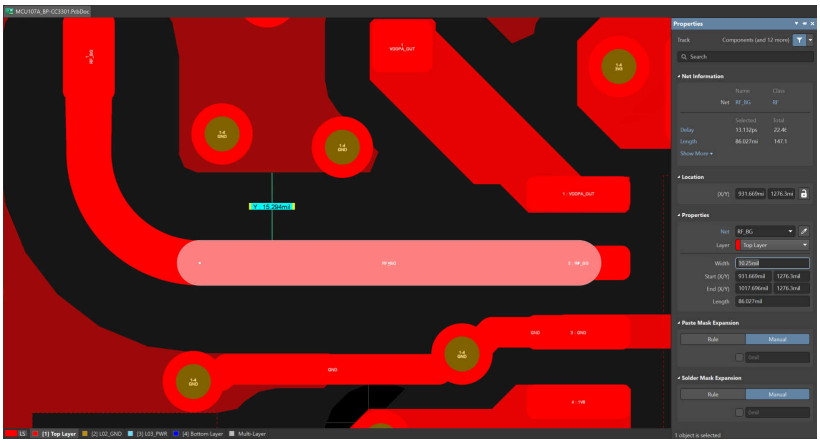

Figure 3-9. Example of Taking RF Trace Measurements

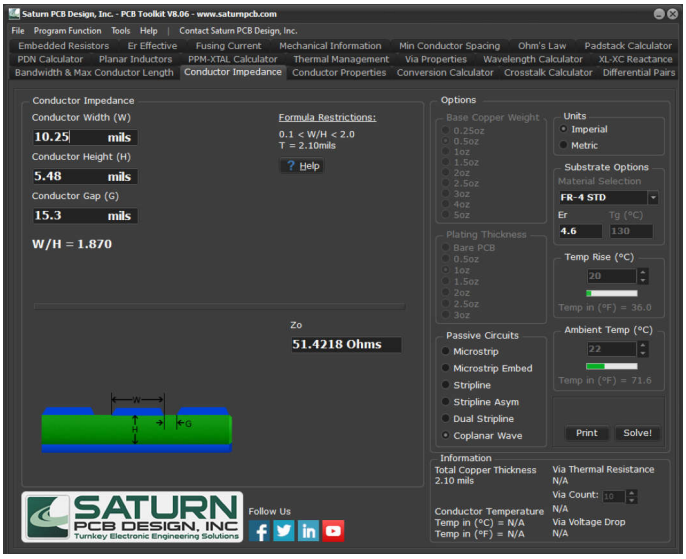

Figure 3-10. Example of Calculating Trace Impedance

3.4 XTAL

Figure 3-11 shows the placement and layout around the 40 MHz XTAL and its connections to the CC33xx IC.

Figure 3-11 is sampled from the BP-CC3301 design files.

Figure 3-11. 40MHz XTAL From BP-CC3301

When integrating the XTAL, please follow these guidelines:

- The traces connecting the XTAL to the CC3301 (XTAL_P and XTAL_M) be as short as possible with matching trace length.
- Place a 150 Ω resistor on the XTAL_P pin as close as possible to the CC33xx.
- The two loading capacitors should be parallel to the edge of the XTAL.
- On layer below the crystal (layer 2), place a cutout underneath the area of the XTAL and the loading capacitors. Check on the layer below that (layer 3) has good ground underneath the same area. For a visual representation, see Figure 3-12.
- Wherever possible, there should be increased ground via stitching around the XTAL for optimal isolation.

Figure 3-12 is sampled from layer 3 of the M2-CC3301 design files.

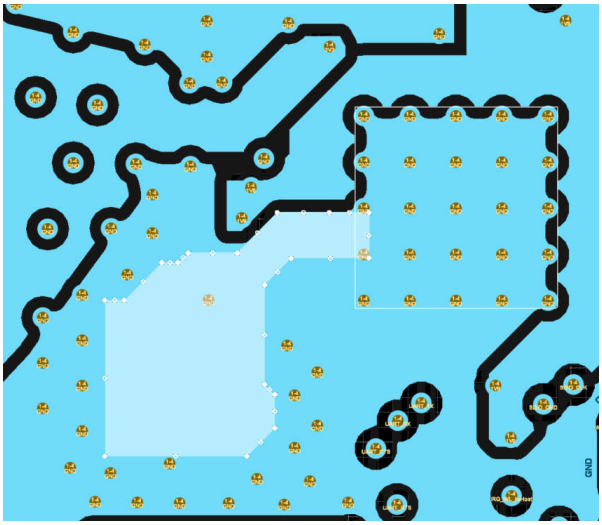

Figure 3-12. Reference Layout for Layer Under XTAL Cutout

3.5 Power Supplies

The power supplies, ground traces, and the decoupling capacitors are important for having an optimal layout. Since the decoupling capacitors can be close to the RF pins and traces of the device and power supplies, traces must be thick enough to support the necessary current to the device.

- PA_LDO_OUT (pin 1): It is suggested to have the decoupling capacitor close to the device pin, as well as a thick enough trace to have a low impedance path to the capacitor. For a visual representation, see Figure 3-13.
- VDDA_IN1 and VDDA_IN2 (pins 4 and 5): The supply side of the decoupling capacitors must be shorted together with a polygon region with two power vias (one for each decoupling capacitor). The ground side of each capacitor must go directly to ground by separate vias (not shorted together), and be isolated from the rest of the ground plane on the top layer.
- For the 1.8V power delivery, a thick trace or power plane must be used to carry the required amount of current consumption in VDD_MAIN_IN, VIO, VDDA_IN1, VDDA_IN2, and VPP_IN combined. For max current consumption, see Table 2-2.
- The 1.8V path must be located around the device on a layer that is not the top layer or ground layer (place it on layer 3 or 4). This way the power path cannot interrupt the RF trace on top layer (layer 1) or the continuous ground layer (layer 2). Only one via is used for each 1.8V power supply, the 1.8V supply currents must not flow under the device.
- For the 3.3V power delivery, a thick trace or a power plane must be used to carry the required amount of current consumption of the PA_LDO_IN. For more information, see Table 2-2. The power delivery must also be placed on a layer that is not top layer or ground layer (layer 3 or 4).
- PA_LDO_IN (pins 39 and 40): These two pins must be shorted together with a solid region. The decoupling capacitor should be placed close to the device. Use two vias if possible to deliver the 3.3V rail.
- The ground for pin 37 and 38 must be shorted together with a solid region. This solid region should be connected to the IC thermal ground pad.
- The ground for pin 3 must be shorted to the thermal pad under the IC and to the ground plane that is adjacent to the RF trace.

Figure 3-13 is sampled from the BP-CC3301 design files.

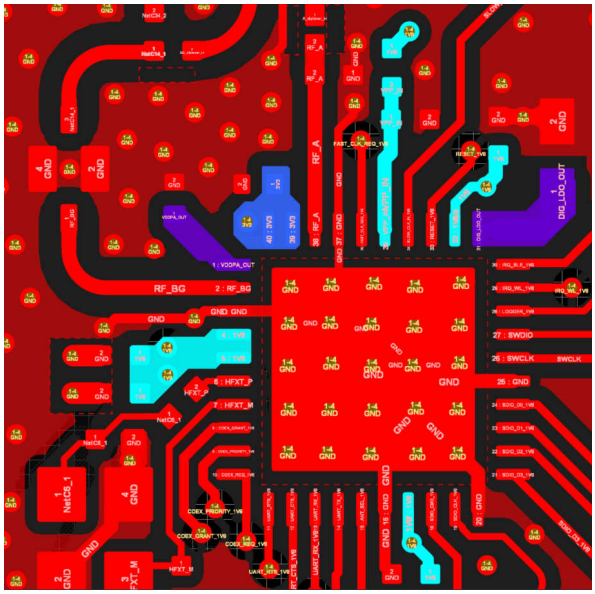

Figure 3-13. Reference Layout of CC33xx Power Supplies

Figure 3-14 is sampled from the M2-CC3301 design files.

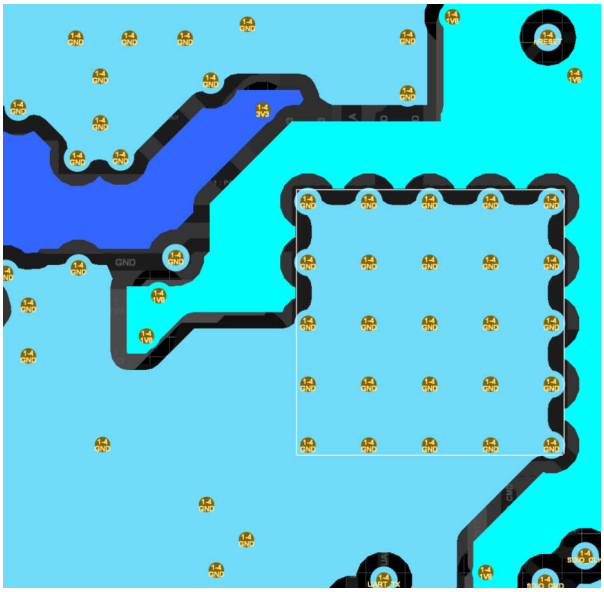

Figure 3-14. Reference Layout of the Power Layer

3.6 SDIO

SDIO is the main communication interface with the host processor for WLAN functions, and can also be used for BLE functions in shared SDIO protocols. These signals are especially sensitive because of the clock, and should be designed as such.

The SDIO lines include SDIO_CLK, SDIO_CMD, SDIO_D0, SDIO_D1, SDIO_D2, and SDIO_D3. The SDIO_CLK signal in particular is very sensitive and should be regarded as such. In order to ensure reliable SDIO communication, the following layout considerations should be taken into account:

- It is recommended that the SDIO lines have at least 5mils of width.
- The SDIO traces should be as far away as possible from the other digital or analog signal traces.
- It is recommended to add ground shielding around the SDIO bus.

- The SDIO_CLK must be isolated from all other signals with ground vias (stitching vias) and adjacent ground planes. The signal trace should have a clearance of at least twice the trace width of the other SDIO signals.
- Route the SDIO lines in parallel to each other with lengths as short as possible (to decrease propagation delay), and have a clearance of 1.5x the trace width.
- The lengths of the SDIO traces must be length matched within 20 mil tolerance to provide the sampled data at the same time on all of the traces. For a visual example of length tuning, see Figure 3-15.

Figure 3-15 is sampled from the BP-CC3301 design files.

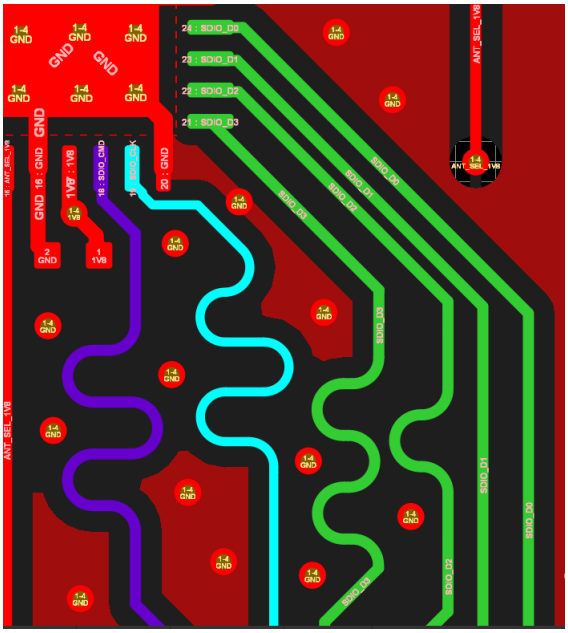

Figure 3-15. Reference Layout for SDIO Signals

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