CC1020 Errata Note 001, rev. 1.0

Improved ESD protection requires changes in matching network and register values for optimum performance.

Description and reason for the problem

Improved ESD protection on I/O pins alters the input/output impedance slightly. In order to maintain optimum performance the antenna matching circuit at 868/915 MHz should be changed. An external switch should be used also at 868/915 MHz, similar to the recommended circuit for 433 MHz. The new reference design for 868/915 MHz is available as CC1020EMX-868.

SmartRF Studio rev. 4.8 should be used to get optimum register values for the new chip revision.

For the old chip revision, SmartRF Studio rev. 4.7 should be used, and the chip can be evaluated using the CC1020EM-868 design.

If the new chip is used with the "old" CC1020EM-868 reference design, a sensitivity degradation up to 10 dB could be experienced compared to using the external switch. The degradation depends on supply voltage. The MATCH register should then be set to 0x00. Otherwise the SmartRF Studio rev. 4.8 should be used to get register values.

Suggested modifications

1. Use a T/R switch as shown in application circuit (Data Sheet, rev. 1.3), and CC1020EMX-868 reference design
2. Use new register values given by SmartRF Studio rev. 4.8

Batches affected

This errata note applies to all chip batches and revisions of the chip with date code 0317 and onwards. The date code can be found on the top of the chip as "YYWW", where WW is calendar week and YY is last to digits in year.

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CC1020 Errata Note 002, rev. 1.0

Carrier sense squelch function must be turned off in transmit mode in order to enable the DCLK signal.

Description and reason for the problem
If the DCLK squelch is used (enabled by setting INTERFACE.DCLK_CS = 1), this will prevent the DCLK from operating in TX mode if not disabled.

Suggested software work-around
1. Disable DCLK squelch when in TX mode by setting INTERFACE.DCLK_CS = 0 before entering TX mode

Batches affected
This errata note applies to all chip batches and revisions of the chip.

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CC1020 Errata Note 003, rev. 2.0

February 21, 2005

High output power on the CC1020EMX-433 v1.0 (402 – 470 MHz) reference design leads to voltage levels exceeding maximum operating conditions causing a power drop with time in many usage scenarios.

Description and reason for the problem

When using high output power settings with the CC1020EMX-433 v1.0 the recommended maximum voltage level on the RF_OUT pin (pin 21) is exceeded. This may cause a drop in output power over time, particularly if the transmit duty cycle is high. Power drop has only been observed on the 402 – 470 MHz version of the reference design (i.e. the CC1020EMX-433 v1.0) as the 804 – 940 MHz version has a considerably lower voltage swing during transmit.

For the CC1020EMX-433 v1.0 operating at 3.0 V, 402 – 470 MHz, with an output power of +10 dBm, the output power has been observed to drop by more than 3 dB over weeks with continuous transmit operation. The majority of the power drop occurs during the first hours. For operation above 3.0 V the drop can be slightly worse, while for supply voltages lower than 3.0 V, the drop will be less.

The output power drop will not cause any serious damage to the chip, nor will it affect device reliability. Accelerated lifetime tests of CC1020 at 125 °C for more than 1000 hours have been completed, and show no degradation. The output power drop was unveiled at room temperature.

For future designs, Chipcon recommends using the most recent CC1020EMX reference design (v2.0 or higher), which is available on web at www.chipcon.com. The matching components for this reference design are shown in *Figure 1*. For 804 – 940 MHz, no changes to legacy v1.0 based designs are necessary. However, the resistor R10, as shown in *Figure 1,* will be included in all future CC1020EMX reference designs (please note that from v2.0 there is one common PCB design supporting all of the 433/868/915 MHz frequency bands).

By lowering the load impedance “seen” by the CC1020 power amplifier, the output power drop is avoided. The series resistor R10 is added to reduce the DC voltage at the RF_OUT pin. Finally, for the CC1020EMX-433 the filter topology has been changed from a π-type filter to a T-type filter in order to achieve a better combination of reflection factors for the harmonics. This change applies to the 433 MHz frequency only. Altogether, these changes, which are implemented in the new CC1020EMX reference design v2.0, remedy the output power drop problem. The new solution increases the current consumption in transmit mode by typically 3 mA at maximum output power.

Solution

Copy the CC1020EMX reference design v1.1 (4-layer), v2.0 (2-layer) or newer.

Description of the new matching network

A schematic diagram of the input/output matching networks for the CC1020EMX reference design v2.0 is shown in *Figure 1*.

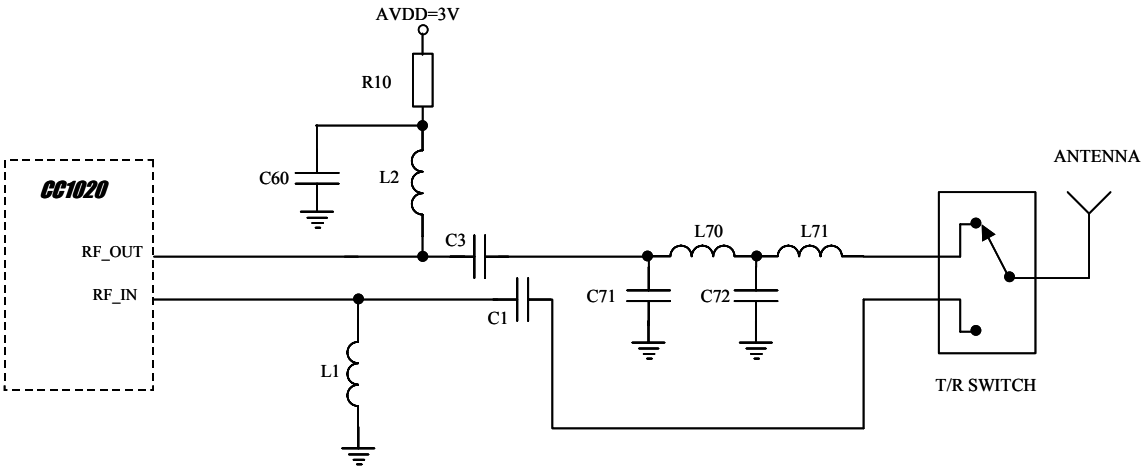

Figure 1: Schematic diagram of the input/output matching network

The corresponding component values of the CC1020EMX reference design v2.0, which is a 2-layer reference design with single-sided assembly, can be found in *Table 1*. It should be noted that all inductors used in the RF matching network are 0402 low-cost multilayer inductors.

Item	433 MHz	868 MHz	915 MHz
C1	10 pF, 5%, NP0, 0402	47 pF, 5%, NP0, 0402	47 pF, 5%, NP0, 0402
C3	5.6 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402
C60	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402
C71	DNM	8.2 pF 5%, NP0, 0402	8.2 pF 5%, NP0, 0402
C72	4.7 pF, 5%, NP0, 0402	8.2 pF 5%, NP0, 0402	8.2 pF 5%, NP0, 0402
L1	33 nH, 5%, 0402	82 nH, 5%, 0402	82 nH, 5%, 0402
L2	22 nH, 5%, 0402	3.6 nH, 5%, 0402	3.6 nH, 5%, 0402
L70	47 nH, 5%, 0402	5.1 nH, 5%, 0402	5.1 nH, 5%, 0402
L71	39 nH, 5%, 0402	0 Ω resistor, 0402	0 Ω resistor, 0402
R10	82 Ω, 5%, 0402	82 Ω, 5%, 0402	82 Ω, 5%, 0402

Table 1: Component values for CC1020EMX-433/868/915 MHz

Batches affected

This errata note applies to all chip batches and revisions of the chip.

Document History

Revision	Date	Description/Changes
1.0	2004-03-19	First edition.
2.0	2005-02-21	Updated Errata Note 003, incl. *Figure 1* and *Table 1*, to reflect the most recent reference design. Removed two of the previously suggested alternatives. Added document history.

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CC1020 Errata Note 004, rev. 1.0

March 14, 2005

When performing PLL calibration it has been verified that waiting at least 100 µs after initiating the calibration is necessary to avoid an unreliable PLL calibration result. Still, there exists a small, but finite probability that the CC1020 PLL will not LOCK. Checking LOCK and recalibrating if LOCK is not achieved is therefore necessary.

Description and reason for the problem

CC1020 PLL calibration and lock can be monitored using one of the following methods:

Method A:

1. Start calibration
2. Monitor [STATUS.CAL_COMPLETE]
3. Monitor [STATUS.LOCK_CONTINUOUS]

or

Method B:

1. Start calibration
2. Monitor [STATUS.CAL_COMPLETE]
3. Monitor LOCK pin

When using a 14.7456 MHz crystal frequency the CC1020 calibration (monitored by steps 2 and 3) typically lasts 27 ms. However, it has been observed that the CAL_COMPLETE indicator in the STATUS register is unreliable during the first 100 µs after initiating the calibration. As a result step 2 might indicate calibration complete too early, i.e. before the actual calibration has actually completed. In such a situation step 3 (LOCK monitoring) is executed during instead of after calibration. In order to avoid this inconsistency, a waiting period of at least 100 µs between calibration start and the start of the polling should be applied using one of the following methods:

Method A:

1. Start Calibration
2. Wait at least 100 µs before starting to monitor [STATUS.CAL_COMPLETE]
3. Monitor [STATUS.LOCK_CONTINUOUS]

or

Method B:

1. Start Calibration
2. Wait at least 100 µs before starting to monitor [STATUS.CAL_COMPLETE]
3. Monitor LOCK pin.

Calibration starts when CALIBRATE.CAL_START is set to 1 as shown in figure 1. The PLL is then set to open loop and the internal VCO control voltage set to a value given by CALIBRATE.CAL_ITERATE[2:0] = 4_h. Based on this value a capacitor array is selected and when the calibration is completed the PLL loop is closed.

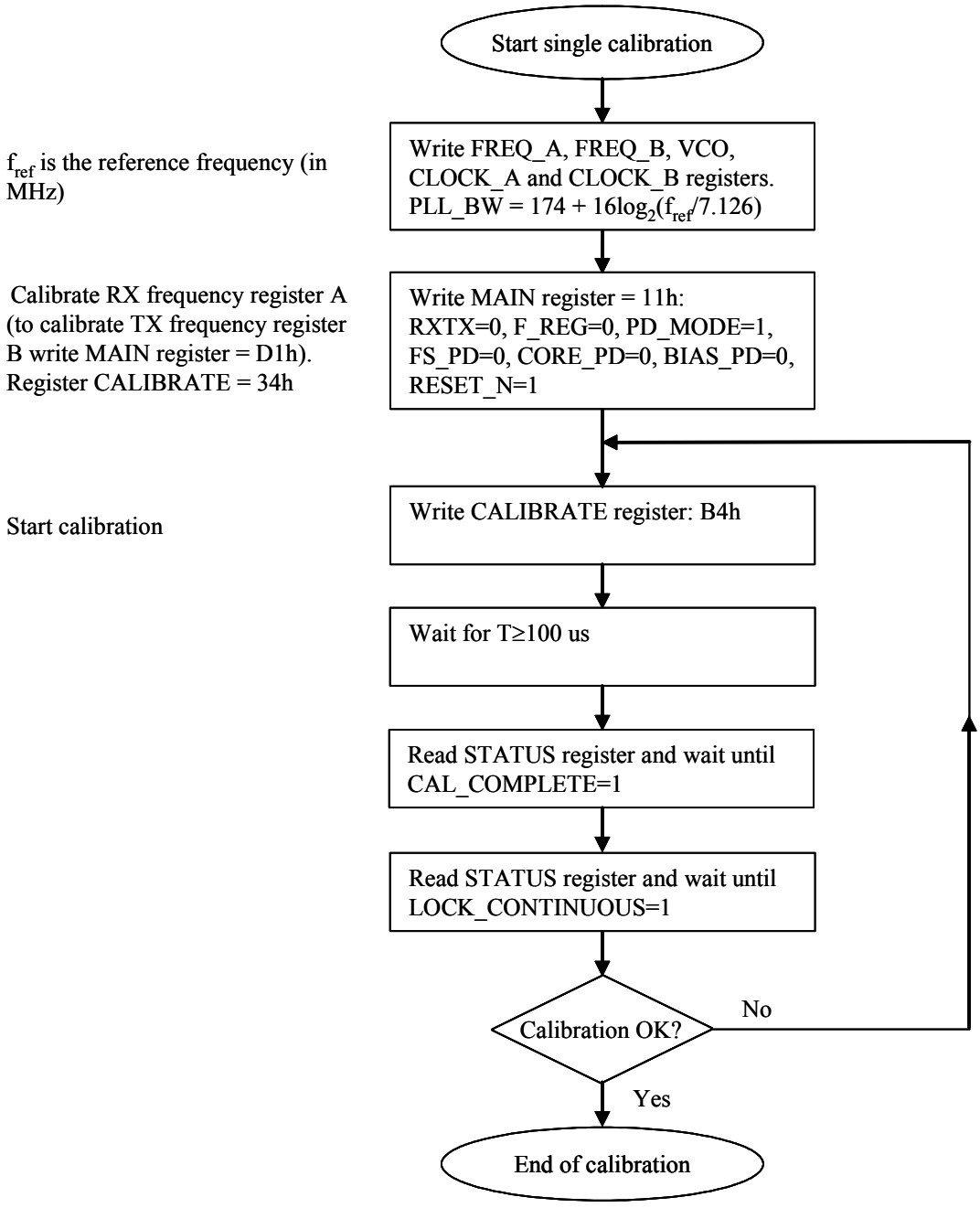

Figure 1: Recommended PLL calibration procedure

In less than 10 ppm of all PLL calibrations performed it was observed that CC1020 did not achieve LOCK even when introducing a 100 µs wait period before polling of [STATUS.CAL_COMPLETE] was initiated. The reason for no LOCK still occurring, even when calibrating the PLL with this small wait period, is due to the PLL calibration procedure making an erroneous frequency measurement causing the PLL calibration algorithm to choose a wrong capacitor array setting producing a no LOCK situation. For this reason it is important to control that the PLL calibration achieves LOCK and recalibrate if it does not.

Suggested workaround

For those users who have not already implemented a recalibration procedure in software it is strongly recommended to avoid polling [STATUS.CAL_COMPLETE] until 100 µs has elapsed following calibration start, then monitor LOCK after calibration complete and, if LOCK is not achieved, recalibrate until LOCK is successfully achieved. The recommended calibration procedure, including recalibration, is provided in figure 1.

High Reliability Applications

In high reliability applications recalibration should be performed frequently and always when retransmitting packets.

Batches affected

This errata note applies to all chip batches and revisions of the chip.

Document History

Revision	Date	Description/Changes
1.0	2005-03-14	First edition.

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