TMDSEVM6657 SCHEMATIC

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	0.6	Initial Draft	03-FEB-2012
	1.1	Release for Alpha Boards	20-MAR-2012
2.0	2.5	Release for Beta Boards	26-JUL-2012
	2.9	Redundant pull-up and termination NU on EMU_TCK	28-NOV-2013

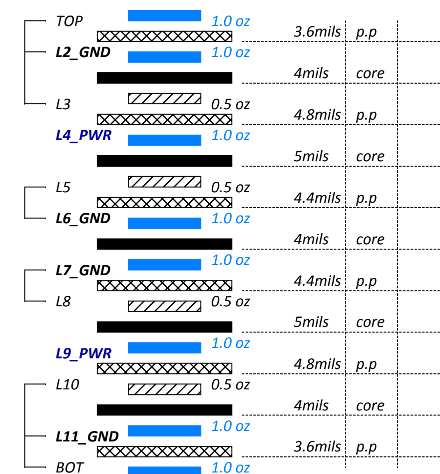
I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
EEPROM1	DSP EEPROM	0x50, 0x51
U264	ETHERNET EEPROM	0x50

PCB MECHANICAL DETAILS :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4_IT168G
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

PCB LAYER STACK-UP DETAILS :



NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

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SCHEMATIC PAGE DESCRIPTION :

01 : COVER PAGE
02 : TABLE OF CONTENTS
03 : SYSTEM BLOCK DIAGRAM
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17 : DSP - MISC
18 : DSP - CLOCK & SMART REFLEX
19 : CLOCK GENERATION
20 : USB - JTAG
21 : GIGABIT ETHERNET
22 : FPGA - POWER, RESET CTRL, McBSP
23 : FPGA - BOOT_MODE & SMART REFLEX
24 : DSP - POWER 1
25 : DSP - POWER 2
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27 : POWER SUPPLY 1
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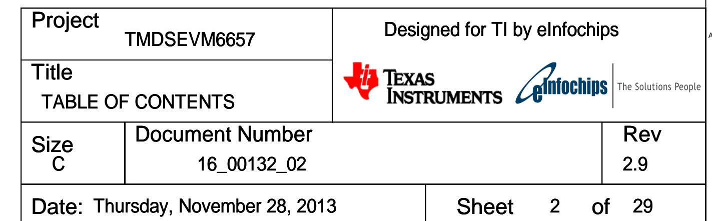
29 : REVISON HISTORY



BLOCK DIAGRAM

Connectors
ICs

2KB EEPROM (24LC02B-I/ST)

JACK (101112FHBMAM 404ZA)
10/100/1000 Mbps

Gigabit Eth PHY 88E1112
F_Px I2C S_Px MDI
MDIO 3.3V

SGMII 4
LVL TXL (PCA9306)

AMC_SGMII x 1 4

DDR3 (ECC) 128M X16 (MT41J128M16HA-125) 4
DDR3-1600 128M X16 (MT41J128M16HA-125) 32 32

NAND Flash 128M X8 (MT29F1G08ABCHC) 14 48 48

TEST HDR SFM-150-L2-S-D-LC
DSP_I2C 2
DSP_SPI 4
GPIO [15:14] 2
4 4 14 14 10
McBSP_Clk/FS (from FPGA)
McBSP_Data 4 (from AMC)

3 Pin Header
RS-232 (MAX3221)
DSP_UART
LVL TXL (SN74AVC4T245) 2

XDS100- On Board Emulator
Mini-USB
USB-JTAG (FT2232H)
LVL TXL (TXS0108) 1.8V
SWITCH (TS3L301) 2
USB_JTAG
3.3V_JTAG
AMC_JTAG
SWITCH (TS3L301)

TI 60-Pin Header (SOLC-115-02-S-Q-A-K)
SEL_LOGIC
JTAG, EMU[0:1]
EMU[2:17]

GAUSS (TMS320C6657)
EMAC
MDIO
DDR3A
EMIF16/ UPP
UART1
Timer[1:0]
McBSP[1:0]
UART0
JTAG,EMU[1:0]
EMU[17:2]
SRIO X4
PCIe X2
I2C
SPI
GPIO[15:0]
RESET & INTERRUPT
PCIe Clk
HyperLink, DDR, SRIO, Core Clks

24 Hyperlink 50Gbps
HyperLink CONN 768670011

SRIO X4 16
PCIe X2 8
DSP_I2C 2
LVL TXL (PCA9306)
128KB EEPROM (AT24C1024B)

AMC (170 pins)
AMC_McBSP_Data 4
LVL TXL (SN74AVC4T245)
McBSP_Data 4
McBSP_AMC_EN# (from FPGA)
AMC_JTAG 5
+12V DC (AMC)
MMC_GA[2:0]
IPMB_L(I2C) 2
ENABLE#
MMC (MSP430F5435)
SpyWire (640454-4)
MMC_Ctrl
MMC_SPI
DSP_UART
AMC_TCLK 8

16MB NOR Flash (N25Q032A11ESE40F) 4
DSP_SPI 4
16

JTAG TSW-108-07-S-S

FPGA (XC3S200AN-4FT70G256C)
JTAG
DSP SPI
DSP GPIO
DSP Rst & Int Ctrl
Mux_Ctrl
Clk_SPI
Clk_Ctrl
GPIO
GPIO
GPIO 10 McBSP CLK/FS
SYSPG_LED
Debug LED x 4
Reset x3
DIP SW x 3 (Boot Config, PCIESSEN, User Switch)
GPIO MMC_Ctrl
GPIO 4 MMC_SPI
GPIO PGood
GPIO Pwr Seq Ctrl

Multiplexer (IDT557-08) 2 16
2 PCIE_REF_CLK (from AMC)
PCIECLK
Clk Gen (CDCE62005) 8

Smart Reflex (UCD9222)

Pwr_Ctrl
+12V DC (AMC)
+12V DC (JACK)
Protection Ckt
ON BOARD Power Regulators
0.75V
0.9-1.1V CVDD
1.0V CVDD1
1.2V
1.5V
1.8V
2.5V
3.3V
5.0V

On Board CLOCK SOURCE
250.0MHz (HyperLink CLKP/N)
250.0MHz (SRIO CLKP/N)
100.0MHz (PCIe CLKP/N)
100.0MHz (Core CLKP/N)
66.67MHz (DDR3 CLKP/N)
48.0MHz (FPGA)
25.0MHz (Ethernet)
12.0MHz (FT2232HL)
32.768kHz (MSP430)

Project	TMDSEVM6657	Designed for TI by eInfochips	
Title	BLOCK DIAGRAM	Texas Instruments eInfochips The Solutions People	
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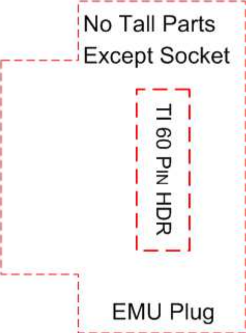
PLACEMENT

~22.58mm (0.89")
~15.15mm (0.6")
64.62mm (2.54")
73.5mm (2.893")
5.5mm (0.217")
7.52mm (0.3")
153.32mm (6.04")
180.6mm (7.11")

80- Pin Header
FPGA JTAG
LVL TXL
Ethernet Jack
PMBUS
Ethernet
FPGA
NAND
TI-60 Header
LVL TXL
Q4
Full Rst
Q2
EEPROM
Q3
Warm Rst
TPS54231
TPS54620
Q5
FT2232
NOR Flash
Cold Rst
MAX 3221
XDS560 Power
LVL TXL
USB Mini-B
UART 3Pin
COM Sel
HyperLink Conn
PCIe SRIO SGMII
JTAG
EMIF
C6657
Hyperlink
DDR3
DDR3 (ECC)
DDR3
DDR3
Clk Gen
MSP430
Mux
UCD7242
UCD9222
TPS54620
TPS54200
DC JACK

Connectors
Power Supply
Memory
UART/JTAG
Clock



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POWER CONSUMPTION

Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)											Total Power (mW)
			0.75V	1.00V	1.00V	1.20V	1.50V	1.80V	1.80V	2.50V	3.30V	3.30V	5.00V	
				CVDD	CVDD1			AUX	VCC		AUX	AMC		
TMS320C6657	CPU	1		2500.00	1000.00		350.00		50.00					4115.00
XC3S200AN-4FTG256C	FPGA	1				125.00		200.00			24.00			589.20
MT41J128M16HA-125	DDR3 SDRAM	2	50.00				525.00							1650.00
MT41J128M16HA-125	DDR3 ECC	0	50.00				525.00							0.00
NAND512R3A2SZA6E	NAND Flash (64MB)	1							15.00					27.00
AT25128B	SPI EEPROM	1									10.00			33.00
FT2232H	USB to JTAG convertor	1							70.00		210.00			819.00
88E1112	Ethernet	1				320.00				338.00				1229.00
MSP430	MMC	1										48.00		158.40
CDCE62005	Clock Generator	1									500.00			1650.00
XDS560v2	XDS560v2 Mezzanine	1									300.00		600.00	3990.00
	Misc	1						100.00			300.00			1170.00
Total Current on individual power supply (mA)			**100.00**	**2500.00**	**1000.00**	**445.00**	**1400.00**	**300.00**	**135.00**	**338.00**	**1344.00**	**48.00**	**600.00**	
5% margin added over design (mA)			**105.00**	**2625.00**	**1050.00**	**467.25**	**1470.00**	**315.00**	**141.75**	**354.90**	**1411.20**	**50.40**	**630.00**	
Power Consumption in (mW)			**78.75**	**2625.00**	**1050.00**	**560.70**	**2205.00**	**567.00**	**255.15**	**887.25**	**4656.96**	**166.32**	**3150.00**	**16202.13**

Vin		
3.3V	**TPS73701 -- 3.3V_Aux to 2.5V regulation**	**372.65 mA**
3.3V	**TPS73701 -- 3.3V_Aux to 1.8V_Aux regulation**	**330.75 mA**
3.3V	**TPS73701 -- 3.3V_Aux to 1.8VCC regulation**	**148.84 mA**
3.3V	**TPS73701 -- 3.3V_Aux to 1.2V regulation**	**490.61 mA**
1.5V	**TPS51200 -- 1.5V to 0.75V regulation**	**110.25 mA**
12.0V	**UCD7242 -- 12V to 1V_CVDD regulation**	**243.06 mA**
12.0V	**UCD7242 -- 12V to CVDD1 regulation**	**97.22 mA**
12.0V	**TPS54620 -- 12V to 1.5V regulation**	**219.48 mA**
12.0V	**TPS54620 -- 12V to 3.3V_AUX regulation**	**946.70 mA**
12.0V	**TPS54231 -- 12V to 5V regulation**	**328.13 mA**
	Total Current @12V	1.83A
	Total Current @3.3V_AMC	0.05A
	Total Power Consumption	22.18W

Project: TMDSEVM6657

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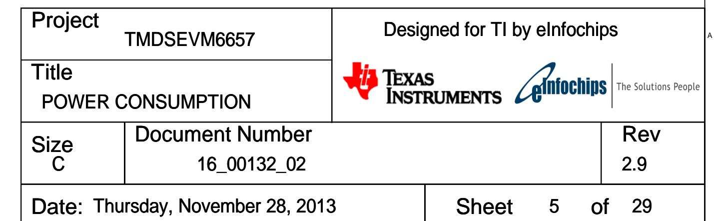

Title: POWER CONSUMPTION

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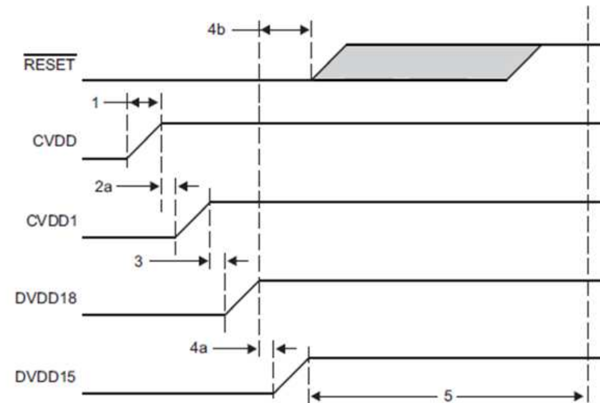
POWER SEQUENCE

VCC3V3_MP_AMC
MMC VCC3V3_MP
VCC12
FPGA, FT2232, Misc VCC3V3_AUX (VCC3V_AUX_PG)
FPGA VCC1V8_AUX
FPGA, Eth PHY VCC1V2
VCC_5V_EN
XDS560v2 Mezzanine Card VCC5 (VCC5_PG, T=10ms)
VCC2V5_EN (T=5ms)
Eth PHY VCC2V5 (VCC2V5_PG)
UCD9222_ENA1
DSP CVDD (UCD9222_PG1, T=5ms)
UCD9222_ENA2
DSP CVDD1/VCC1V0 (UCD9222_PG1, UCD9222_PG, T=5ms)
VCC1V8_EN1
DSP VCC1V8 (VCC1V8_PG, T=10ms)
VCC1V5_EN
DSP, DDR3 VCC1V5 (VCC1V5_PG, T=5ms)
VCC0V75_EN
FPGA_MUX_OE
DSP, DDR3 VCC0V75 (VCC0V75_PG)
REF_CLKP&N (T=5ms)
CLOCK2_PLL_LOCK
RESET# (T=5ms)
PORz (T=5ms)
RESETFULLz
RESETSTAT#



C6657 Design :

1) CVDD1 should ramp at the same time or shortly following CVDD. Although simultaneous ramping is permitted, CVDD1 must never exceed CVDD until after CVDD has reached a valid voltage.

2) DVD15 supply is ramped up following DVDD18. Although ramping DVDD18 and DVDD15 simultaneously is permitted, DVDD15 must never exceed DVDD18.

3) There is no specific power-up nor power-down sequence defined for FPGA.

4) FPGA is first to come up and it generates ENABLE signal for all power supplies using PGOOD signals.

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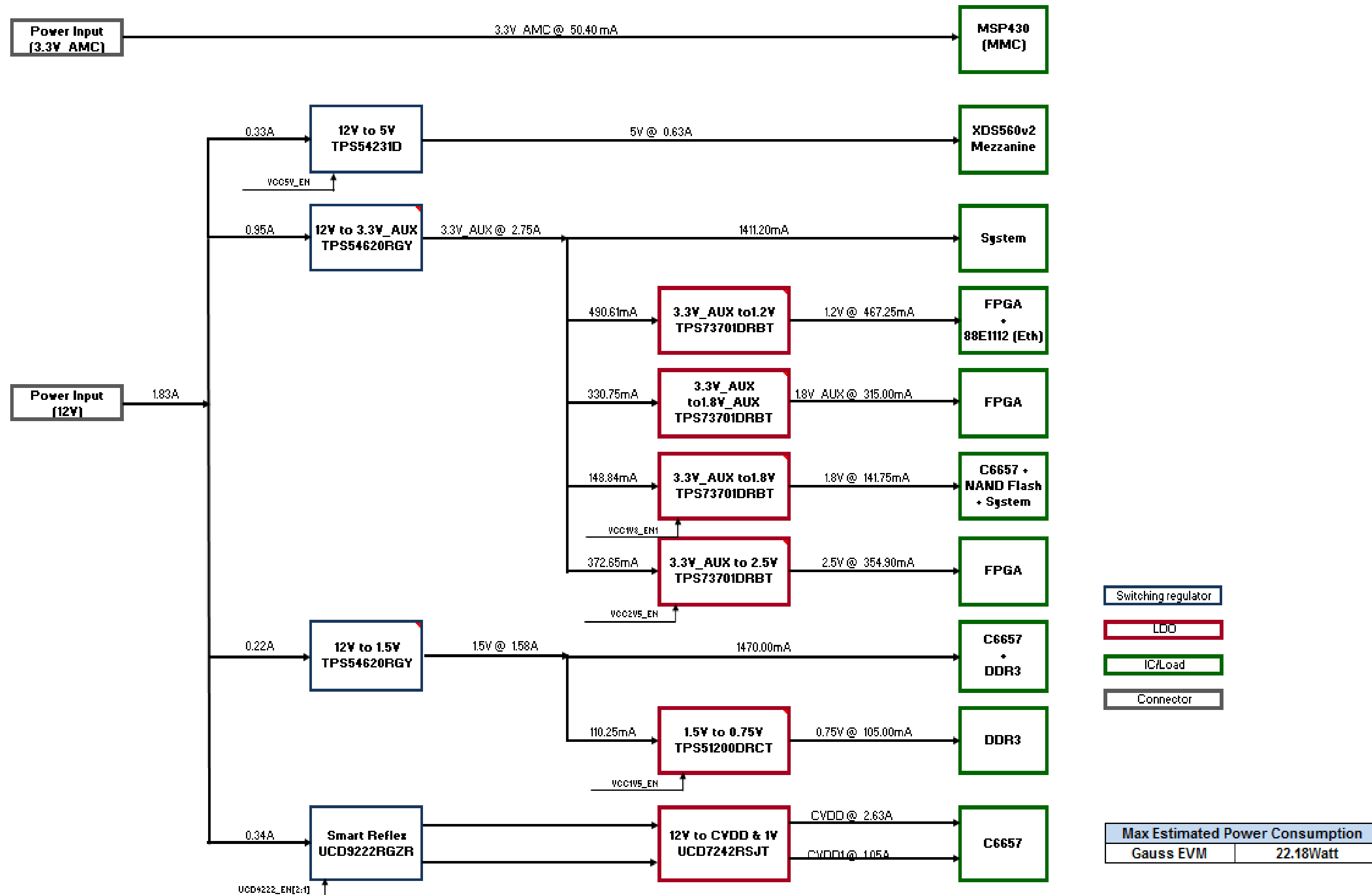
POWER DISTRIBUTION



Max Estimated Power Consumption	
Gauss EVM	22.18Watt

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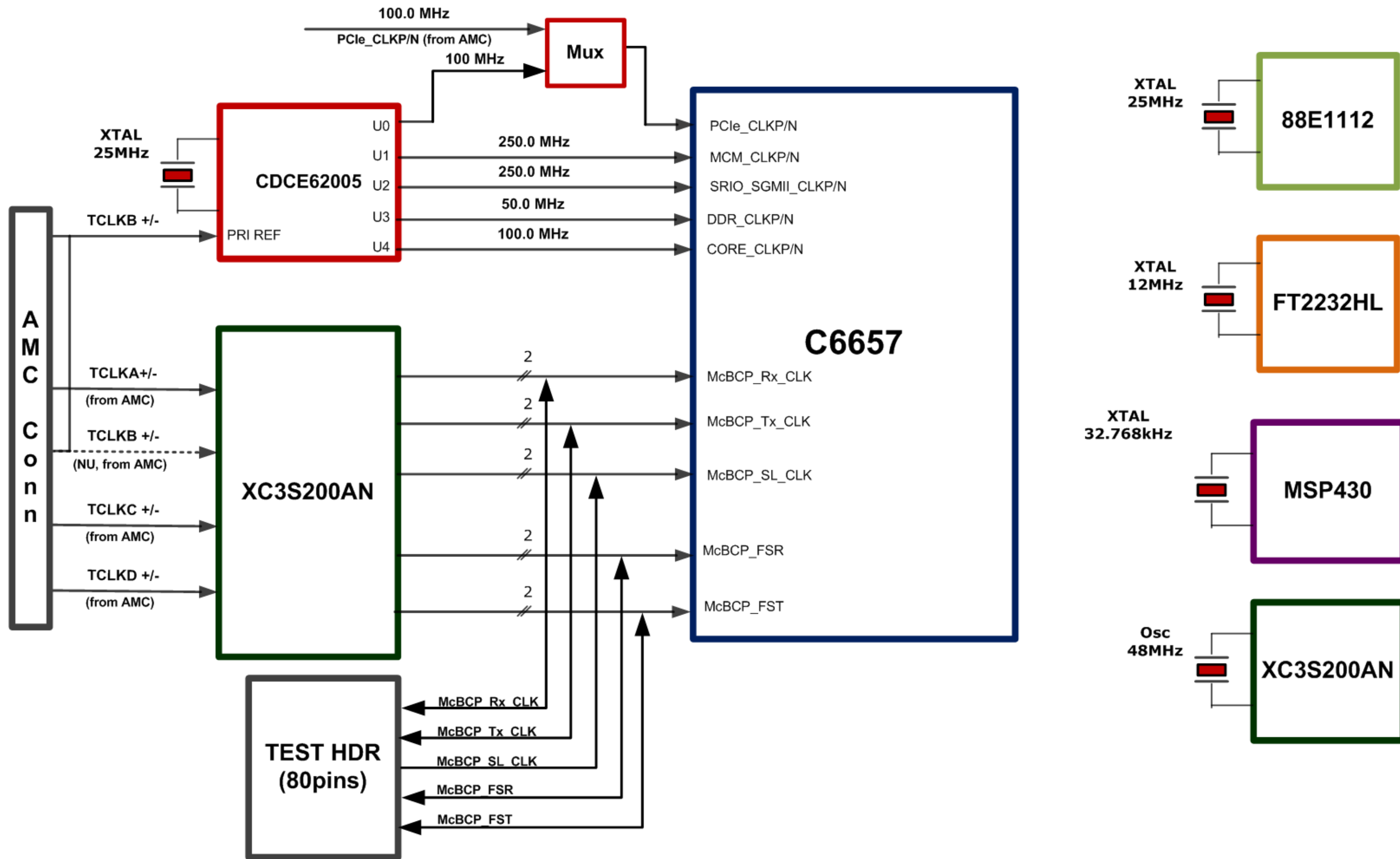
CLOCK DIAGRAM



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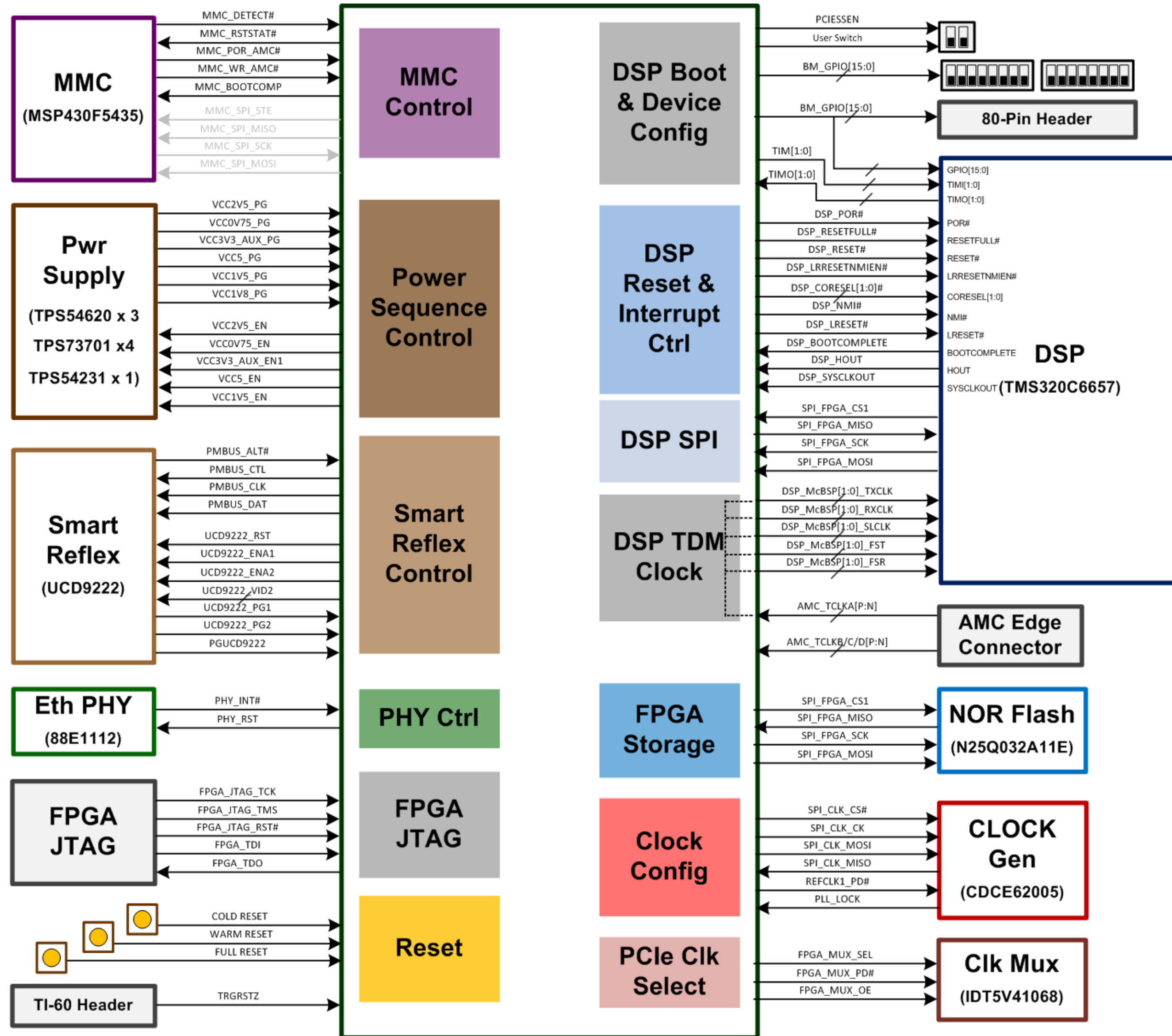
FPGA INTERFACE CONTROL DIAGRAM



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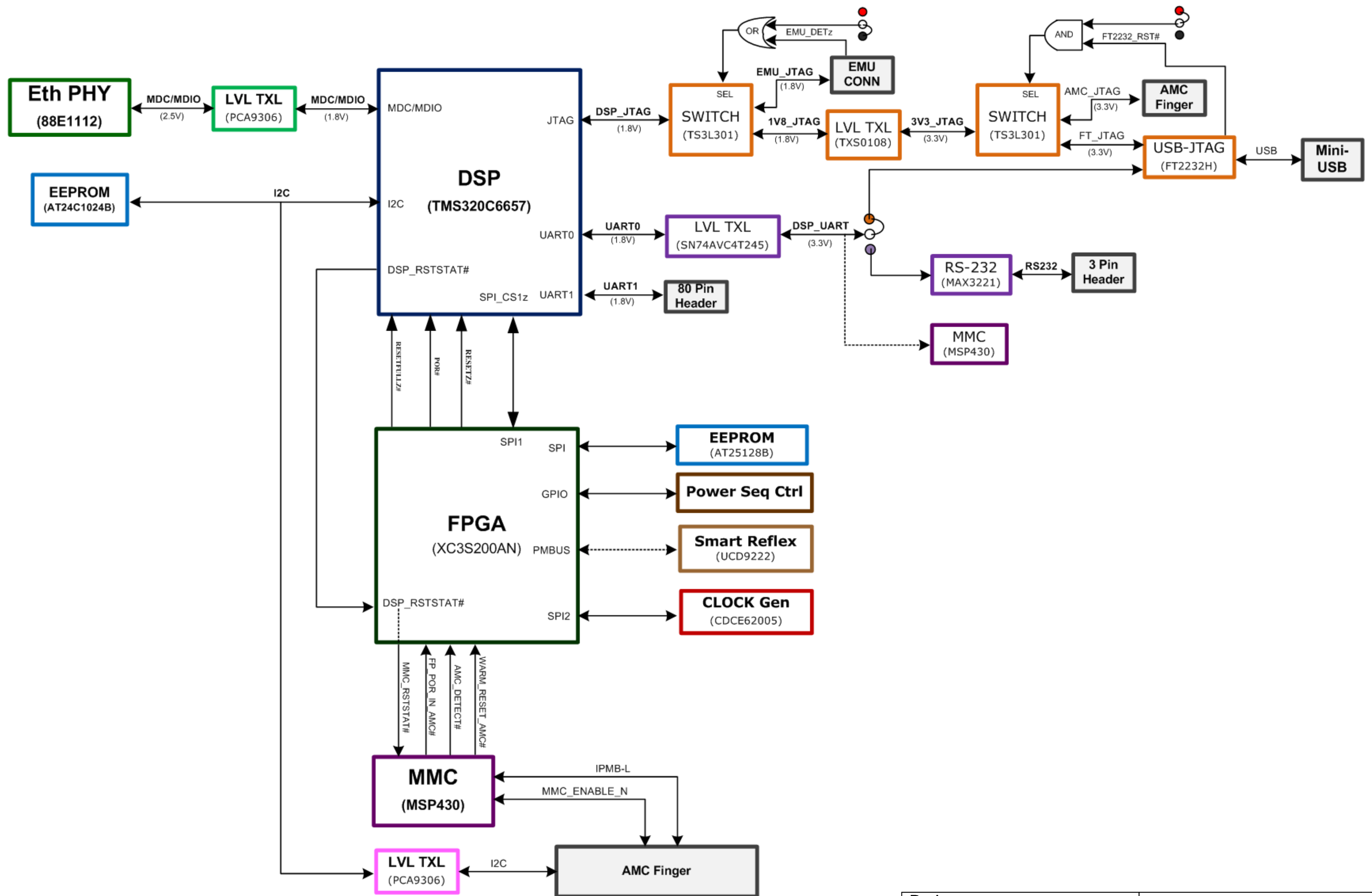
MANAGEMENT MAP



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AMC CONNECTOR

FAN CONNECTOR

VCC12
WB_3V_2.0mm
NU
FAN1
C526
NU
1uF

Front Panel and ESD Strip

R158 NU 0E
R157 NU 0E
R936 10M
R937 10M
TRIP1
TRIP2
TRIP3
ESD1
AMC-ESD-B

VCC3V3_MP_AMC
Management Power

VCC12_AMC
AMC1
GF-AMC-B

AMC_JTAG_TDI R445 10K
AMC_JTAG_TDO R446 10K
AMC_JTAG_TMS R447 10K
AMC_JTAG_TCK R449 10K
AMC_JTAG_RST# R448 10K
VCC3V3_AUX

U245
PCA9306DCURR
DSP_SCL
DSP_SDA
DSP_SCL_AMC
DSP_SDA_AMC

U13
SN74AVC4T245PWR
McBSP_AMC_EN#
AMC_P12_McBSP_TX0
AMC_P12_McBSP_TX1
AMC_P12_McBSP_RX0
AMC_P12_McBSP_RX1
DSP_McBSP0_TX
DSP_McBSP1_TX
DSP_McBSP0_RX
DSP_McBSP1_RX

OE# = 0
DIR = 0 --> B to A
DIR = 1 --> A to B

Project	TMDSEVM6657	Designed for TI by eInfochips
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MMC INTERFACE

MSP430 Power

SpyBiWire

The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7

SPI Interface for FPGA debugging.

IPASS+HD for HyperLink

DEBUG HEADER

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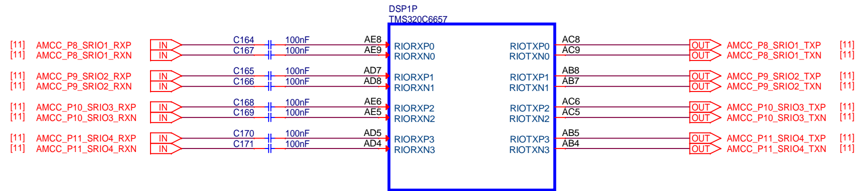
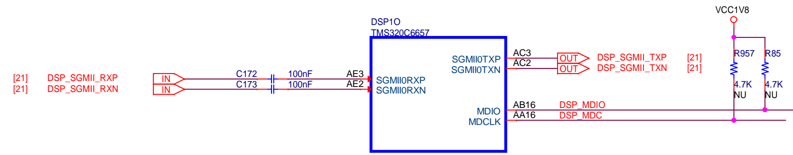
SRIO

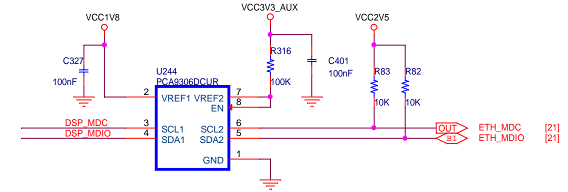


Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias

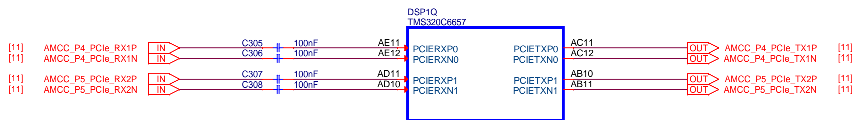
SGMII



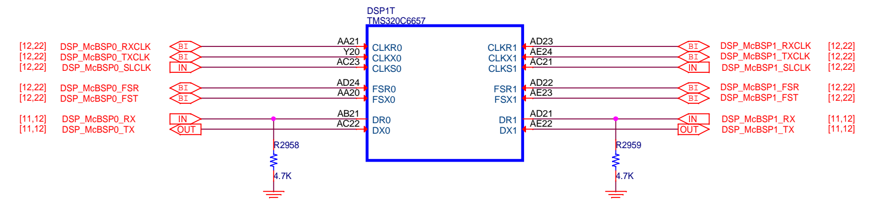
VOLTAGE LEVEL TRANSLATOR



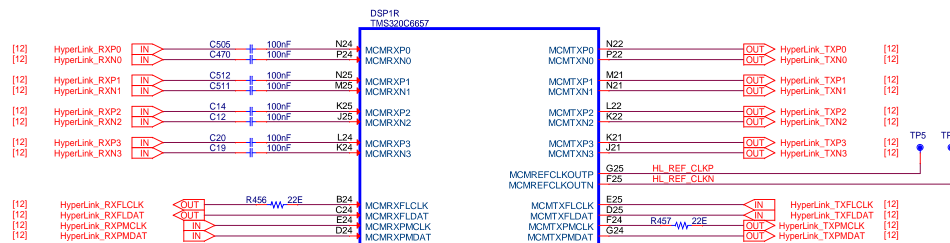
PCIE



McBSP



HYPERLINK



The HyperLink routes must have a max of 2 vias and no via stubs (Outer layer routing recommended)

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Title	DSP SERDES PORTS	Texas Instruments	eInfochips The Solutions People
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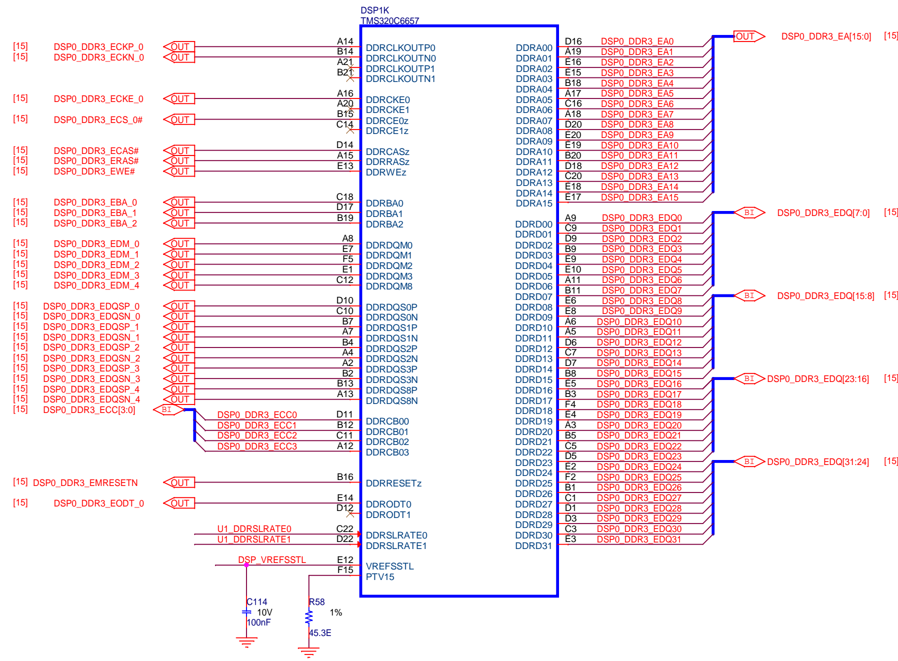
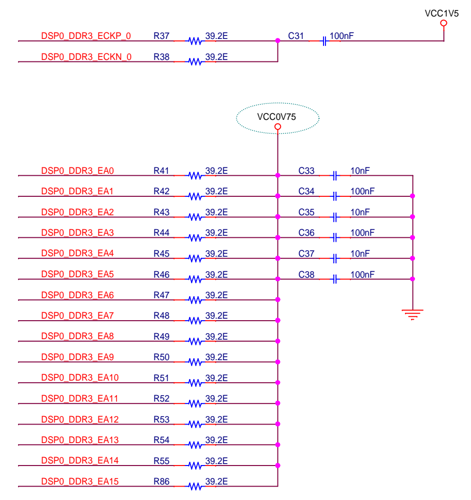
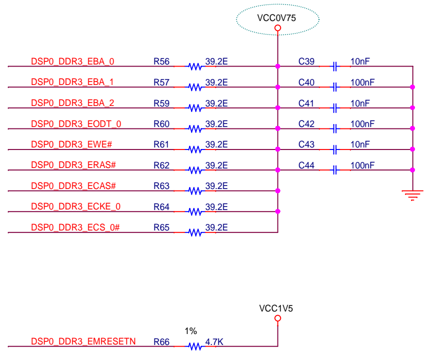
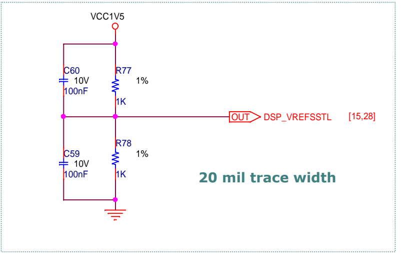
DDR3 INTERFACE



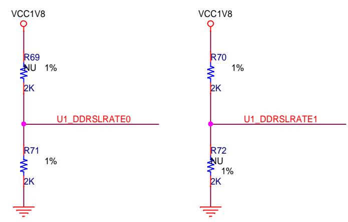


Place these resistors at the end of the trace.





20 mil trace width



DDR3 Slew-Rate Setting (DDRSLRATE[1:0]):

00 Fastest
01 Fast
10 Slow
11 Slowest

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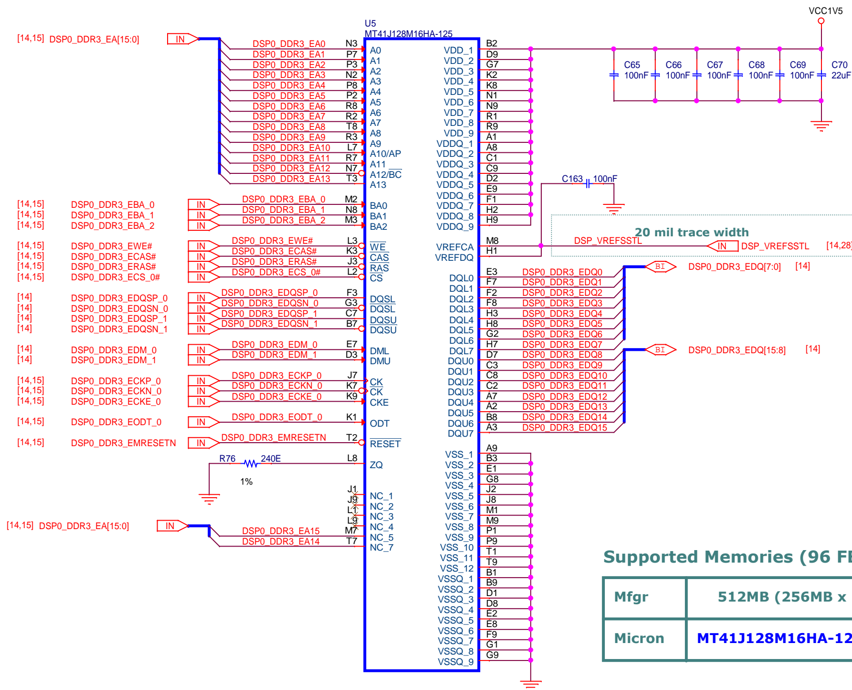
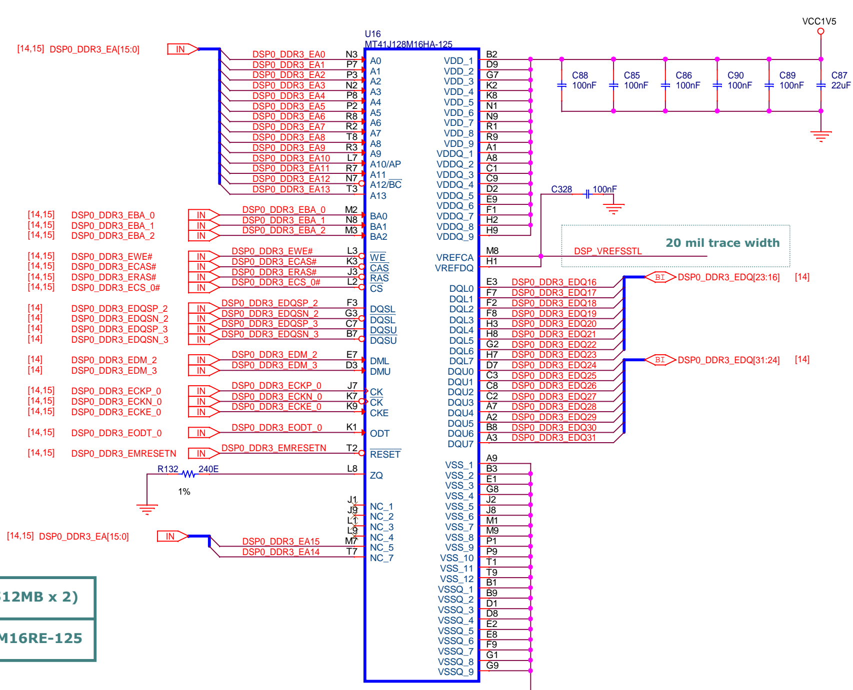
DDR3 MEMORY INTERFACE

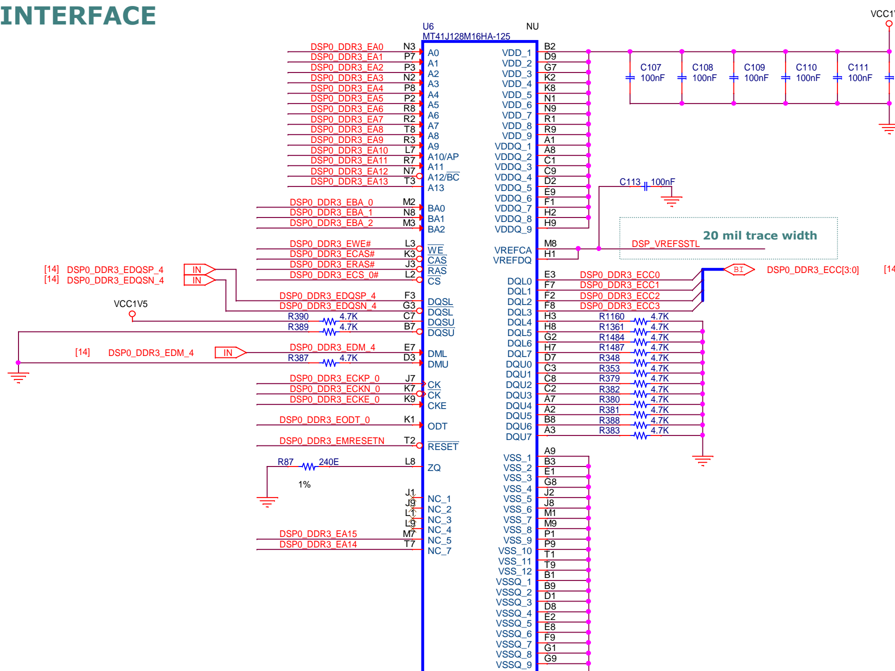




Supported Memories (96 FBGA) :

Mfgr	512MB (256MB x 2)	1024MB (512MB x 2)
Micron	MT41J128M16HA-125	MT41J256M16RE-125

DDR3 ECC INTERFACE



- Data bits can be swapped within the byte lane to ease routing.

- Address/Command/Control/Clock routing must be Fly-By in byte order ECC, 0, 1, 2, 3.

Supported ECC Chip (96 FBGA) :

Mfgr	256MB	512MB
Micron	MT41J128M16HA-125	MT41J256M16RE-125

Project	TMDSEVM6657	Designed for TI by eInfochips
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C6657 - EMIF

NAND FLASH

C6657 - JTAG & EMU

TI-60 Header

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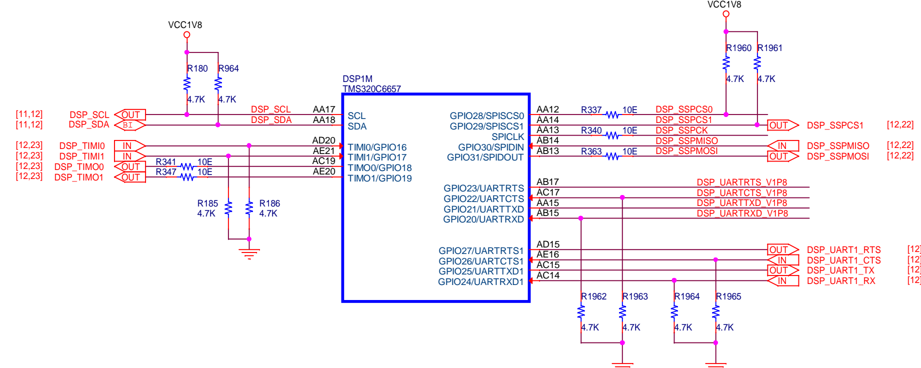
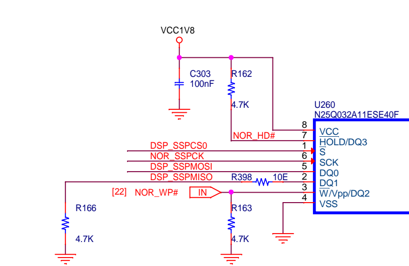
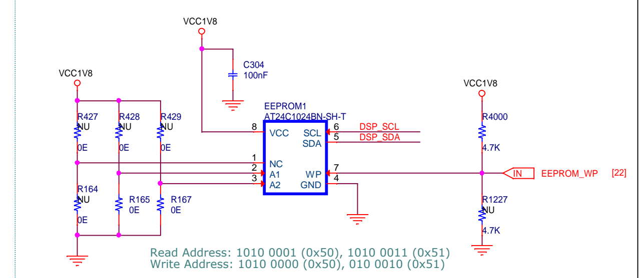
I2C, TIMER[1:0], SPI



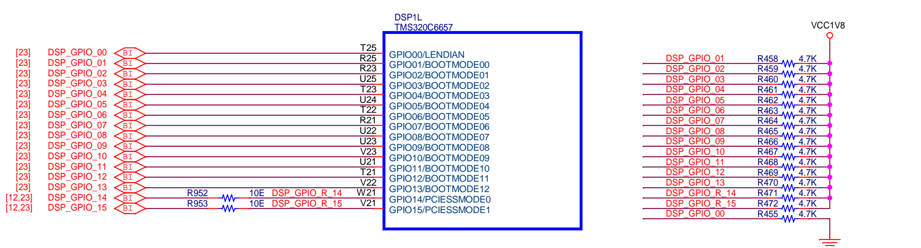
32Mb SPI NOR Flash



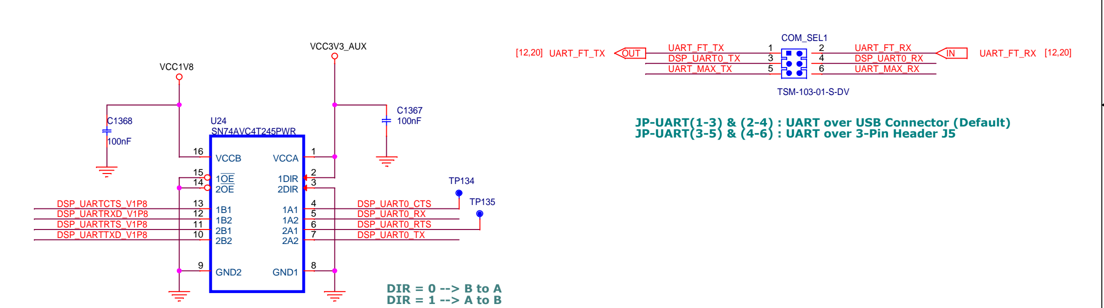
1Mb I2C EEPROM

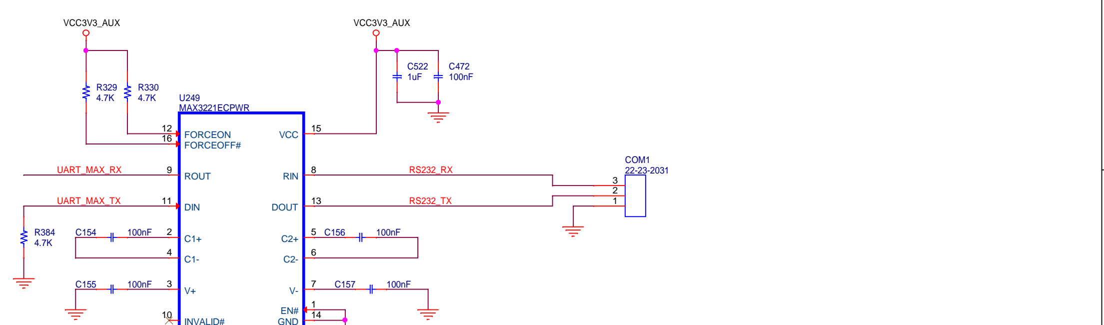


GPIO

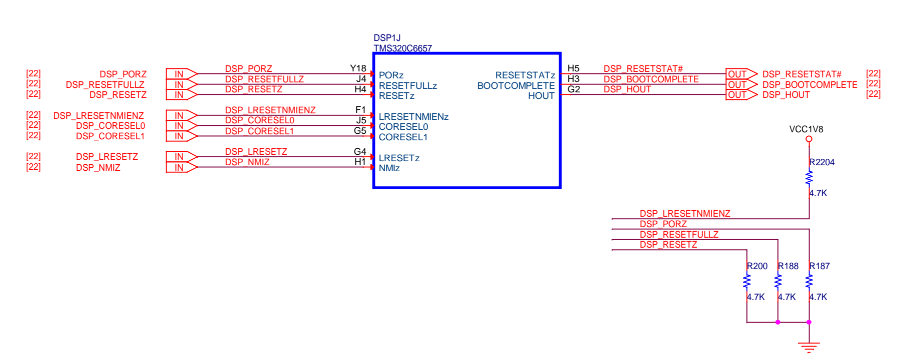


UART to RS232

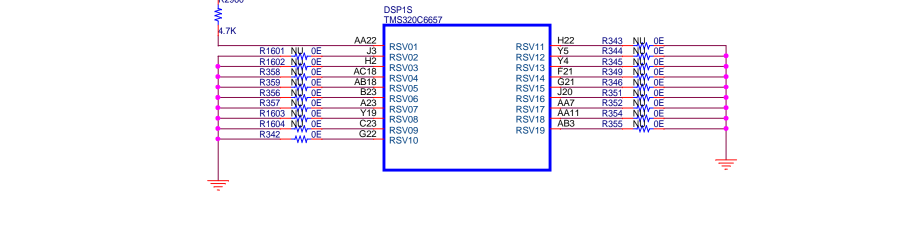




Reset Control



Reserved



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DSP CLOCK

100.00MHz
66.67MHz
250MHz
100.00MHz
250MHz

All blocking capacitors to be placed near DSP
to keep connecting routes short and minimize vias

PCI CLOCK MUX

(LVDS)
(HCSL)

SEL	I/p PAIR SEL
LOW	IN2/IN2#
HIGH	IN1/IN1#

SMART REFLEX

DIR = 0 --> B to A
DIR = 1 --> A to B

Reserved for future use
Not supported at this time

Project	TMDSEVM6657	Designed for TI by eInfochips
Title	DSP-CLOCK & SMART REFLEX	
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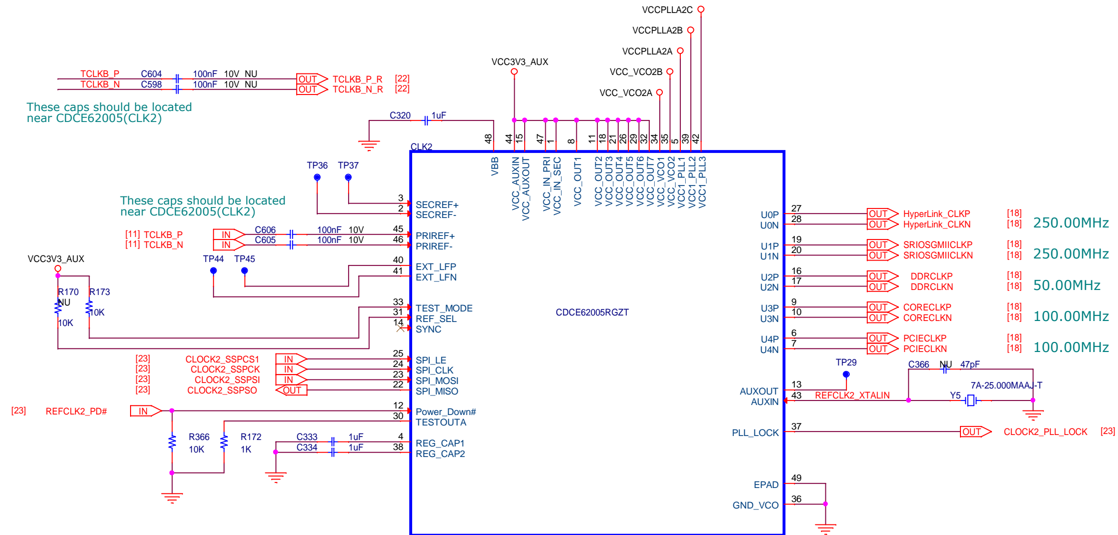
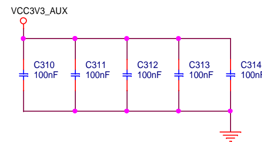
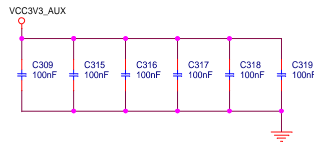
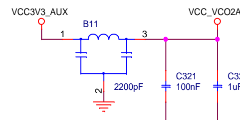
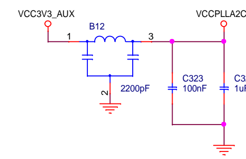
CLOCK GEN2

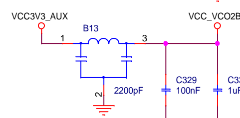


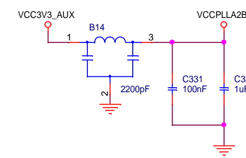


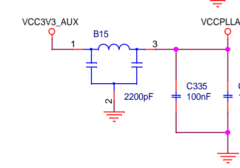












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Title	CLOCK GENRATION	Texas Instruments / eInfochips The Solutions People
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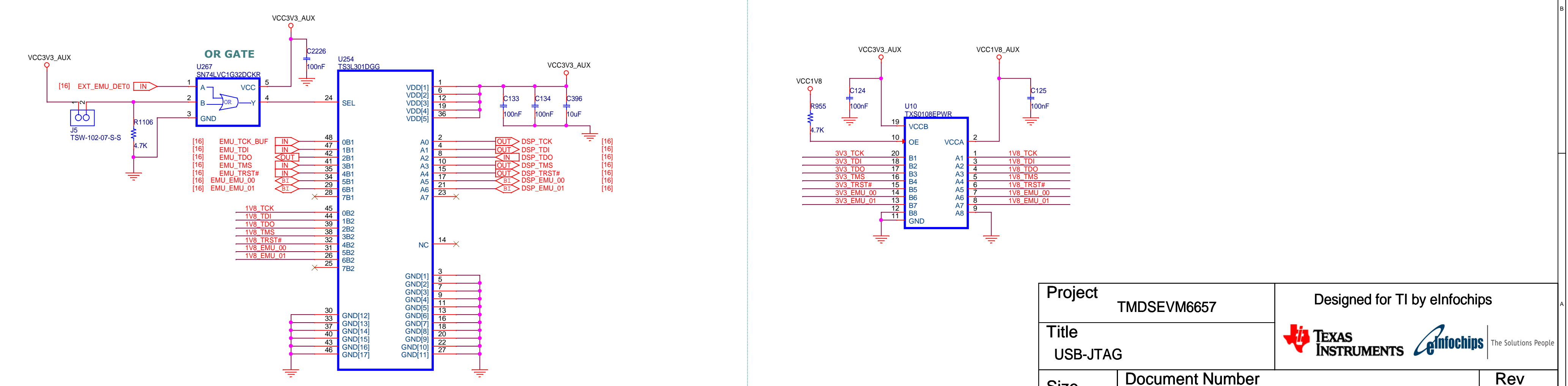
USB, JTAG

Switch for JTAG emulation
FT2232HL_RESET# = 0 --> AMC
FT2232HL_RESET# = 1 --> Mini USB



Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation

Project	TMDSEVM6657	Designed for TI by eInfochips
Title	USB-JTAG	Texas Instruments / eInfochips The Solutions People
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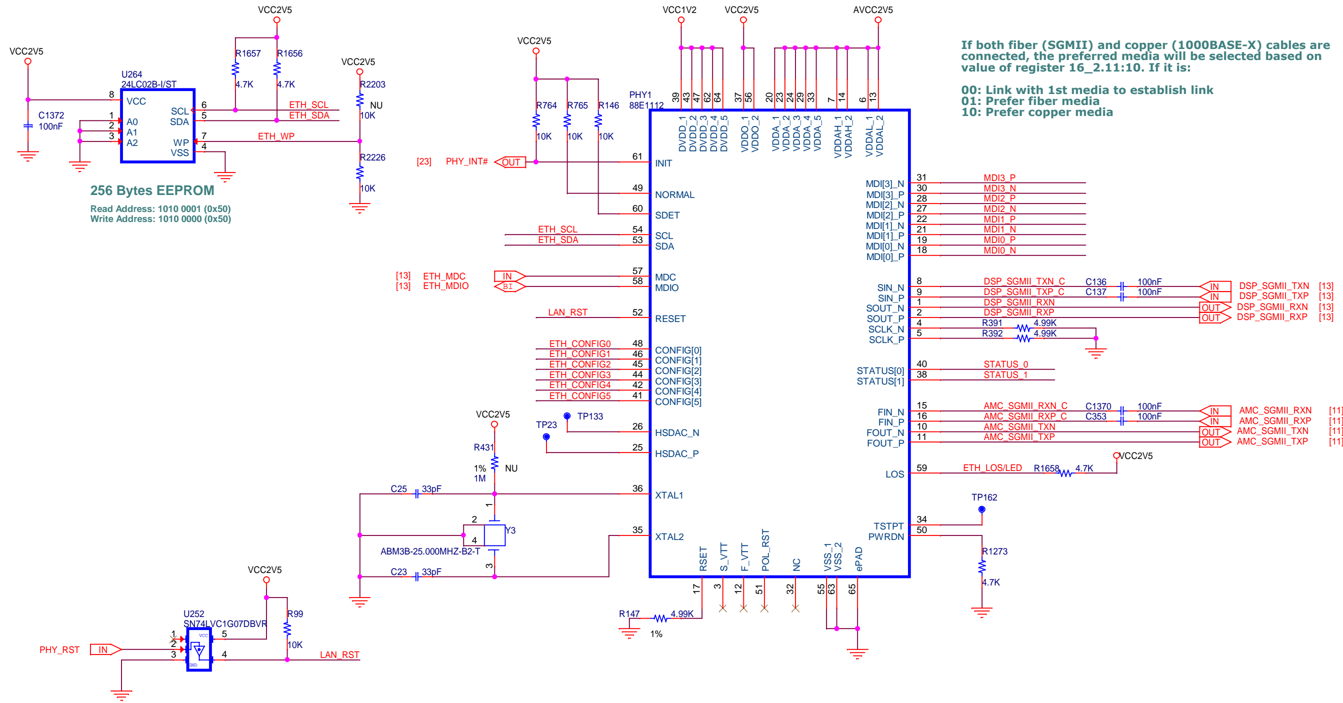
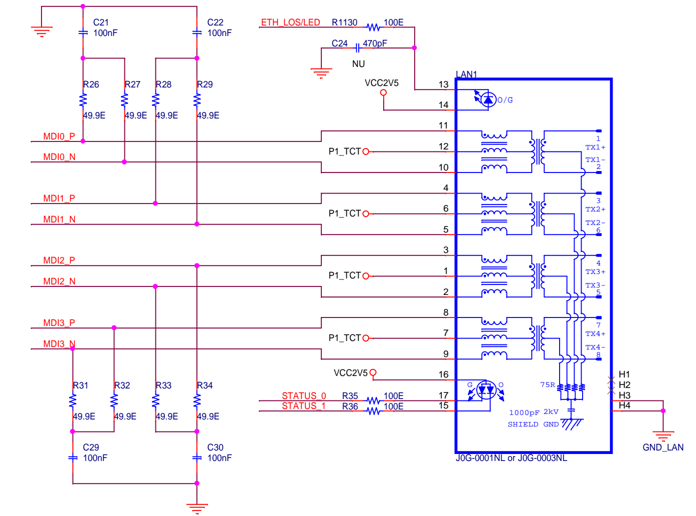
ETHERNET PHY

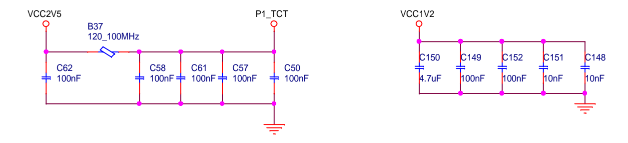


ETHERNET JACK

LED (Colour)	Link	No Link
LOS (Orange/Green)	ON	OFF



LED (Colour)	1Gbps		100Mbps		10Mbps	
	Activity	No Activity	Activity	No Activity	Activity	No Activity
Status 0 (Green)	BLINK	SOLID ON	BLINK	SOLID ON	OFF	OFF
Status 1 (Orange)	OFF	OFF	BLINK	SOLID ON	BLINK	SOLID ON



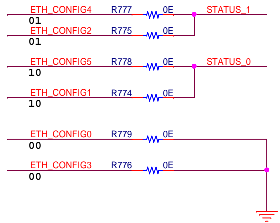
Pin to Configuration Bit Mapping

PIN	BIT[1]	BIT[0]
CONFIG0	PHYADR[1]	PHYADR[0]
CONFIG1	PHYADR[3]	PHYADR[2]
CONFIG2	SGMII_CLK	PHYADR[4]
CONFIG3	SEL_TWSI	SEL_VTT
CONFIG4	EEPROM[1]	EEPROM[0]
CONFIG5	MODE[1]	MODE[0]

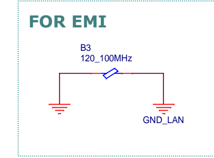
PIN	VALUE
VDD0	11
STATUS[0]	10
STATUS[1]	01
VSS	00

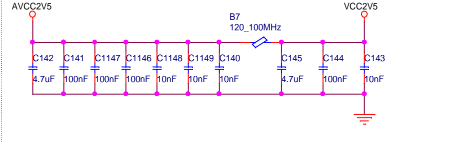
POL_RST	RESET=0	RESET=1
0	Reset	Normal
1 or Floating	Normal	Reset

PIN	VALUE	CONNECTION	INTERPRETATION
CONFIG0	00	VSS	PHY Address[1:0] is 00
CONFIG1	10	STATUS[0]	PHY Address[3:2] is 10
CONFIG2	01	STATUS[1]	SGMII_CLK not supplied; PHY Address[4] is 1
CONFIG3	00	VSS	MDC/MDIO mode; S_VTT & F_VTT int supplied
CONFIG4	01	STATUS[1]	Start reading from address 0
CONFIG5	10	STATUS[0]	SGMII MAC Int to Auto Media select (Cu/SGMII)



FOR EMI





Project	TMDSEVM6657	Designed for TI by eInfochips
Title	GIGABIT ETHERNET	Texas Instruments / eInfochips The Solutions People
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FPGA - POWER & RST CTRL, McBSP

FPGA - POWER, JTAG

Reserved for future use

MMC

VCL/VDA Enable

Power Sequence

UCD9222

Reset Switch

AMC TCLK

Place near FPGA

TCLKA_P	R228	100E	TCLKA_N
TCLKB_P_R	R317	100E	TCLKB_N_R
TCLKC_P	R318	100E	TCLKC_N
TCLKD_P	R319	100E	TCLKD_N

Bank1

Bank0

DSP

EEPROM
NOR Flash

C6657 SPI

DSP McBSP SCLK

60 Pin Header C6657

DSP McBSP CLK & FS

PUDC (User I/O Pull-Up Control)
If its value during configuration is:

0: enable PUs in all I/O pins to resp VCCO
1: No pull-ups

Must be High During Configuration to allow configuration to start

Cold_RESET

WARM_RESET

FULL_RESET

High active

Project	TMDSEVM6657
Title	FPGA-POWER,RESET,McBSP
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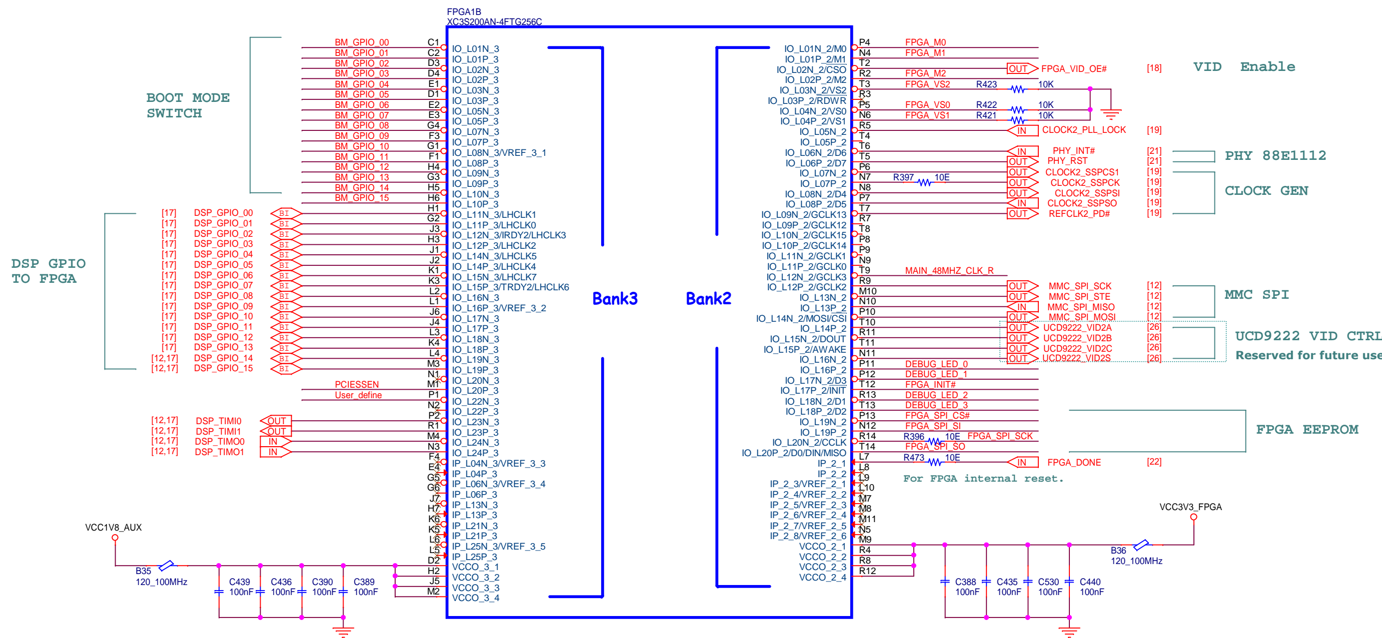
Designed for TI by eInfochips

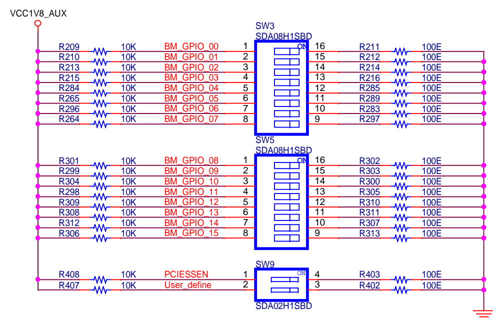
Texas Instruments

eInfochips The Solutions People

FPGA, BOOT MODE & SMART REFLEX



BOOT STRAP CONFIGURATION



Boot Configuration

DIP Switch	DSP	BM_GPIO	Primary Function
BM_GPIO0	GPIO0	ENDIANESS	0 - Big Endian 1 - Little Endian
BM_GPIO[4:1]	GPIO[4:1]	BOOTMODE[3:0]	Boot Device
BM_GPIO[10:5]	GPIO[10:5]	BOOTMODE[9:4]	Boot Device Config
BM_GPIO[13:11]	GPIO[13:11]	BOOTMODE[12:10]	PLL Multiplier/I2C
BM_GPIO[15:14]	GPIO[15:14]	PCIESSMODE[1:0]	Endpt/RootComplex

Boot Device

BM_GPIO [4:1]	Boot Device	BM_GPIO [4:1]	Boot Device
0 0 0 0	Sleep/EMIF16	X 1 0 1	I2C Master
0 0 0 1	SRIO	0 1 0 1	I2C Slave
X 0 1 0	Ethernet	X 1 1 0	SPI
0 0 1 1	NAND	0 1 1 1	Hyperlink
0 1 0 0	PCIe	1 0 0 0	UART

Note: GPIO[10:5] bit definitions depend on the boot mode.

Boot PLL Settings

BM_GPIO [13:11]	Input Clock (in MHz)	BM_GPIO [13:11]	Input Clock (in MHz)
0 0 0	50.00	1 0 0	156.25
0 0 1	66.67	1 0 1	250.00
0 1 0	80.00	1 1 0	312.50
0 1 1	100.00	1 1 1	122.88

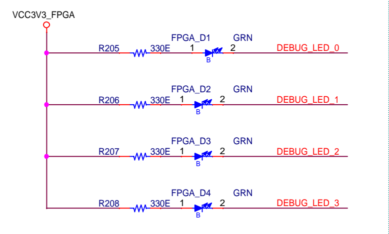
PCIe Mode Selection PCIESSMODE[1:0]

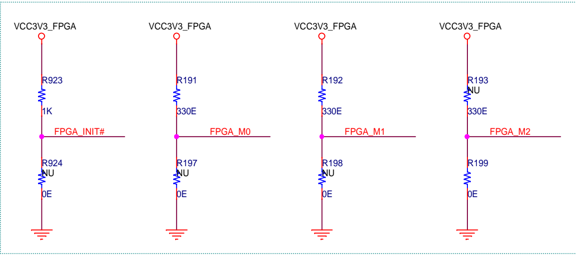
BM_GPIO [15:14]	PCIe Mode
0 0	End-point mode
0 1	Legacy End-point mode (support for legacy INTx)
1 0	Root complex mode
1 1	Reserved

PCIESSEN

BM_GPIO16	PCIe Status
0	PCIe module disabled
1	PCIe module enabled

DEBUG_LED





Project	TMDSEVM6657	Designed for TI by eInfochips	
Title	FPGA & BM & SMART REFLEX		
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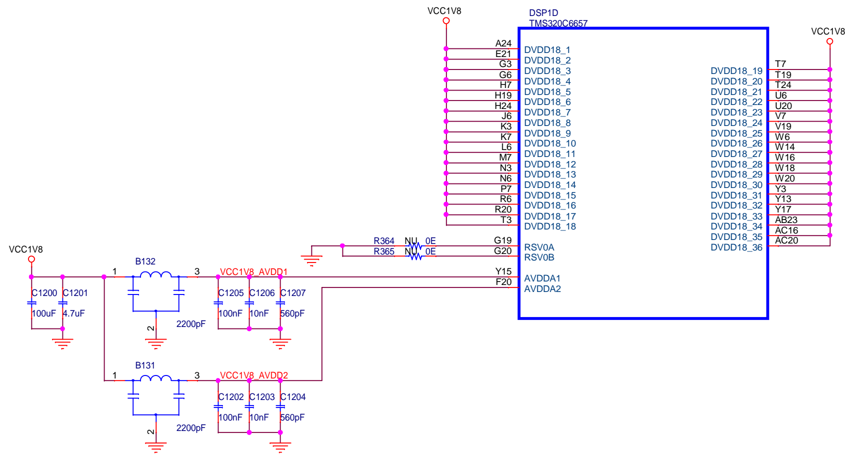
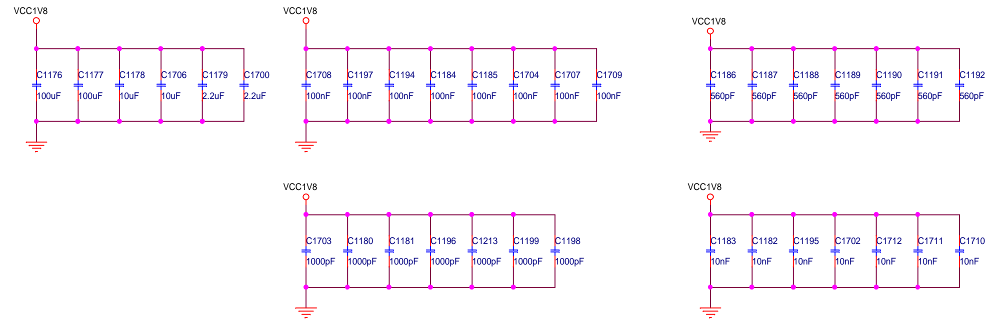
1.8V

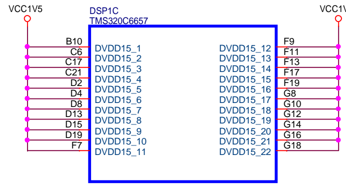
Place near to DSP

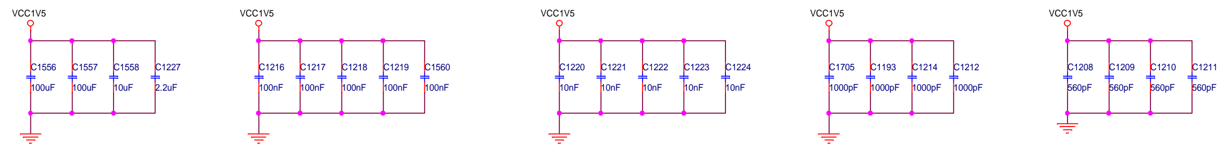




1.5V

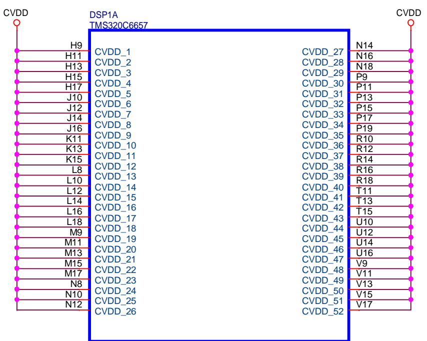
Place near to DSP





0.9V - 1.1V (SMART REFLEX)

Place near to DSP



CVDD
C1570 10uF
C1571 10uF
C1266 2.2uF
C1568 2.2uF

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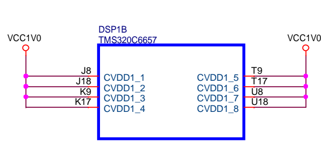
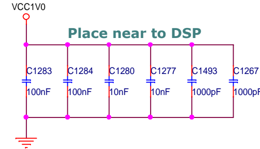
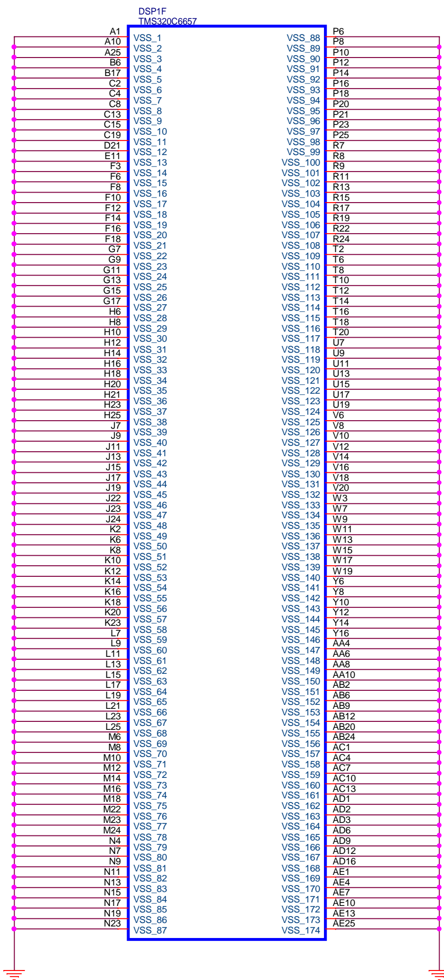
1.0V

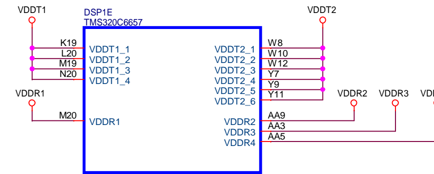


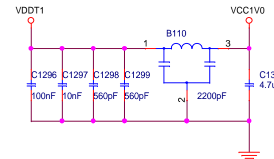


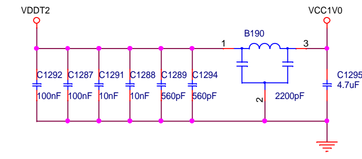
GROUND

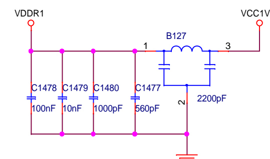


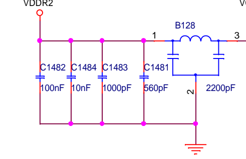
1.0V & 1.5V for SERDES

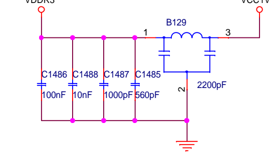


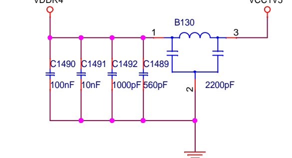












Project	TMDSEVM6657	Designed for TI by eInfochips	
Title	DSP POWER 2		
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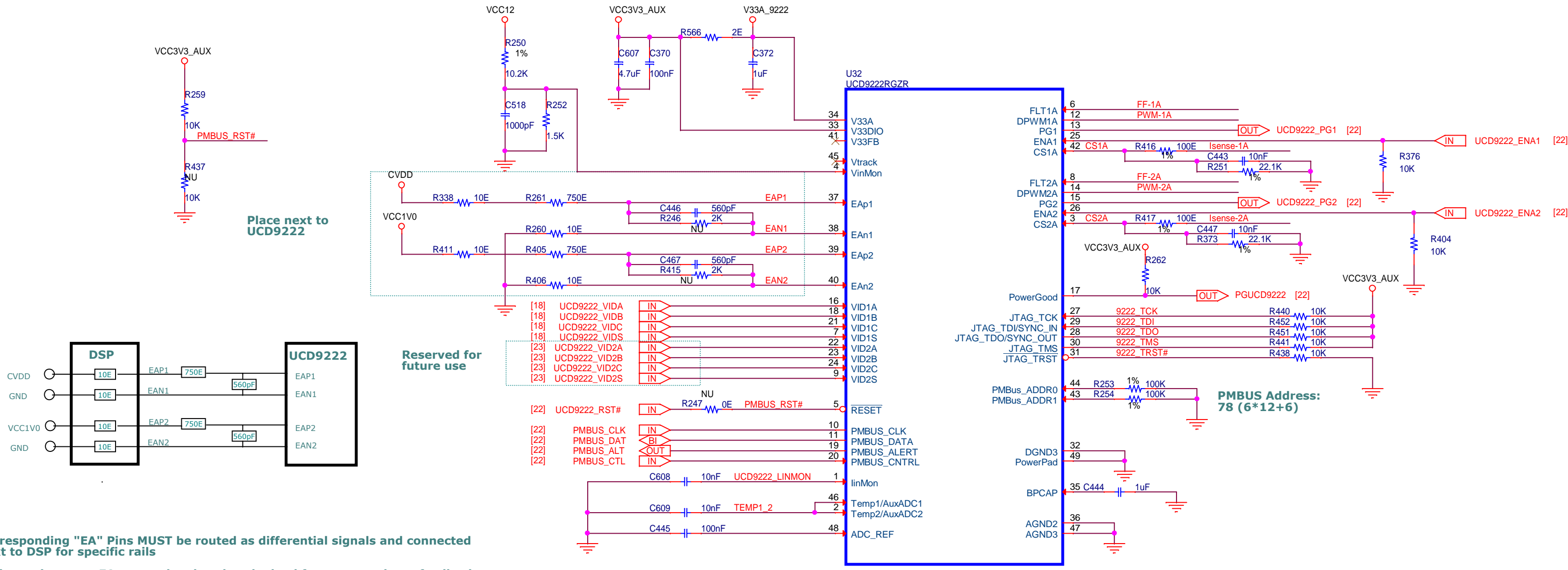
SMART REFLEX



Place next to UCD9222

Reserved for future use

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Provide min 25 thermal vias for IC

- C444 and C372 should be mounted adjacent to UCD9222 and connected without a via
- Components related to Isense pins should be located adjacent to UCD9222 with tightly coupled gnds.

PMBUS Address: 78 (6*12+6)

Resistor Calculation for Isense

Rmon = Vmon/ (Imax x 20 uA/A)
Vmon = 12*1.5/(1.5+10.2) = 1.53V

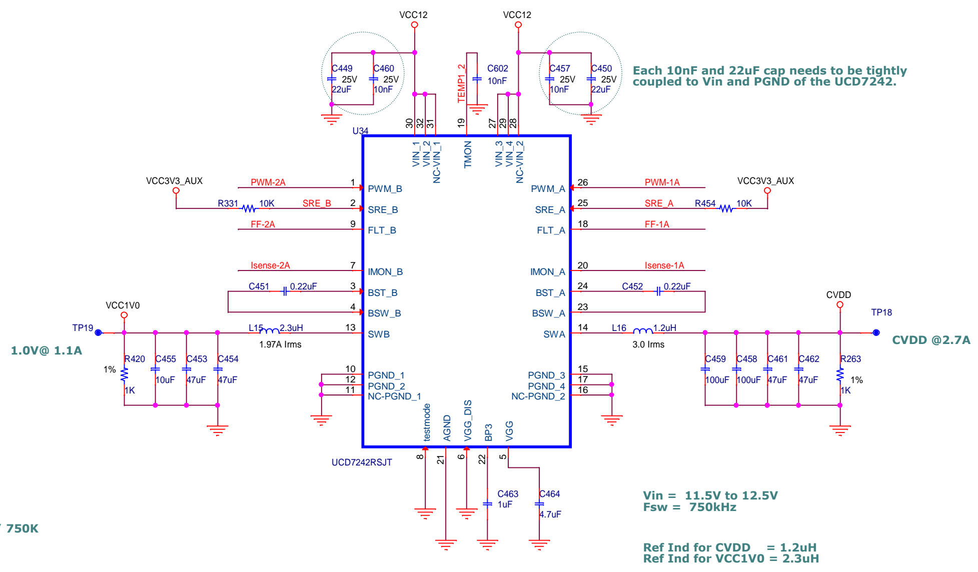
Rmon1 = 1.53*1000/(2.7*20) K
= 28.49K

Rmon2 = 1.53*1000/(1.1*20) K
= 69.93K

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

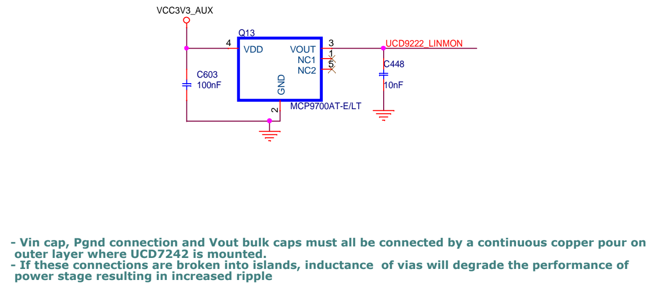
CVDD/CVDD1



Each 10nF and 22uF cap needs to be tightly coupled to Vin and PGND of the UCD7242.

1.0V@ 1.1A

CVDD @2.7A



- Vin cap, Pgnd connection and Vout bulk caps must all be connected by a continuous copper pour on outer layer where UCD7242 is mounted.
- If these connections are broken into islands, inductance of vias will degrade the performance of power stage resulting in increased ripple

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I}\,\frac{D}{fs}$$

Inductor Calculation for CVDD

L= (12.5 - 1) / (2.7) * (1/12.5) / 750K
= 0.46 uH

Inductor Calculation for CVDD1

L= (12.5 - 1) / (1.1) * (1/12.5) / 750K
= 1.11 uH

Vin = 11.5V to 12.5V
Fsw = 750kHz

Ref Ind for CVDD = 1.2uH
Ref Ind for VCC1V0 = 2.3uH

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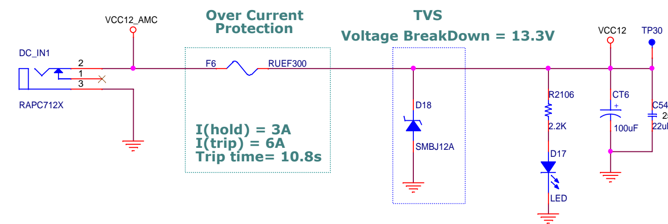
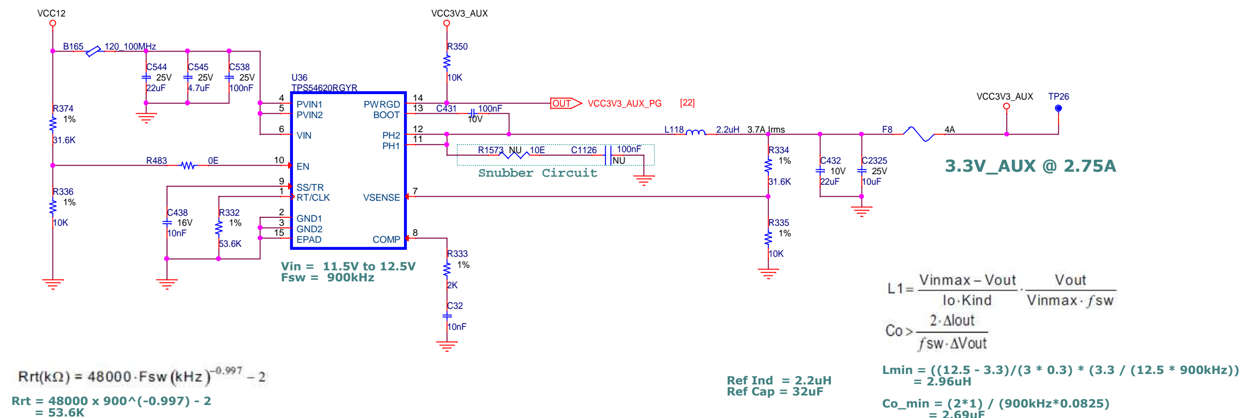
VCC12



12V to 3.3_AUX Generation

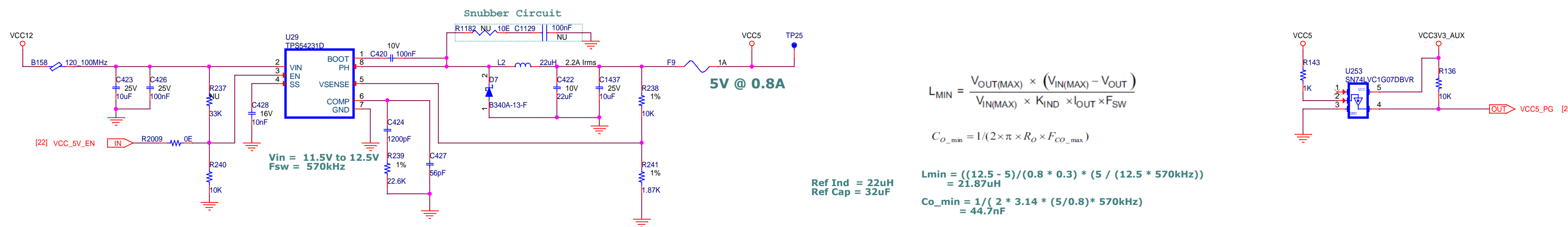


$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot fsw}$$

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout}$$

$$Rrt(k\Omega) = 48000 \cdot Fsw(kHz)^{-0.997} - 2$$

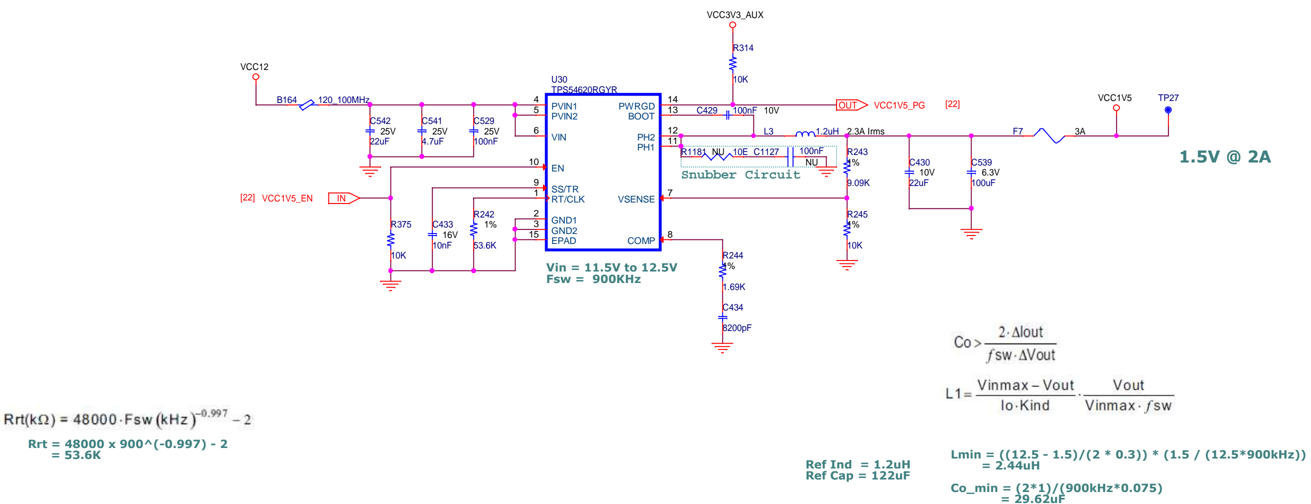
12V to 5V Generation



$$L_{MIN} = \frac{V_{OUT(MAX)} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}}$$

$$C_{O_min} = 1/(2 \times \pi \times R_O \times F_{CO_max})$$

12V to 1.5V Generation

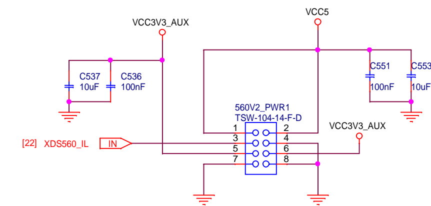


$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout}$$

$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot fsw}$$

$$Rrt(k\Omega) = 48000 \cdot Fsw(kHz)^{-0.997} - 2$$

XDS560 v2 Mezzanine Power



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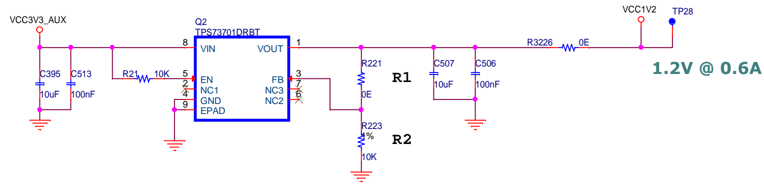
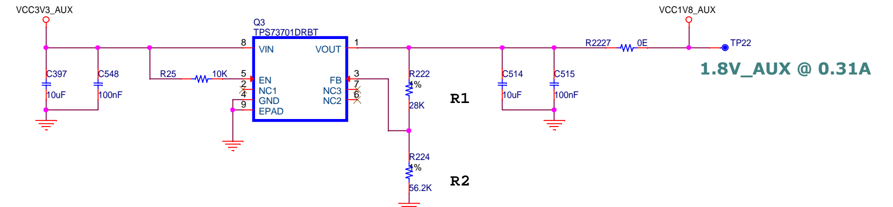
3.3V_AUX to 1.2V Generation



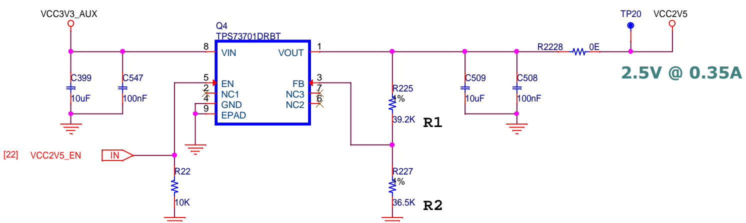
Vout = (R1+R2)/R2*1.204
= (0+10k)/10k*1.204
= 1.204V

3.3V_AUX to 1.8V_AUX Generation



Vout = (R1+R2)/R2*1.204
= (28k+56.2k)/56.2k*1.204
= 1.804V

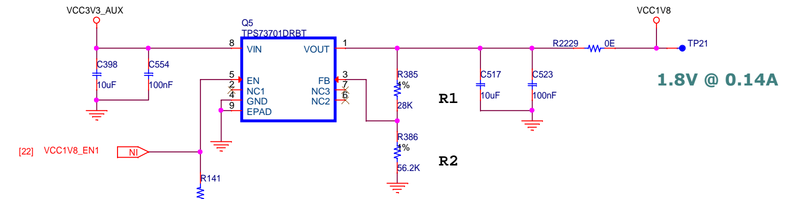
3.3V_AUX to 2.5V Generation



Vout = (R1+R2)/R2*1.204
= (39.2k+36.5k)/36.5k*1.204
= 2.50V

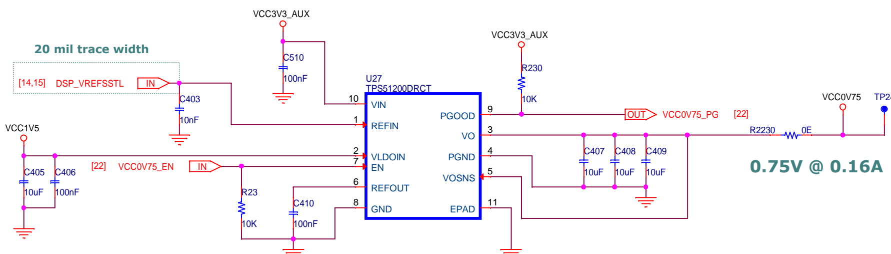
VCC3V3_AUX
VCC2V5
R142 1K
U251
SN74LVC1G07DBVR
R75
10K
OUT VCC2V5_PG [22]

3.3V_AUX to 1.8V Generation

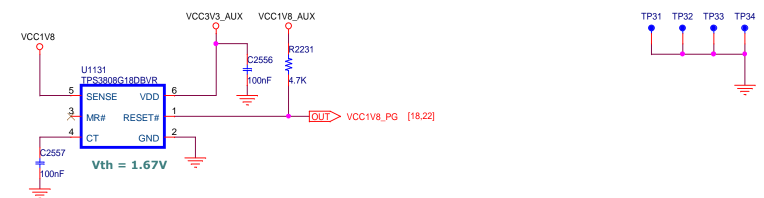


Vout = (R1+R2)/R2*1.204
= (28k+56.2k)/56.2k*1.204
= 1.804V

3.3V_AUX to 0.75V Generation



1.8V Superviser Circuit



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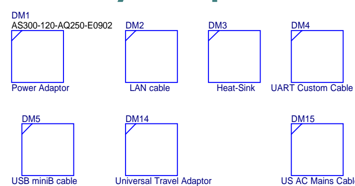
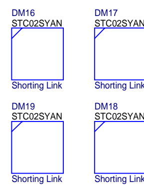
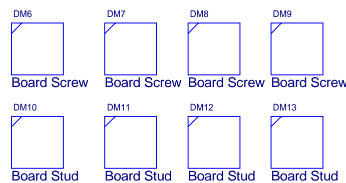
TMDSEVM6657 - REVISION HISTORY

PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	0.6	- CLK3 removed - Series Termination removed from GPIO0 to GPIO13 lines	3-FEB-2012	eInfochips
	1.1	- D9 and D10 part changed with one with higher current capacity. - R134 changed to 1K from 4.7K - NU resistors R433 and R434 changed to 10K and 1.2K resp. They are to be mounted. - R12 and R17 replaced by 100nF caps C1225 and C1226 - R70 and R71 mounting status changed from NU to populated. - U6 (DDR3 ECC chip) made NU. - DDR3 Clock frequency from Clock Gen changed to 50 MHz (software change only).	20-MAR-2012	eInfochips
2.0	0.1	- Clock buffer U1132 removed. 2 OR gates (U268, U269) and the corresponding circuitry to buffer EMU_TCK added. - 4 Test Points for Gnd added. - ETH_SCK net renamed to ETH_SDA - SIGDETunconnected with LOS; its directly pulled high. R145 and R146 removed - SYSPG_D1 LED changed to Yellow colour from Green	02-APR-2012	eInfochips
	0.2	- 10 nF capacitors (C457 and C460) added on VCC12 input rail of U34. - Capacitors on CVDD rail optimized from two 220uF, two 100uF and four 47uF to two 100uF and two 47uF. - Capacitors on VCC1V0 rail optimized from one 220uF, three 47uF and one 10uF to two 47uF and one 10uF. - An additional 22uF cap (C549) added on VCC12 input for U29. C426 changed from 10nF to 100nF. - R183 changed to 1K from 4.7K. - SIGDET connected to VCC2V5 using R146. - R1273 changed to 4.7K from 10K.	02-MAY-2012	eInfochips
	0.3	- L15 and L16 changed to 2.3uH and 1.2uH respectively - R251 and R373 changed to 22.1K - C549 moved before B158 on 12V plane - C2325 changed from 100nF to 10uF - R2203 made NU and R2226 to be mounted	07-MAY-2012	eInfochips
	0.4	- NOR Flash density label corrected to 32 Mb from 16MB.	20-JUL-2012	eInfochips
	0.5	- DISCLAIMER Changed	26-JUL-2012	eInfochips
	0.6	- Asthetical Change Name swap between LVDS and HCSL on page 18	06-DEC-2012	eInfochips
	0.7	- Asthetical Change Note for DDR3 Slew-Rate setting corrected on page 14	29-JAN-2013	eInfochips
	0.8	- R82 and R83 changed to 10K - R85 and R957 made NU	22-FEB-2013	eInfochips
	0.9	- The Resistors R896,R67 and capacitor C555 are redundant components on EMU_TCK and can be NU from design. - Pull-up resister R1119 on EMU_TCK change from 10K to 4.7K	28-NOV-2013	eInfochips

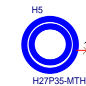
Dummy Components

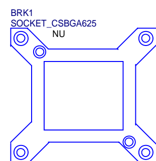




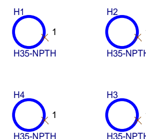


AMC Hole

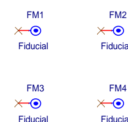




Mounting Holes



On Board Fiducials



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