

K2GEVM

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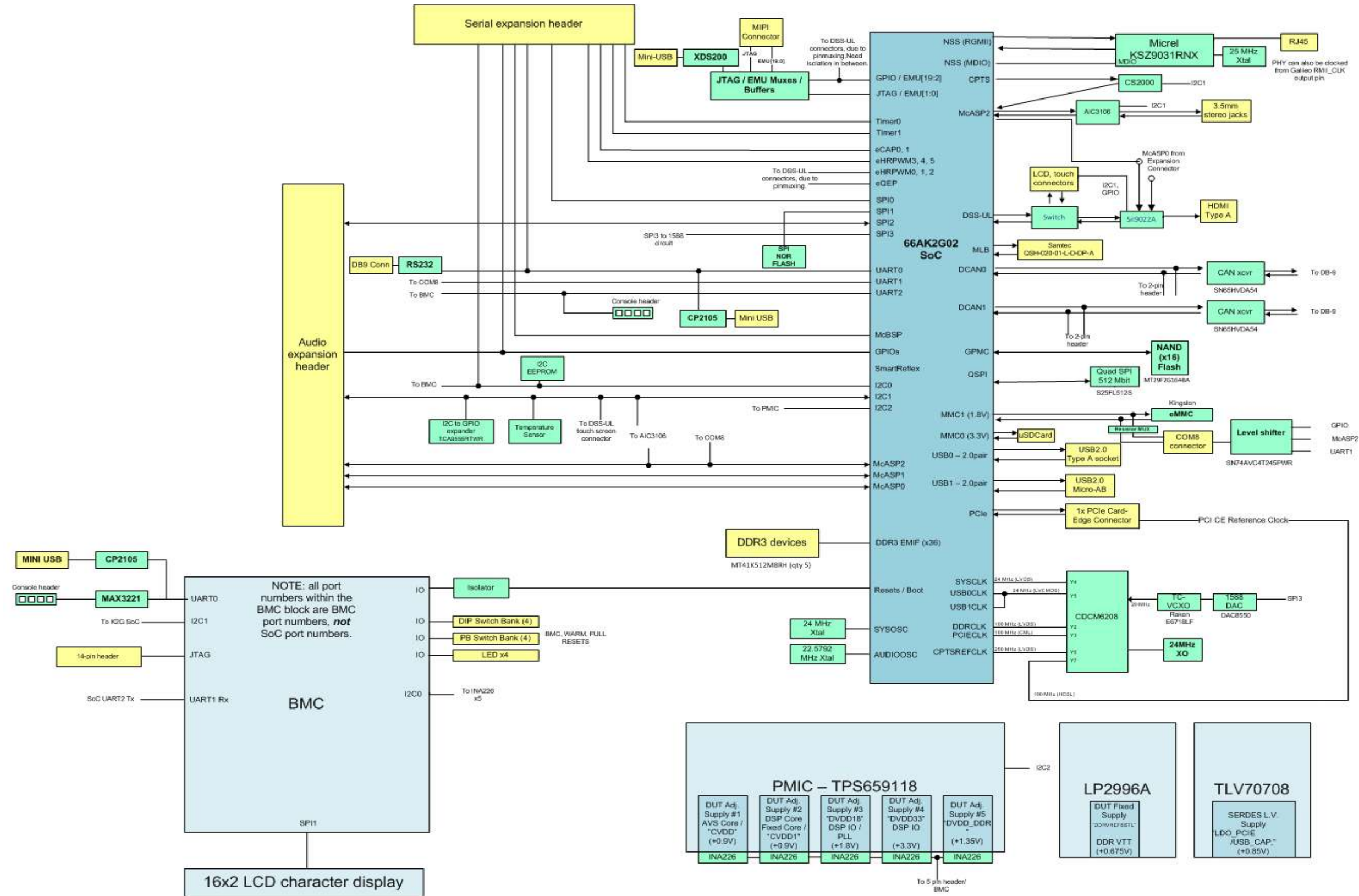
REV	D
VER	1.5

REVISION HISTORY

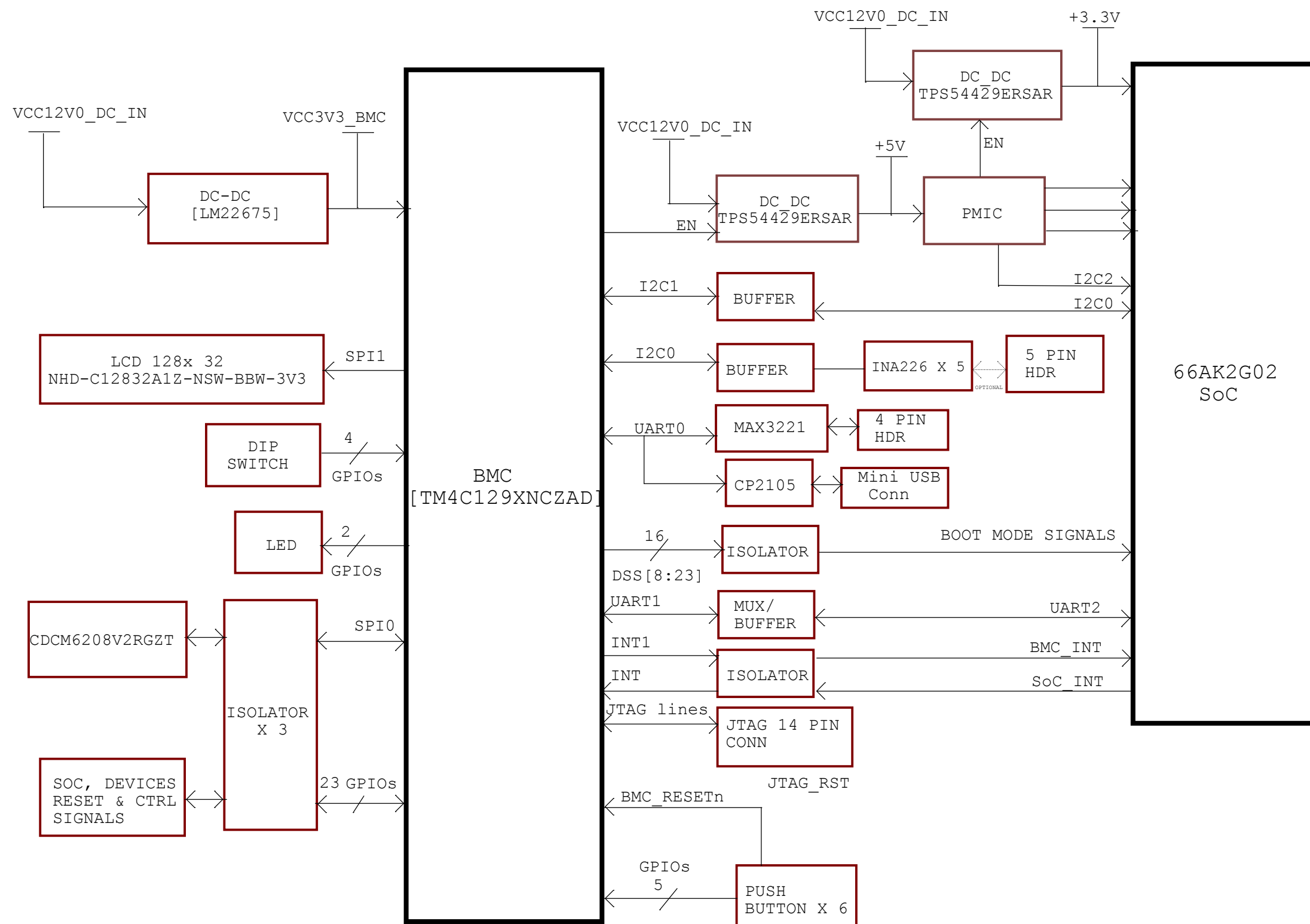
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
0.1	12th OCT 2015	QSPI Buffer Removed (U148,C823,R916) ,R463 Mounted Over Voltage Protection Circuit Added in Page 50	Mistral Design Team
0.2	19th OCT 2015	AA19,AB19,Y20,W19,D2,L2,G3,F18,H2,AA18,Y19,Y14,H5 and M5 balls of the processor renamed R737 added R176,R184,R191,R198 changed to pull down R197,R190,R183,R175 changed to pull up	Mistral Design Team
0.3	28th OCT 2015	R927 added b/w SOC and BMC Net "SOC_BAWCLKSEL" renamed as "RSV6_TOGGLE"	Mistral Design Team
0.4	29th OCT 2015	Nets BAW_ATEST, VDDA_BAW, VDD18_BAW are renamed as RSV7_ATEST, VDDA_0V9 ,VDD18_1V8	Mistral Design Team
0.5	4th NOV 2015	"M5" & "H5" pins of processor moved to corresponding power domain symbol parts " M5 " pin of processor tied directly to CVDD1 FB18,C186,C526 Removed Tittle block updated as per customer request	Mistral Design Team
0.6	11th NOV 2015	U142 replaced with TXS0108EPWR R58 made DNI	Mistral Design Team
0.7	16th NOV 2015	R769 R562,R764 are made DNI due to internal pull up/down in TPD12S016	Mistral Design Team
0.8	8th DEC 2015	Customer comments updated	Mistral Design Team
1.0	11th DEC 2015	Beta ECR/ECN implemented Baselined schematics	Mistral Design Team
1.1	18th JAN 2016	R374 and R370 mounted	Mistral Design Team
1.2	4th MAR 2016	R431 and R442 value changed to 200E	Mistral Design Team
1.3	23rd MAR 2016	VCNTL[0:5] pin names of U1-32 renamed as RSV[13:18]	Mistral Design Team
1.4	28th MAR 2016	Hided VCNTL[0:5] net labels of U1-32	Mistral Design Team
1.5	12th APR 2016	SOC pin names updated as per datasheet ' SPRS932A-DECEMBER 2015-REVISED FEBRUARY 2016 '	Mistral Design Team

Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title REVISION HISTORY	
K2G EVM	 	Size C	Document Number MS_TI_K2GEVM_SCH_REVD
		Date: Wednesday, April 13, 2016	Rev D
		Sheet 2 of 50	

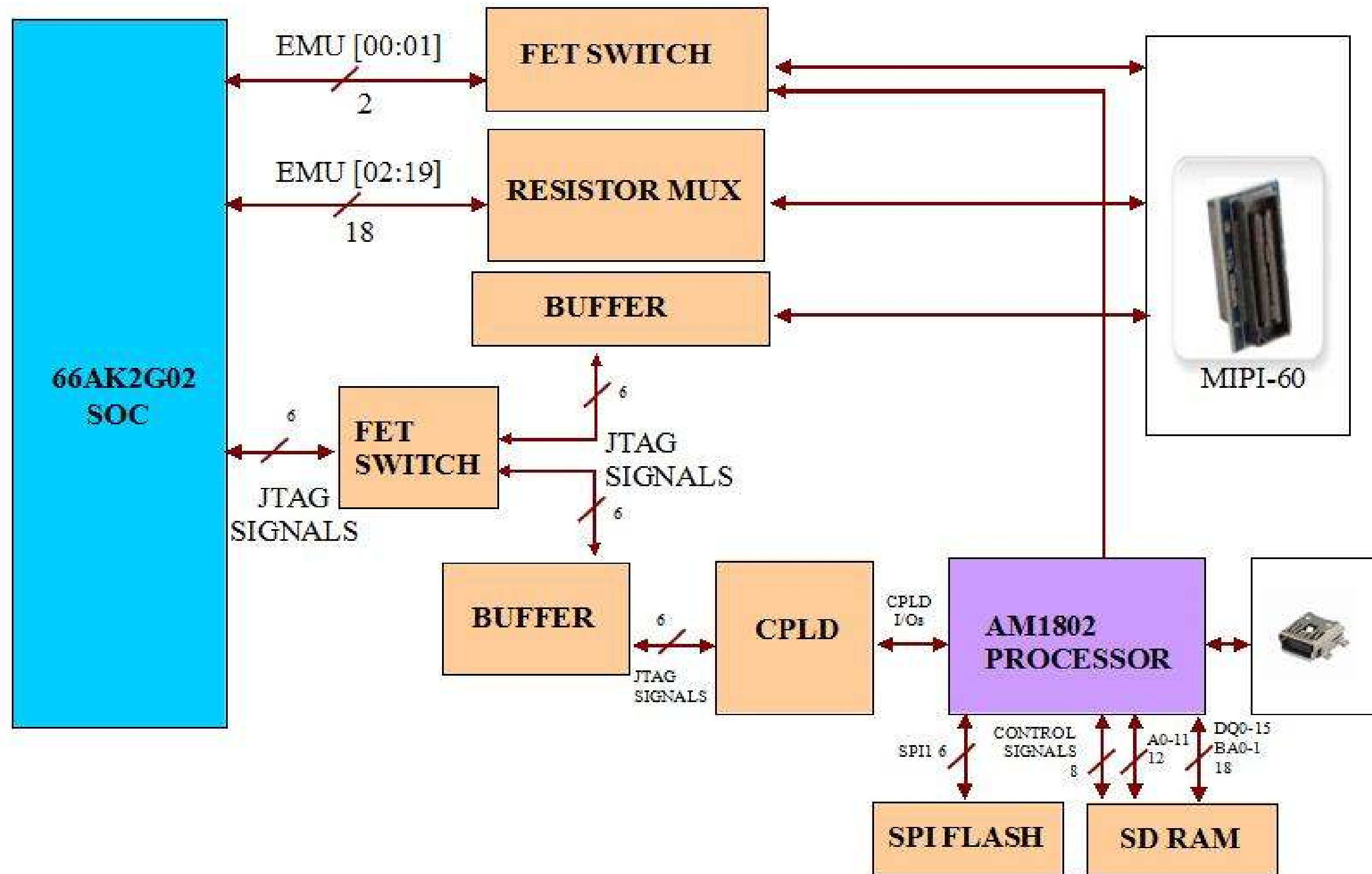
BLOCK DIAGRAM - K2GEVM



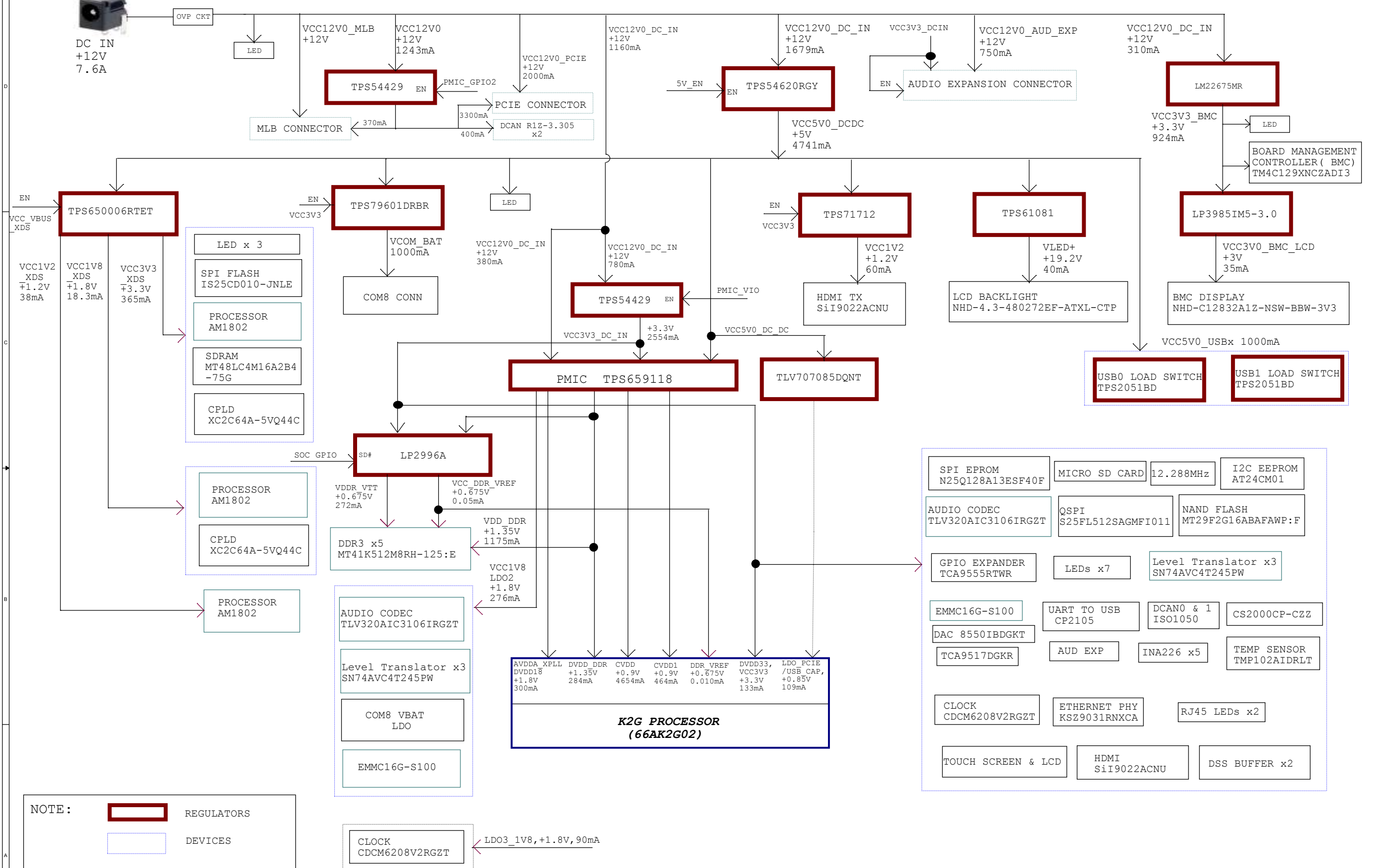
BLOCK DIAGRAM - BMC



BLOCK DIAGRAM - XDS200



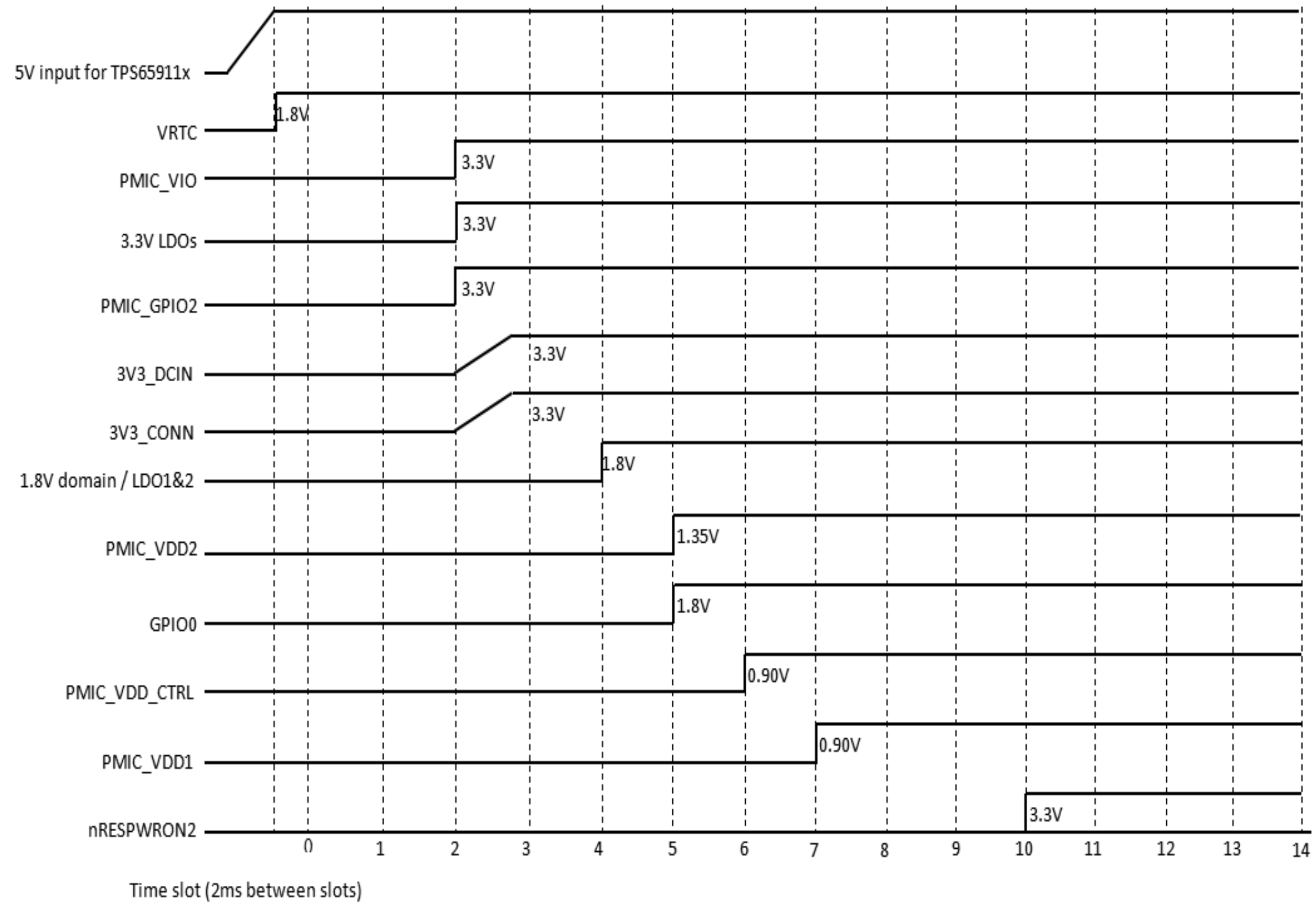
POWER FLOW DIAGRAM



NOTE:

- REGULATORS
- DEVICES
- Multiple powered device

BOARD POWER UP SEQUENCE



SoC I2C ADDRESS TABLE

I2C0 DEVICES	7 BIT ADDRESS
EEPROM	0x50 (PAGE 0)
	0x51 (PAGE 1)
BMC	0x0 (PROGRAMMABLE)
SERIAL EXPANSION CONNECTOR	TBD
PCIe CONNECTOR	TBD

I2C2 DEVICES	7 BIT ADDRESS
PMIC	0x2D (GENERAL PURPOSE) TBD
	0x12 (VOLTAGE SCALING) TBD

I2C1 DEVICES	7 BIT ADDRESS
HDMI TRANSMITTER	0x3B
	0x3F
	0x62
AUDIO CODEC	0x1B
TOUCH SCREEN	0x70 (WRITE)
	0x71 (READ)
I/O EXPANDER	0x20
TEMPERATURE SENSOR	0x48
MLB CONNECTOR	TBD
AUDIO EXPANSION CONNECTOR	0x4A, 0x4B, 0x4C, 0x4D
CLOCK GENERATOR (CS2000CF-CZZ)	0x4F

BMC I2C ADDRESS TABLE

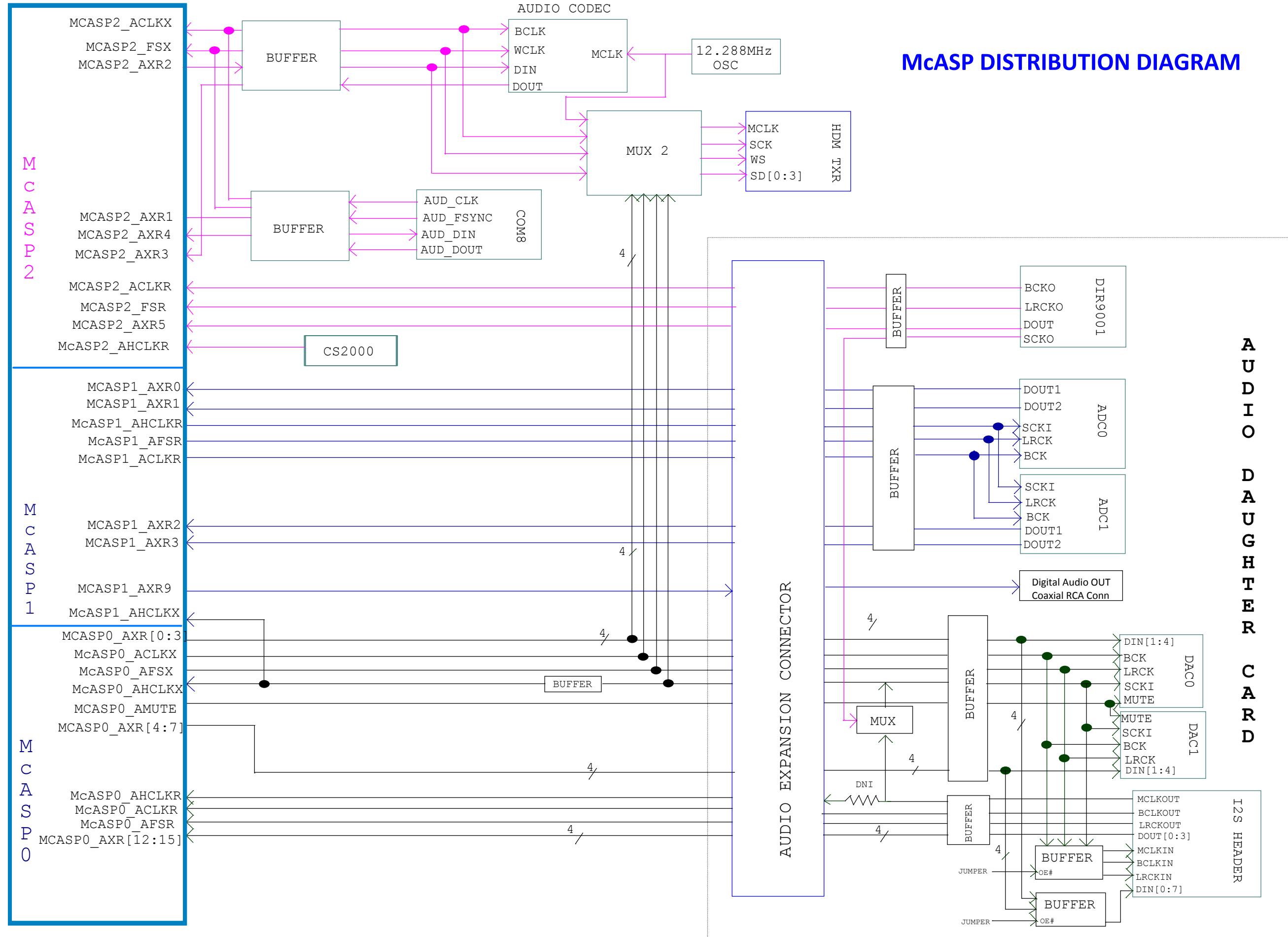
BMC I2C0 DEVICES	7 BIT ADDRESS
PMBUS	0x40 : 3.3V
	0x41 : CVDD
	0x42 : CVDD1
	0x43 : 1.8V
	0x44 : DVDD_DER

BMC I2C1 DEVICES	7 BIT ADDRESS
PROCESSOR	ALWAYS MASTER

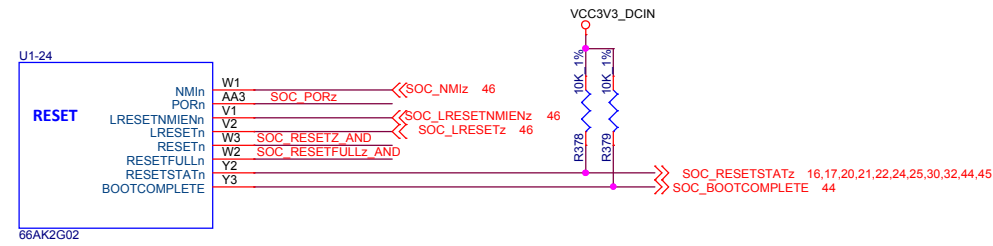
McASP CONFIGURATION

McASP PORT	DEVICES	DEVICE MODE
McASP0	DAC- PCM1690 x2	SLAVE
	I2S HEADER	MASTER
McASP1	ADC- PCM1865 x2	SLAVE
McASP2	HDMI TRANSMITTER (DEFAULT)	SLAVE
	AUDIO CODEC AIC3106	
	DIR9001 (DEFAULT)	MASTER
	COM8	

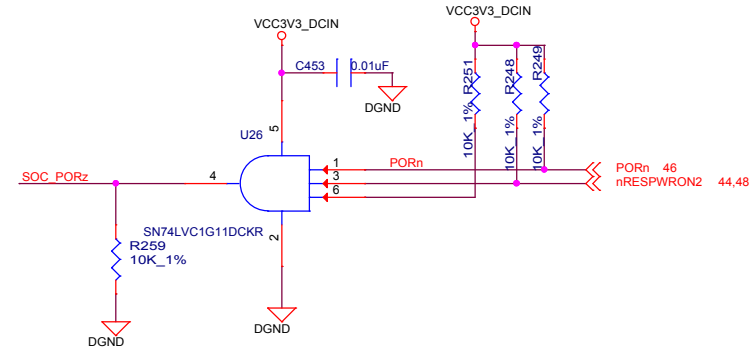
McASP DISTRIBUTION DIAGRAM



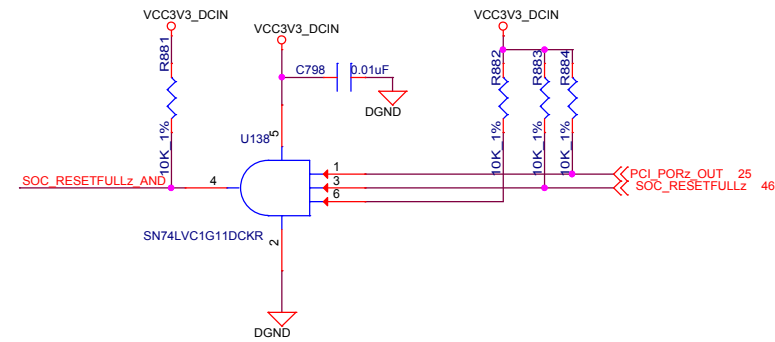
SoC RESET



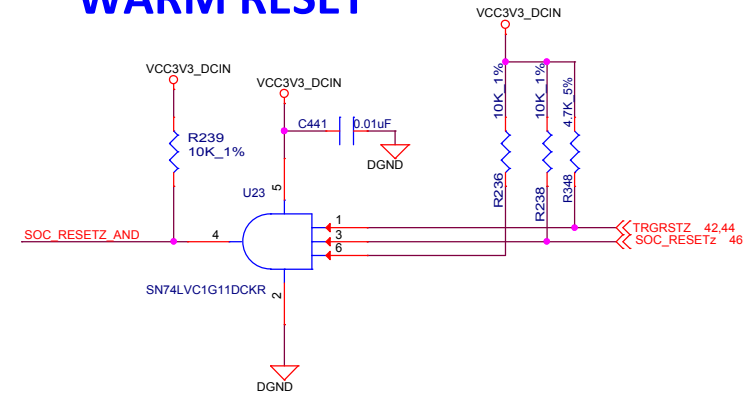
POWER ON RESET



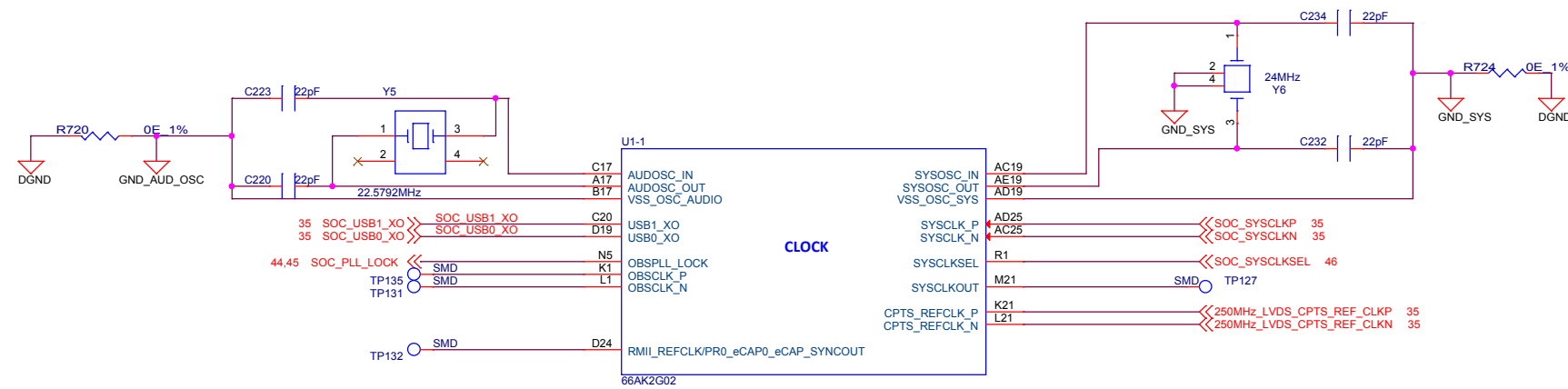
FULL RESET



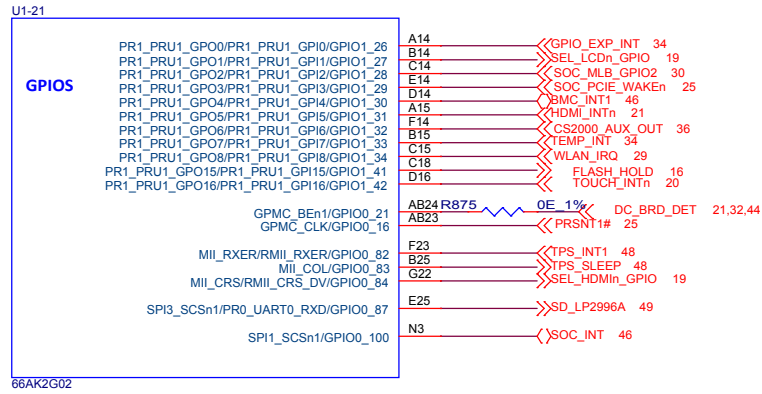
WARM RESET



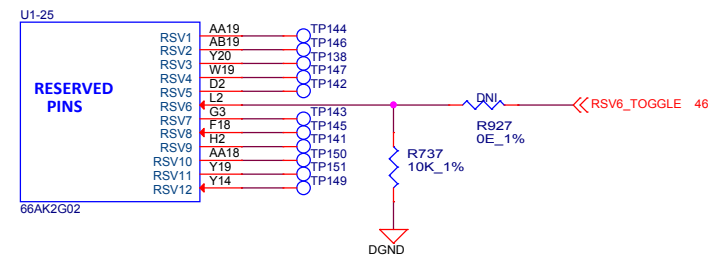
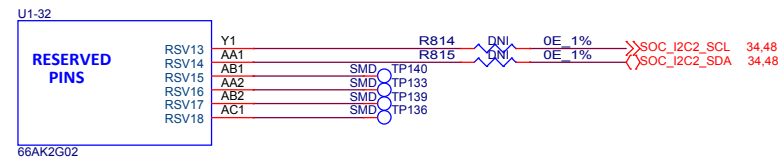
SoC CLOCK



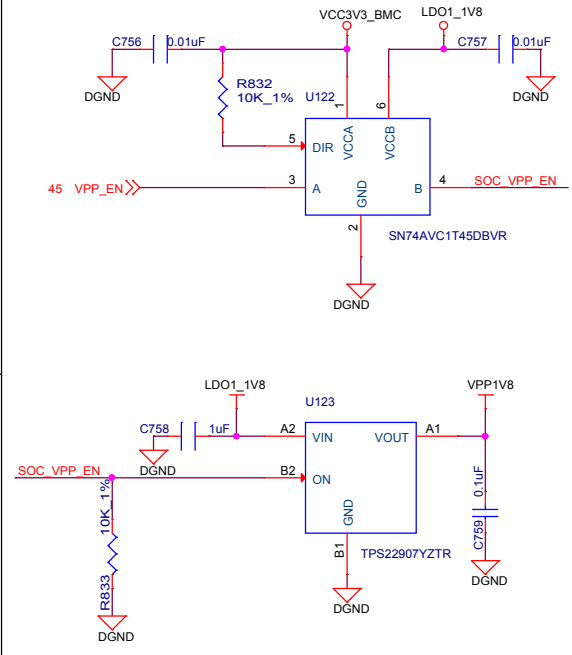
SoC GPIOs



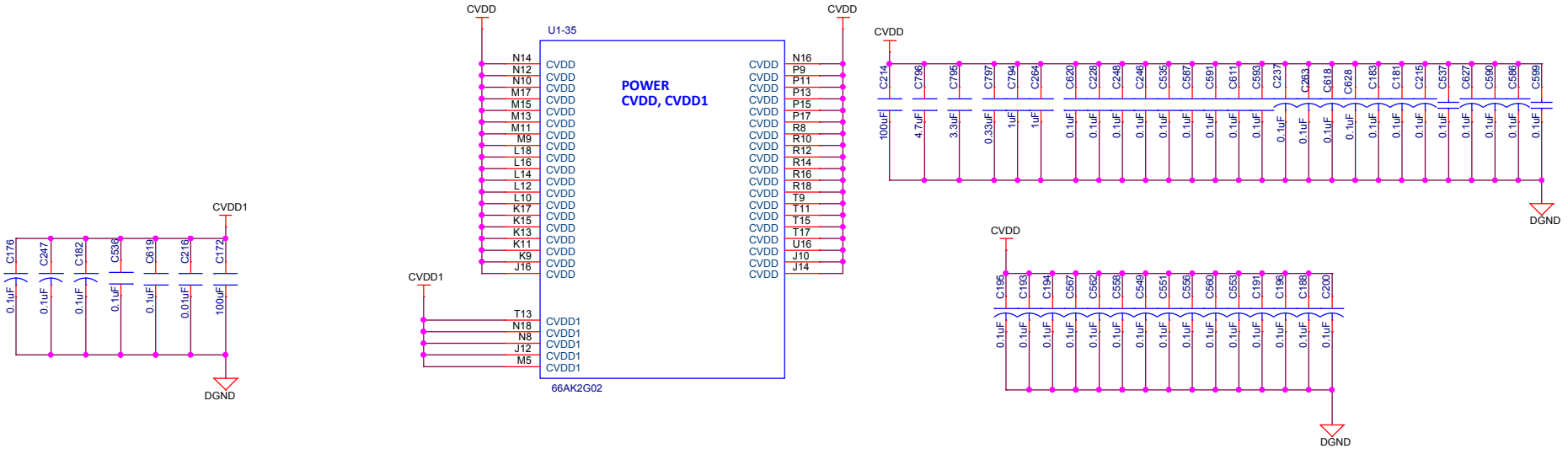
RESERVED PINS



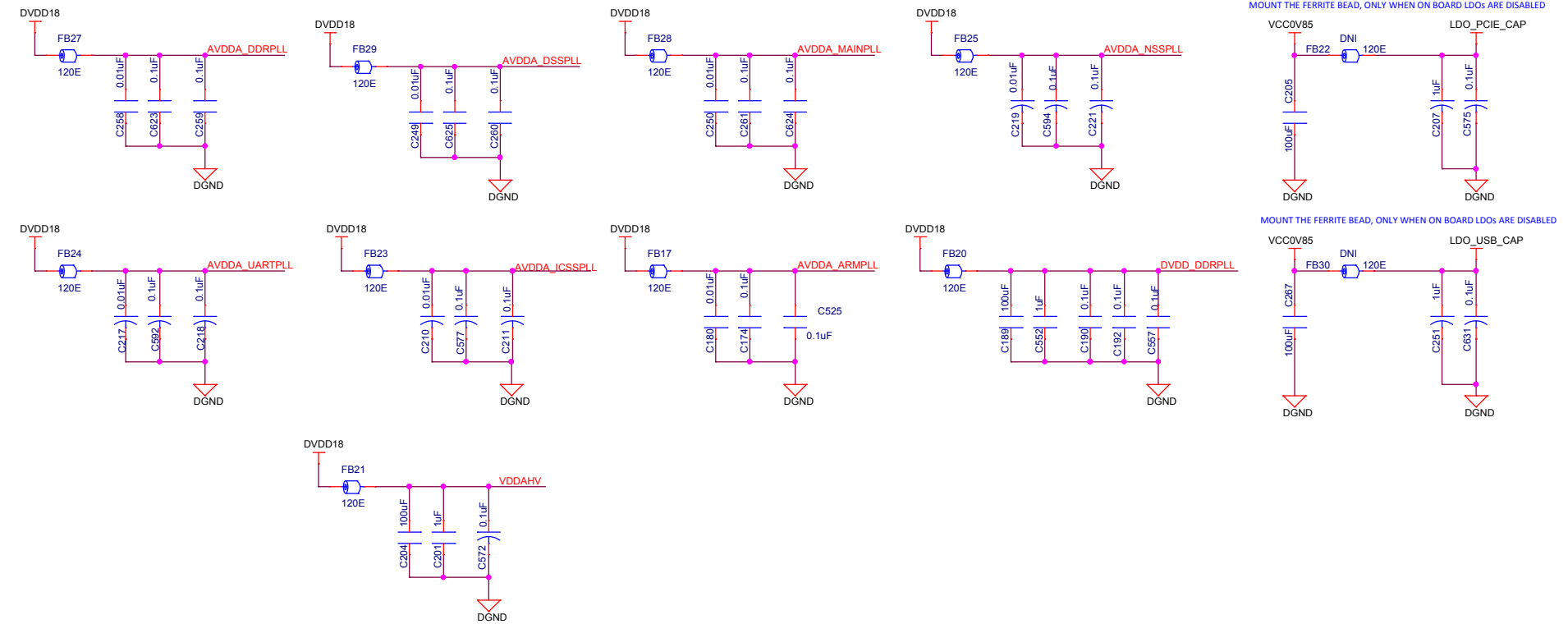
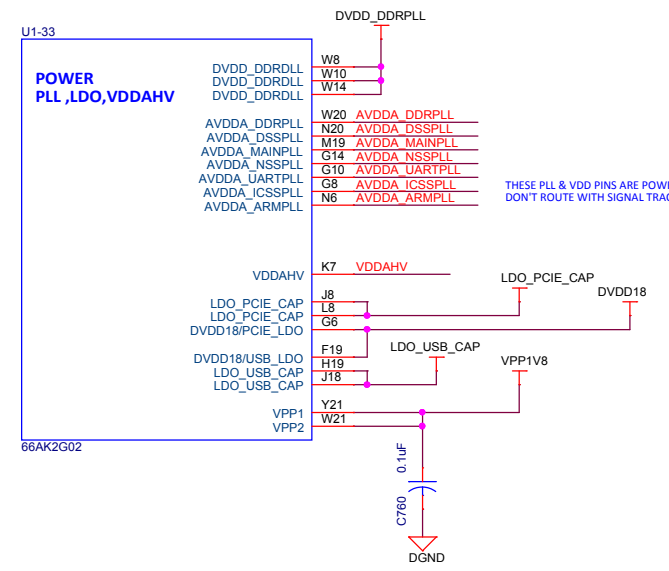
VPP POWER GENERATION



SoC POWER - CVDD, CVDD1

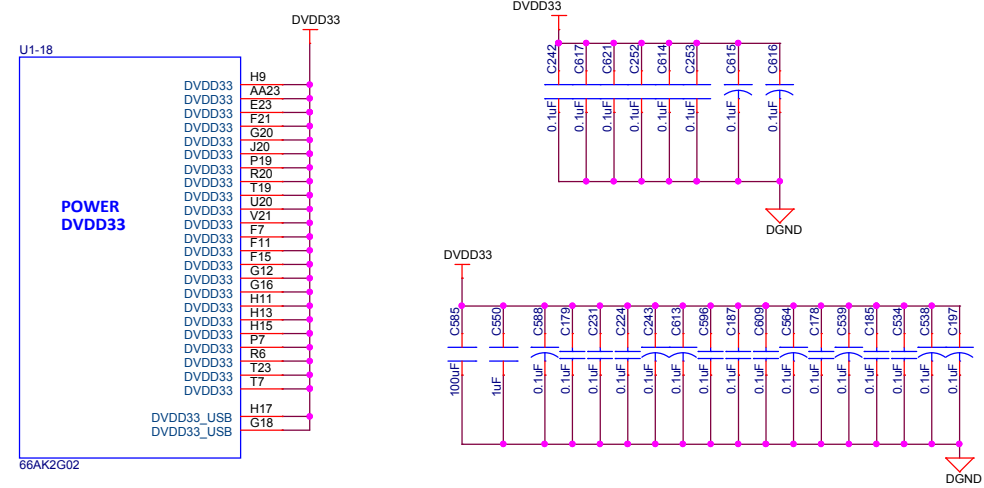


SoC POWER - PLL

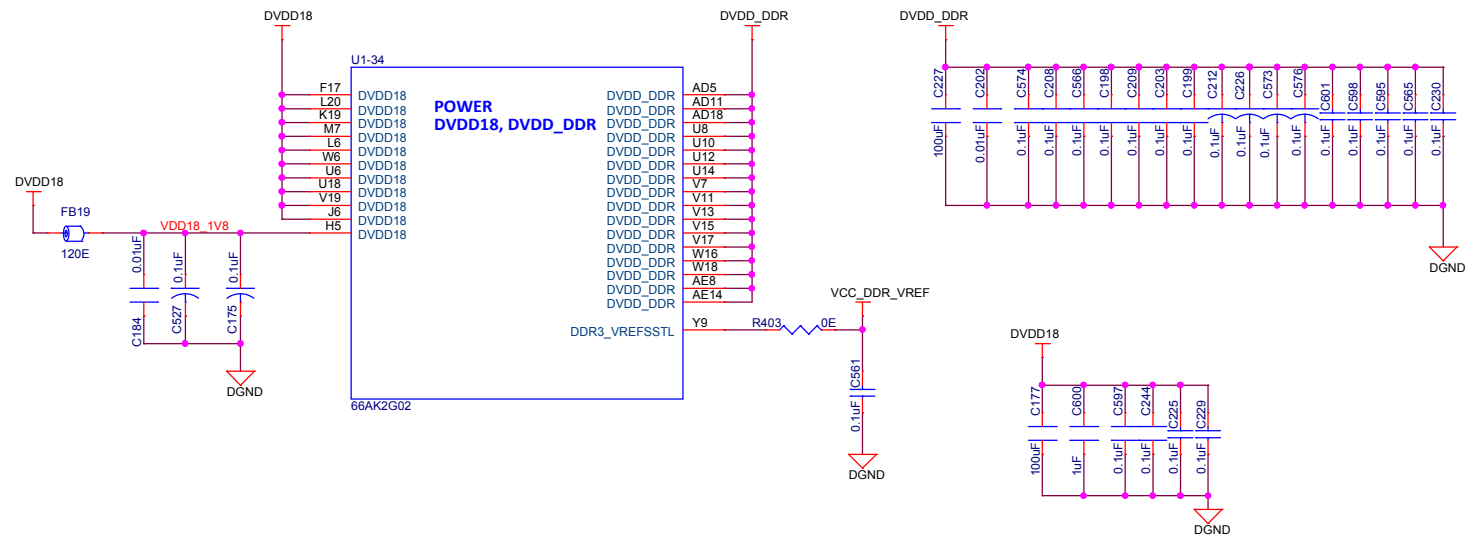


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title : SOC POWER - CVDD, CVDD1 & PLL	
K2G EVM		Size : Document Number	Rev
		C : MS_TI_K2GEVM_SCH_REV D	D
Date : Thursday, April 14, 2016	Sheet 12 of 50		

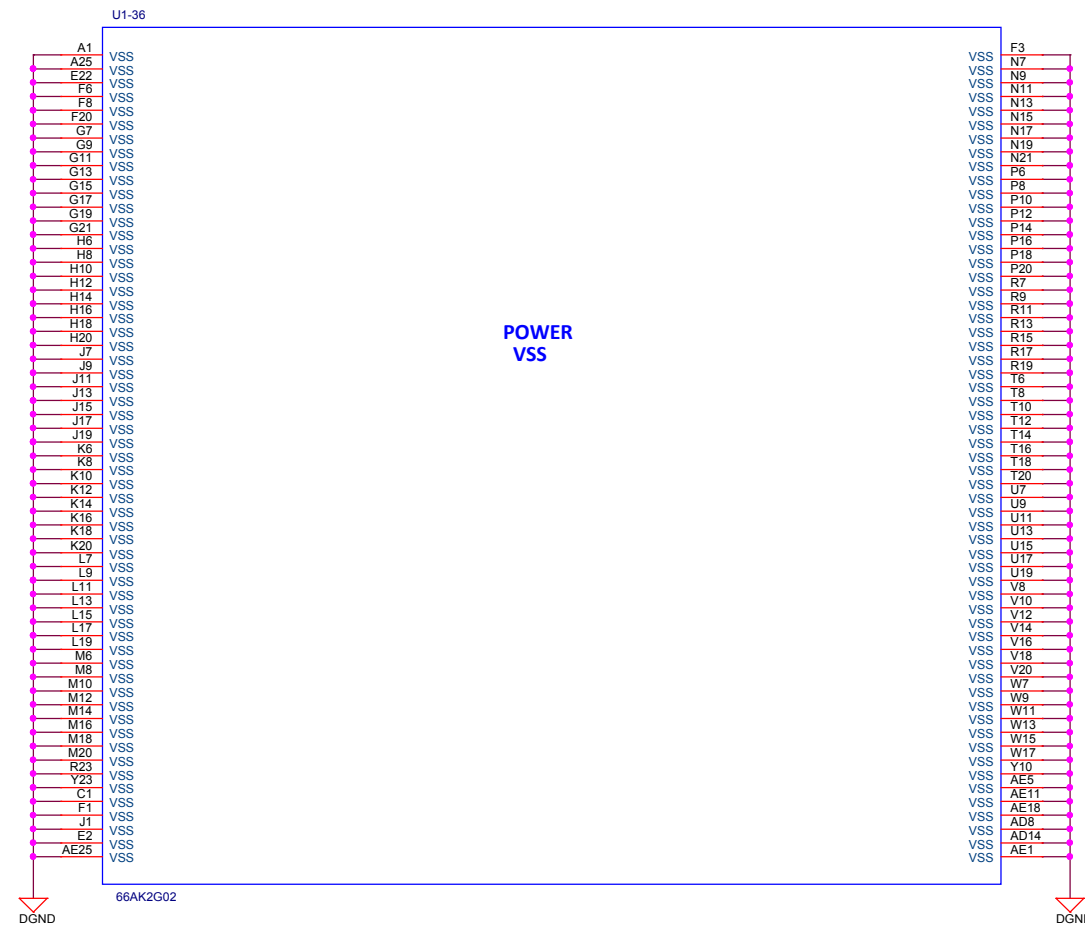
SoC POWER - DVDD33



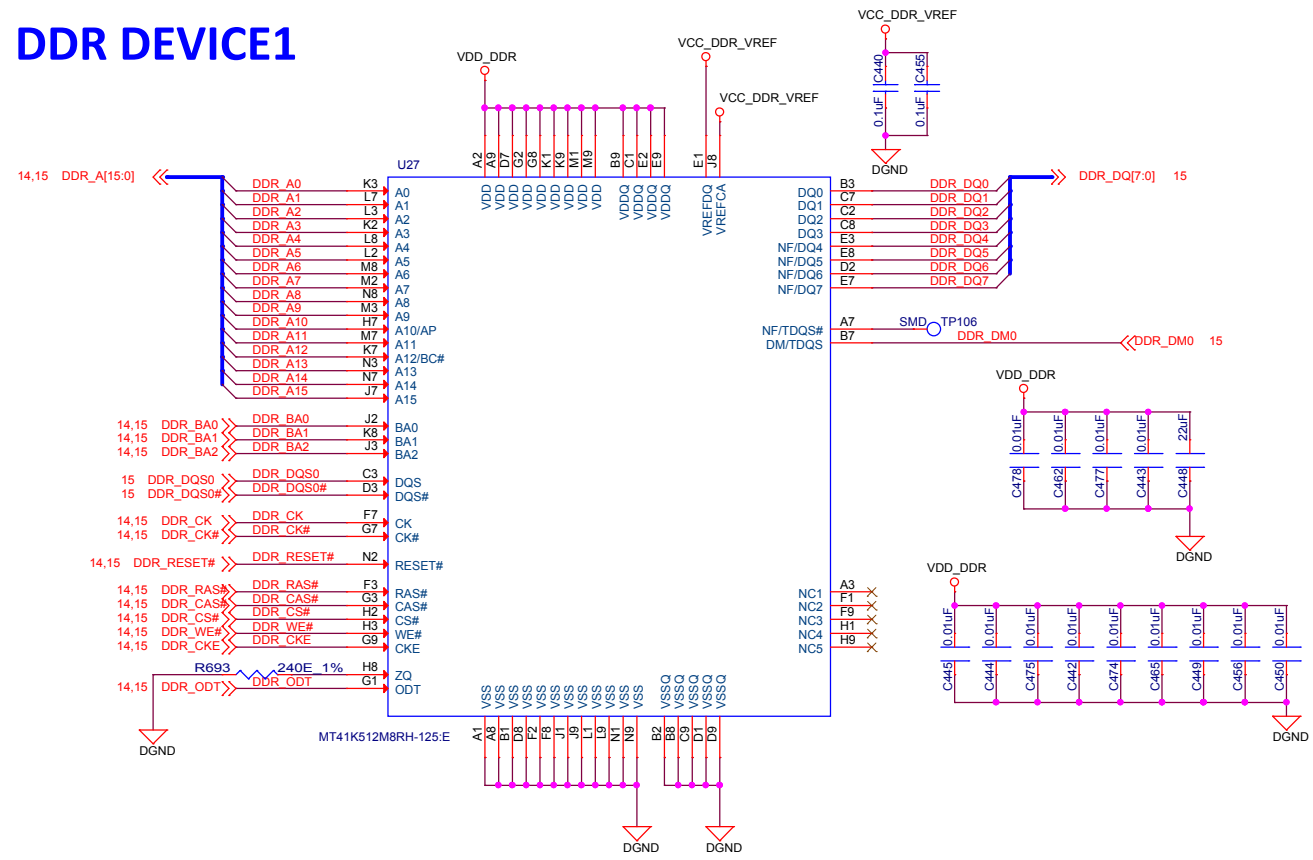
SoC POWER - DVDD18, DVDD_DDR



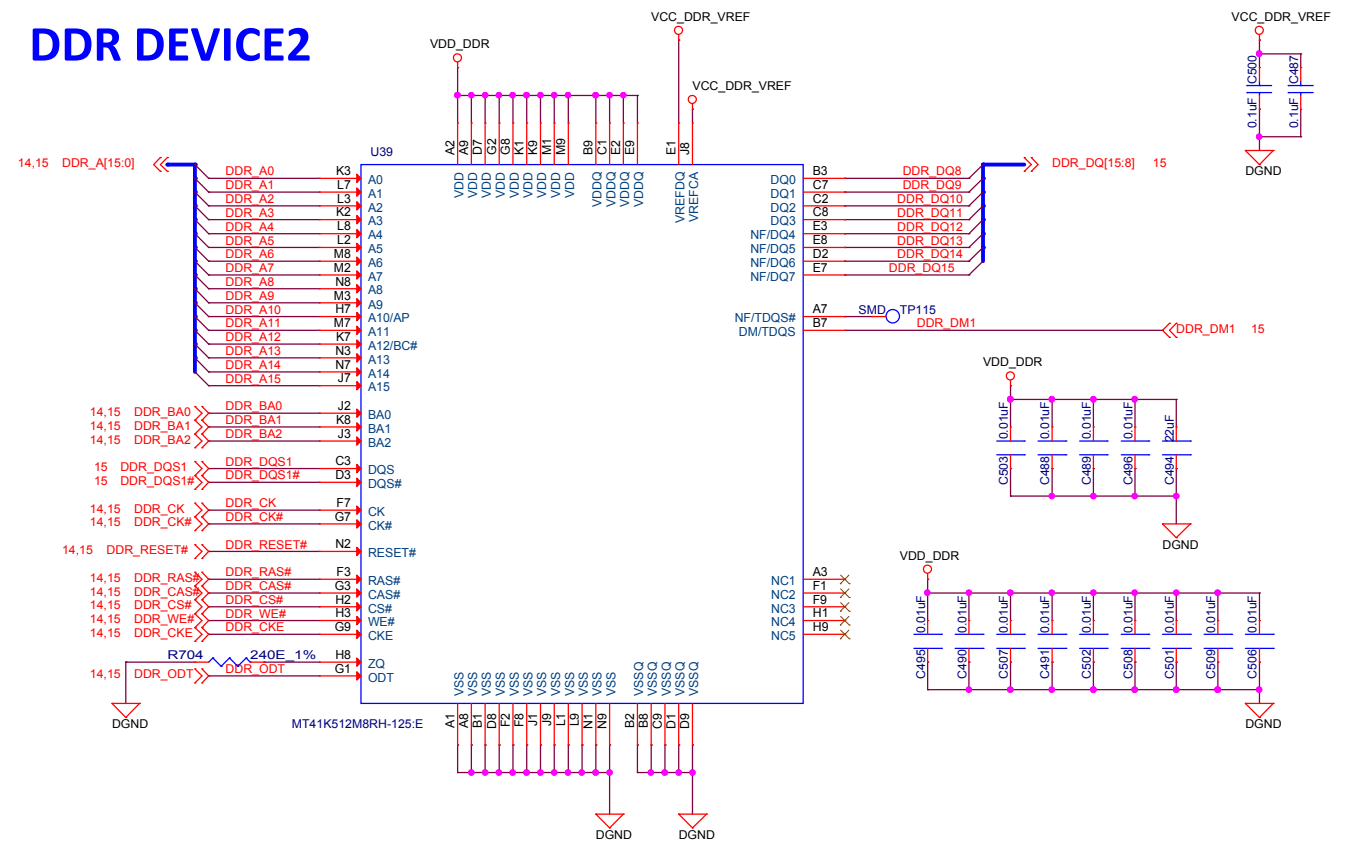
SoC POWER - VSS



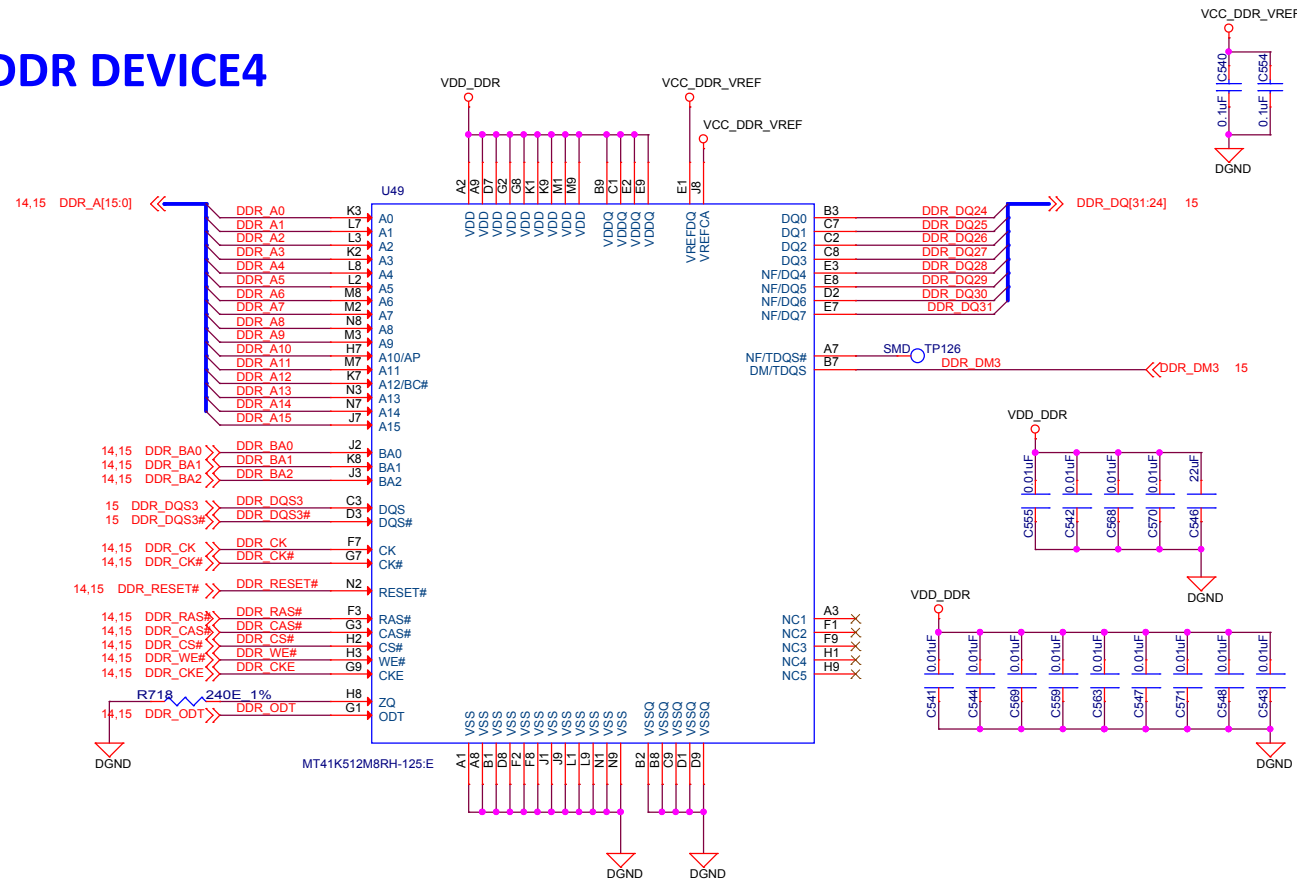
DDR DEVICE1



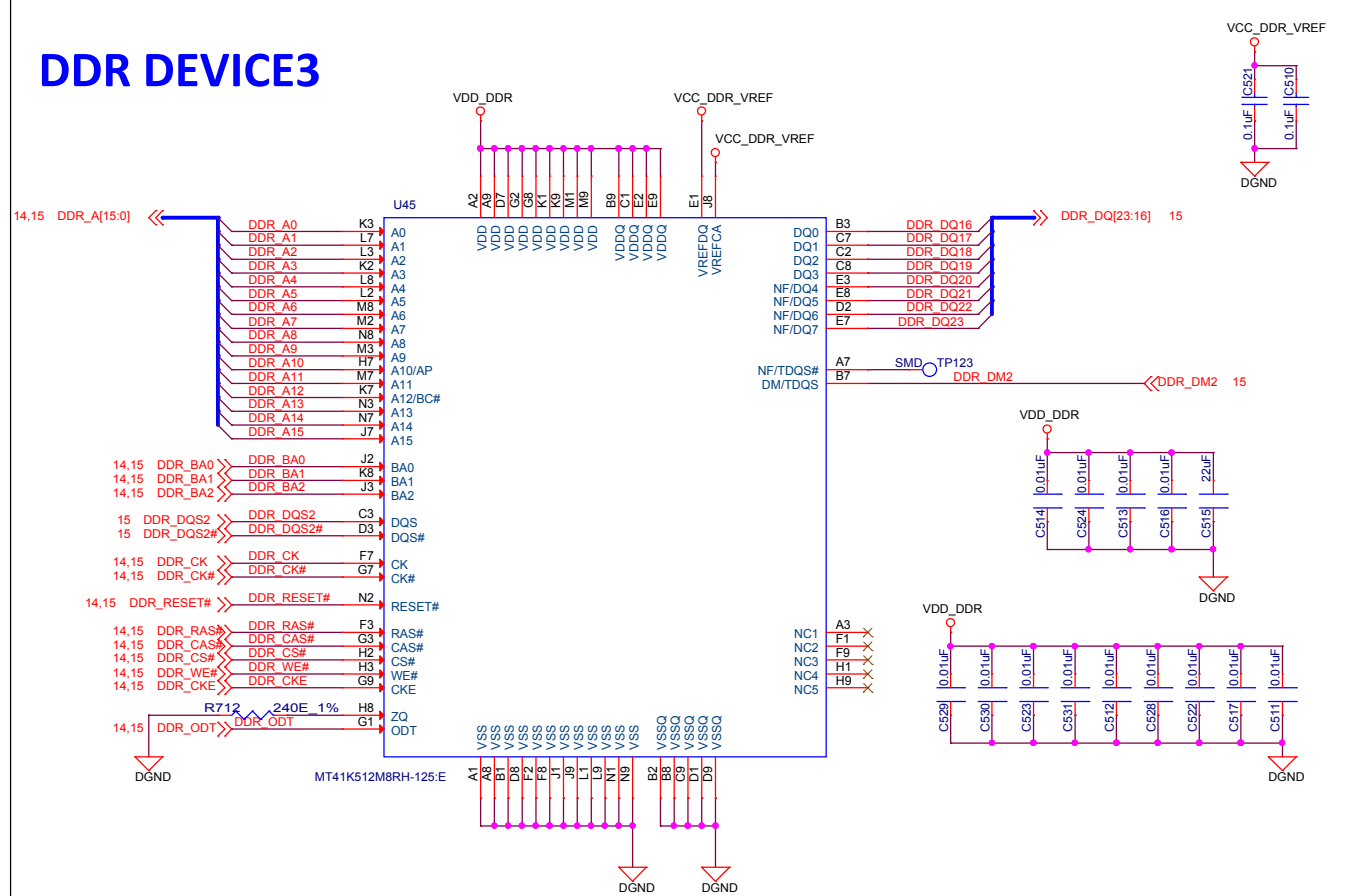
DDR DEVICE2



DDR DEVICE4

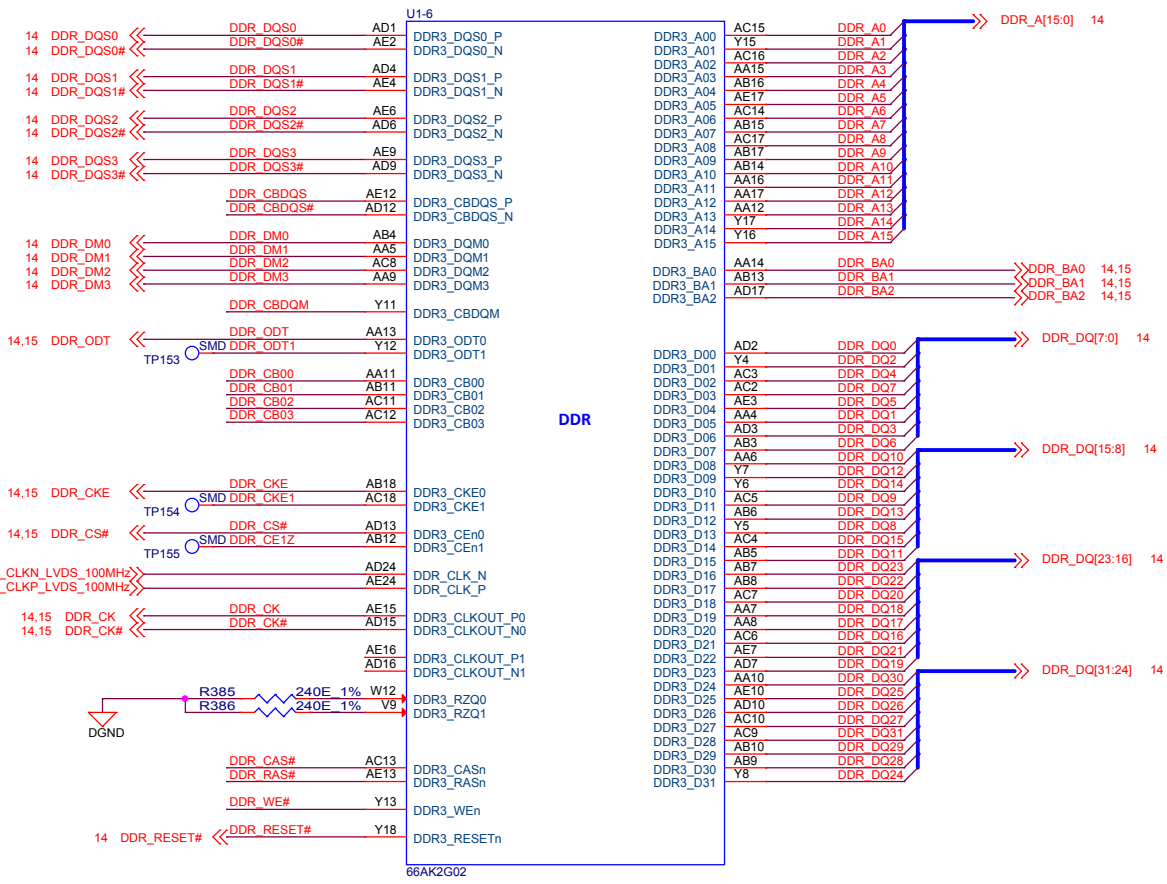
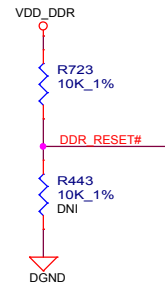


DDR DEVICE3

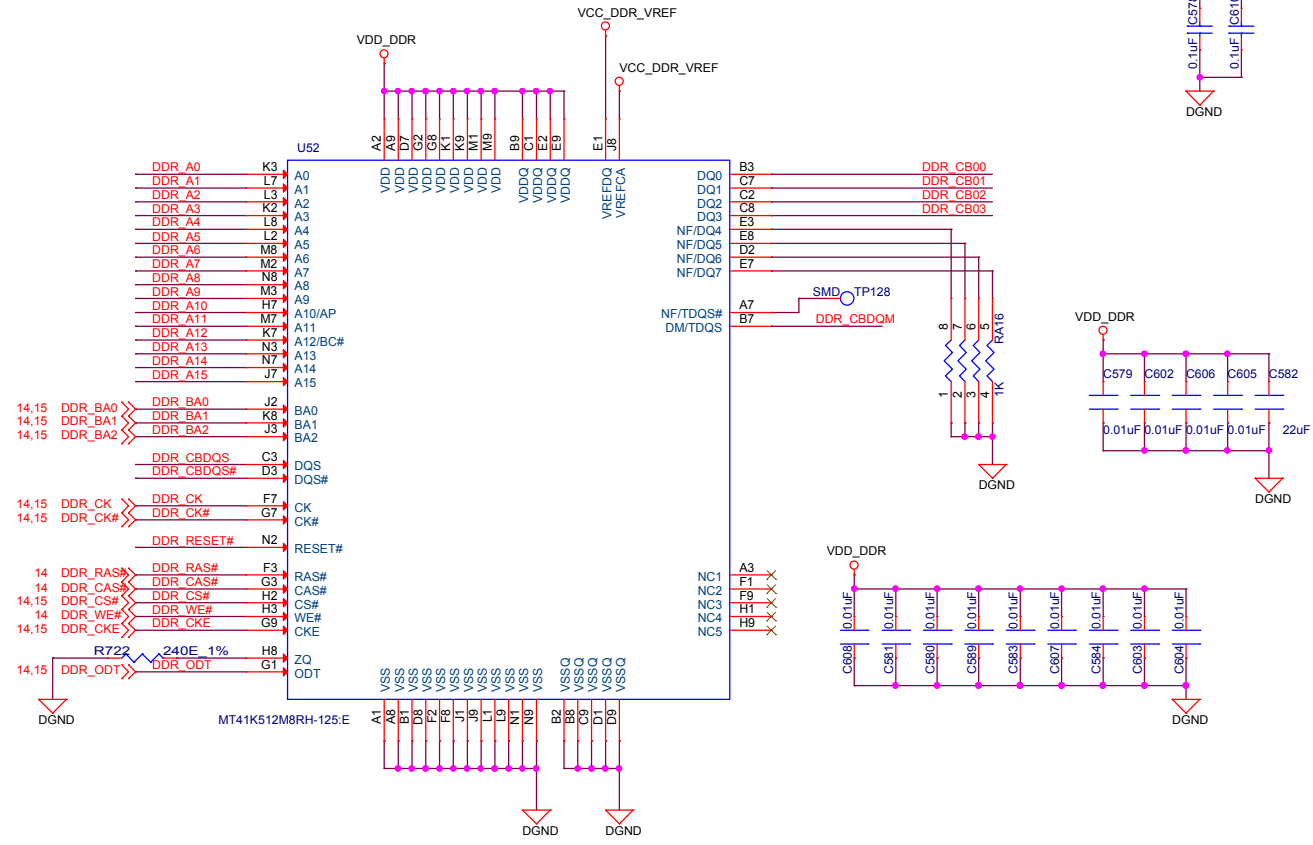


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title DDR3L DEVICES	
K2G EVM	 	Size Document Number	Rev
		C MS_TI_K2GEVM_SCH_REV D	D
Date: Wednesday, April 13, 2016	Sheet 14 of 50		

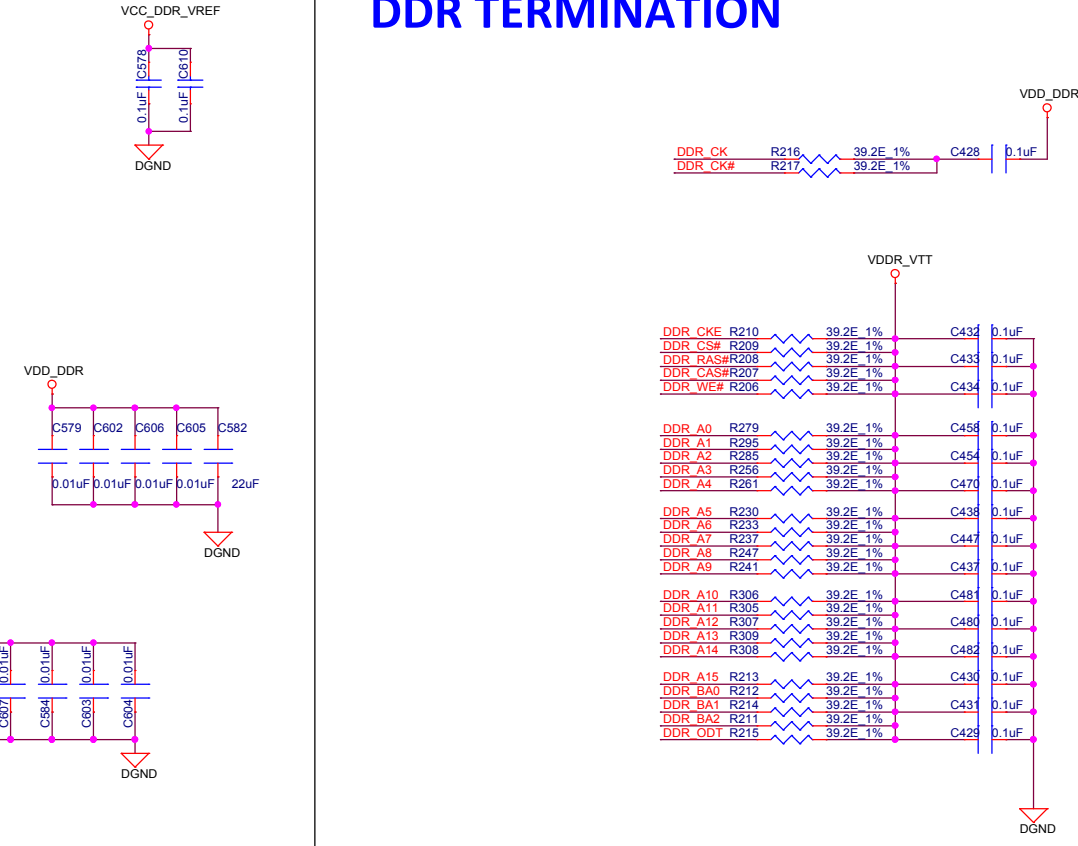
SoC DDR INTERFACE

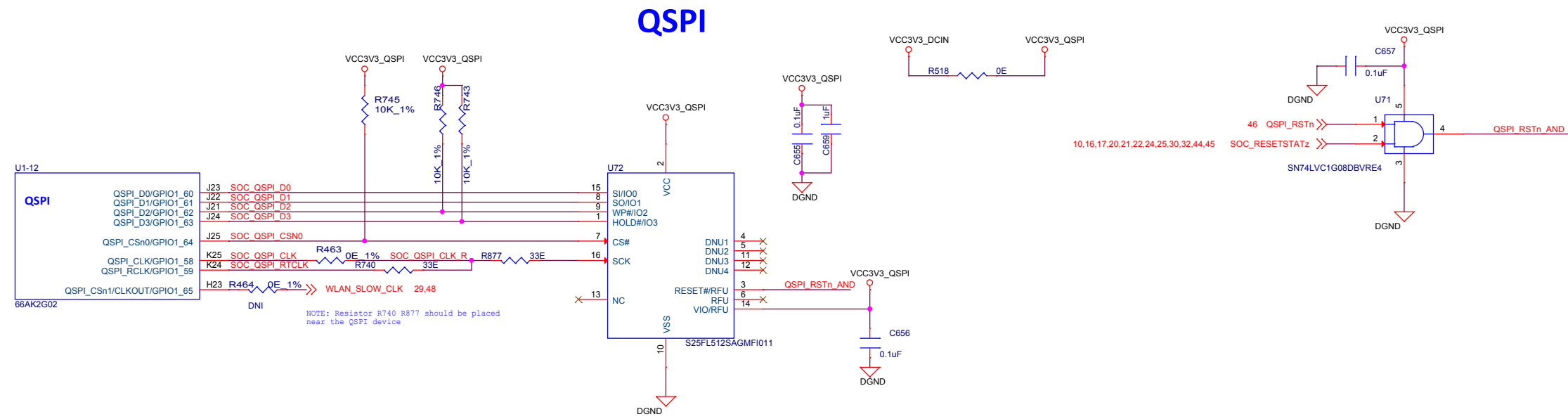


ECC DEVICE

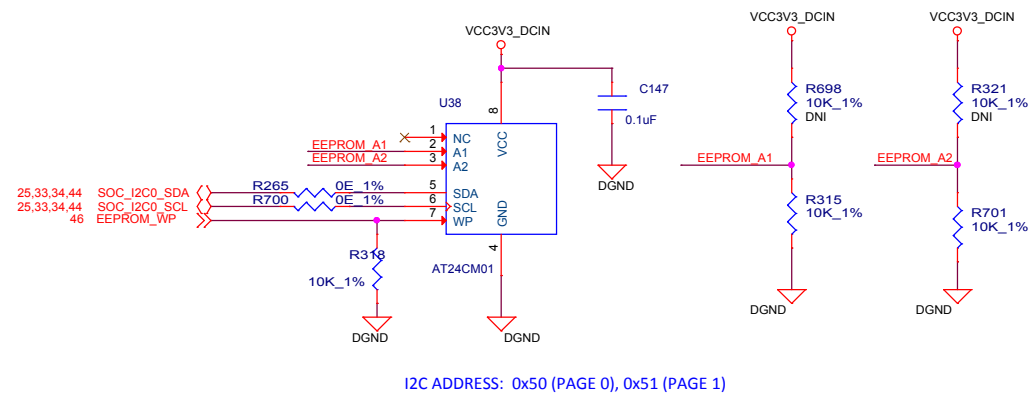


DDR TERMINATION

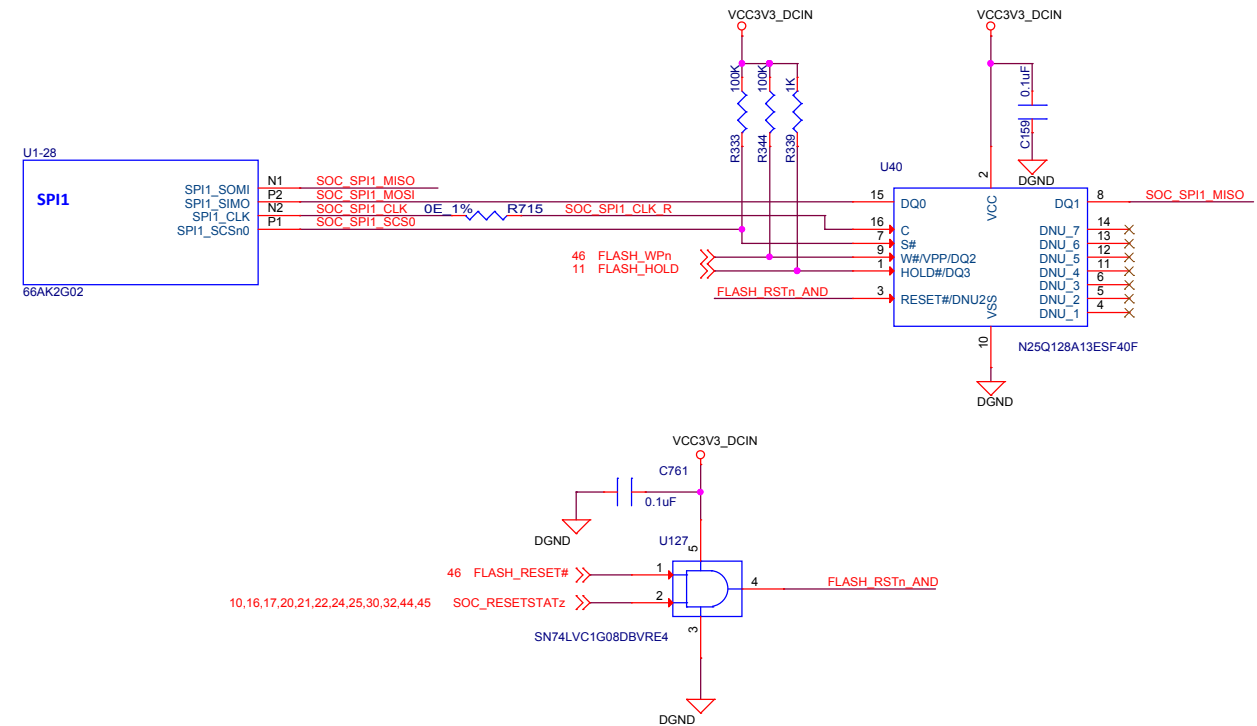




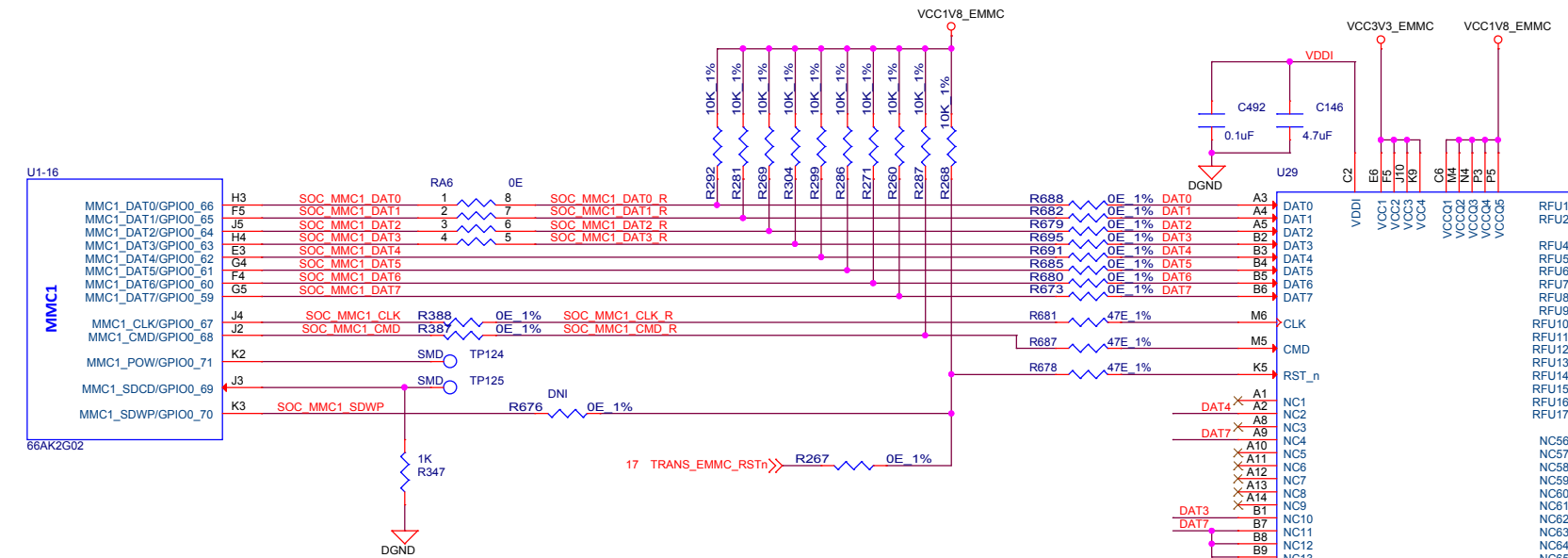
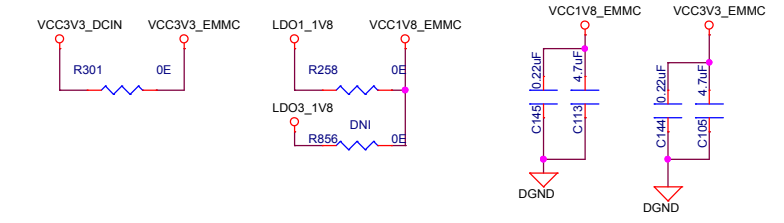
I2C EEPROM FLASH



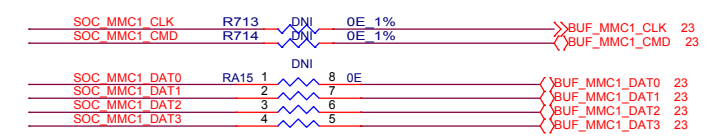
SPI NORFLASH



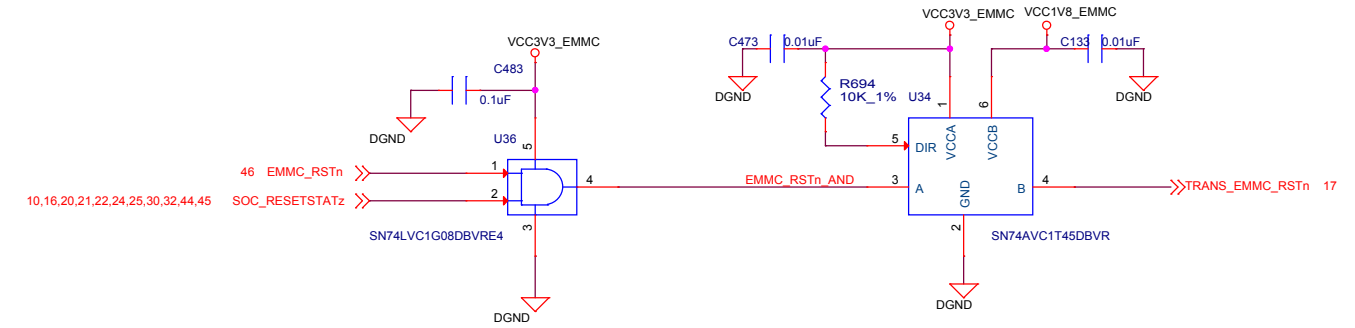
eMMC FLASH



NOTE: MMC1 IS BY DEFAULT CONNECTED TO EMMC. IF COM8 TO BE USED RESISTOR RA6, R387, R388 & R822 SHOULD BE DNI AND RA15, R713, R714 & R393 SHOULD BE MOUNTED



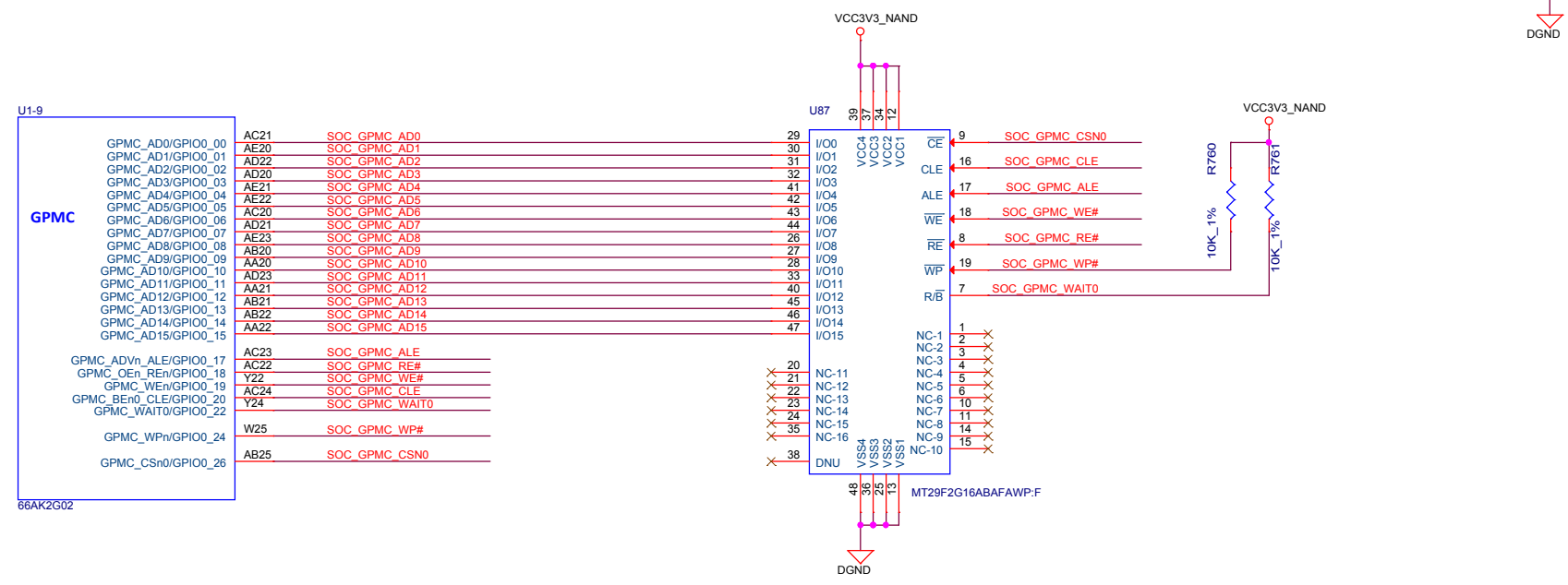
eMMC RESET



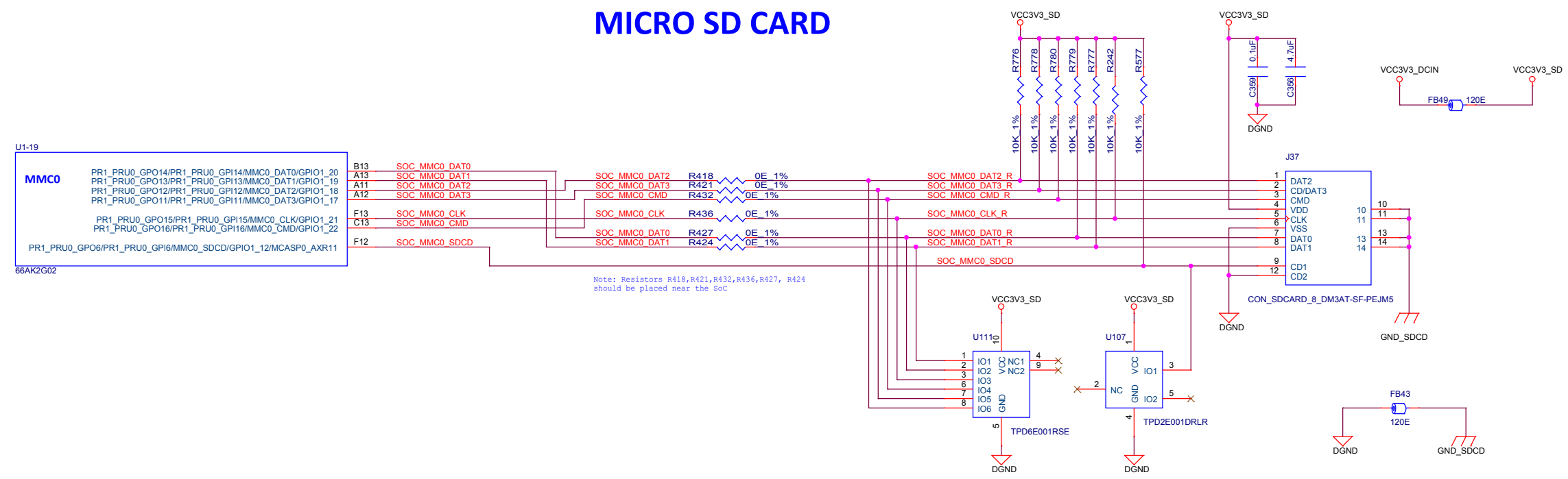
Note: NC pins are connected to eMMC Signals for routing

Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title EMMC FLASH	
K2G EVM		Size	Document Number
		C	MS_TI_K2GEVM_SCH_REV D
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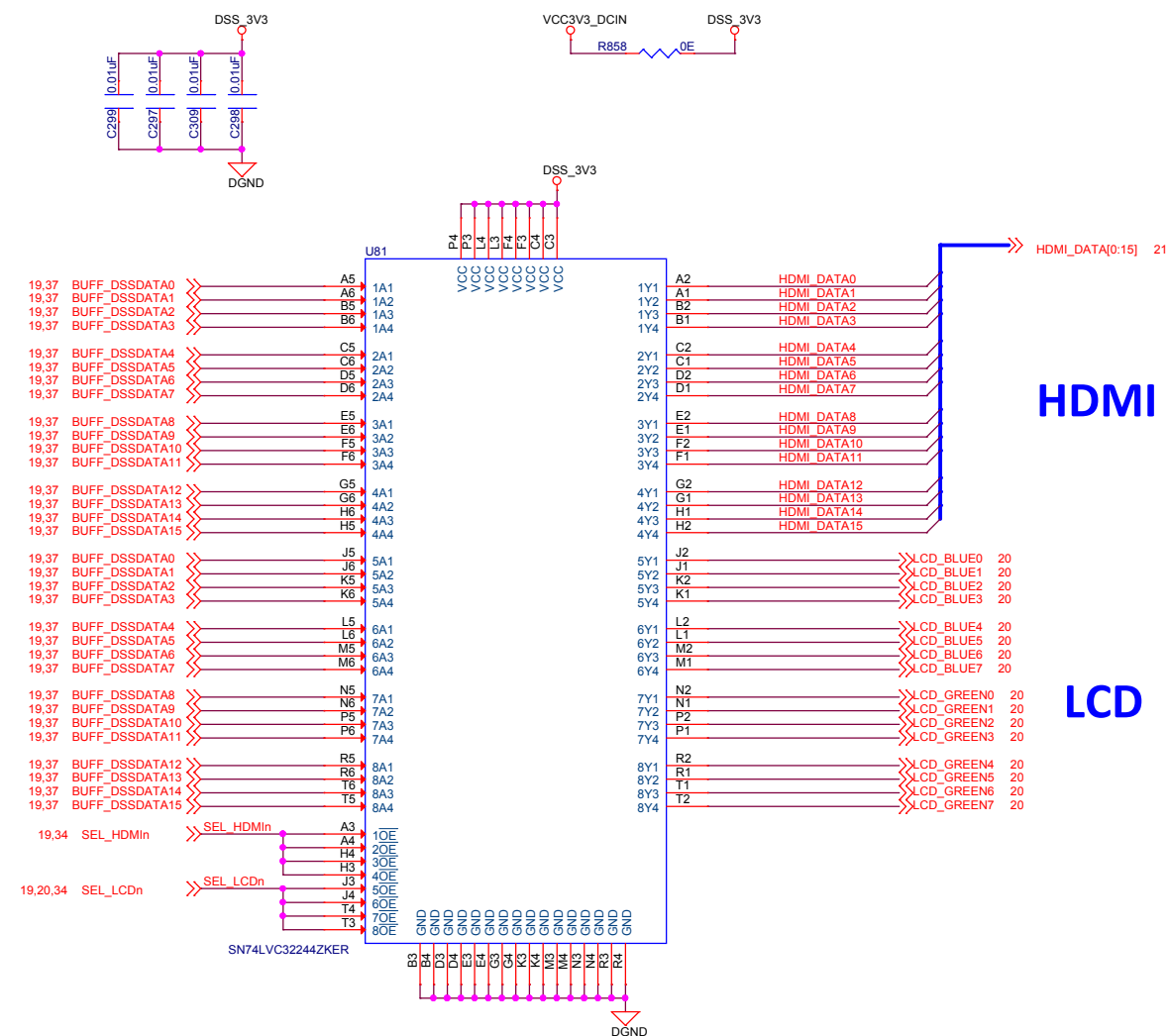
NAND Flash



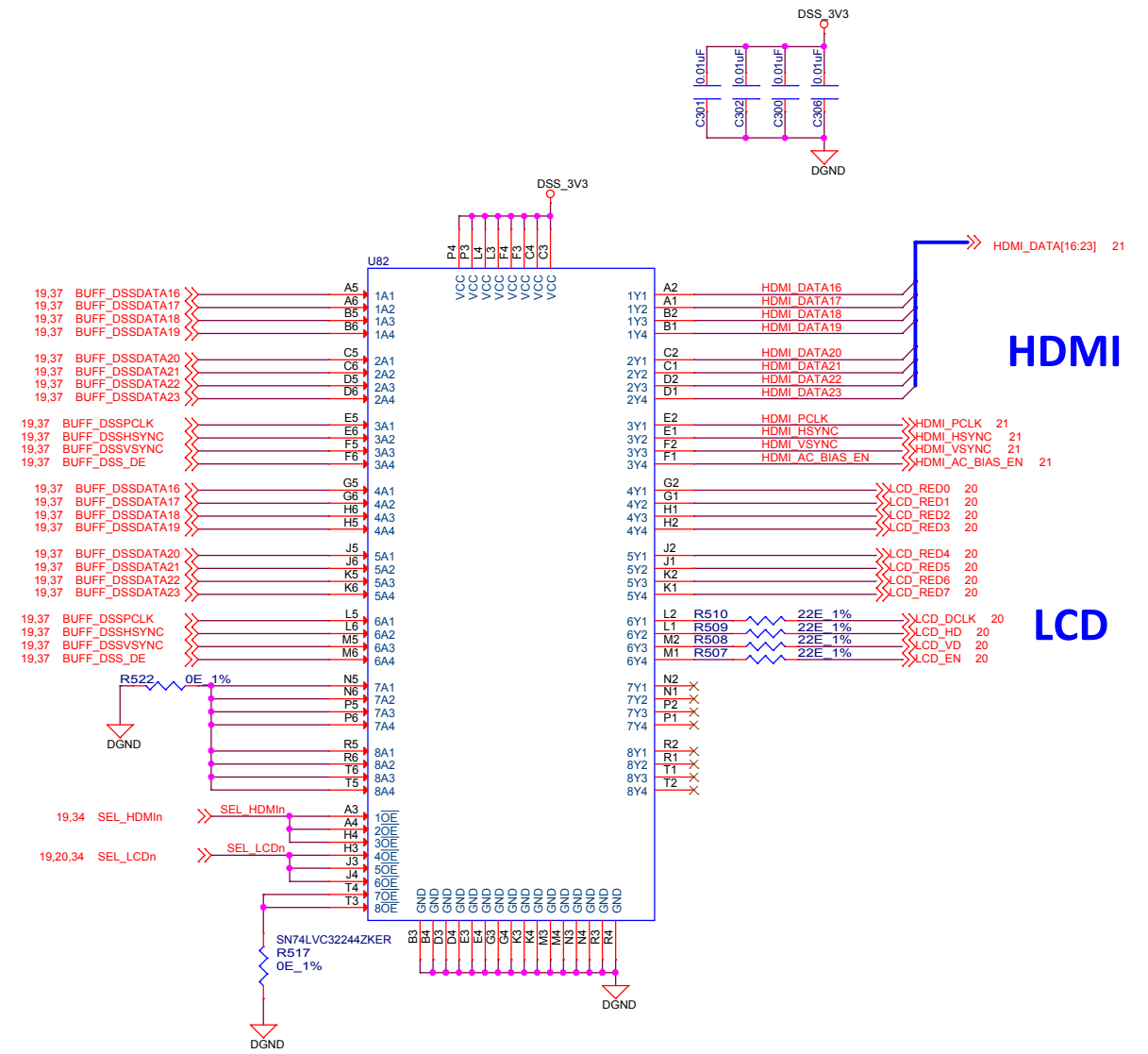
MICRO SD CARD



DSS BUFFER 1



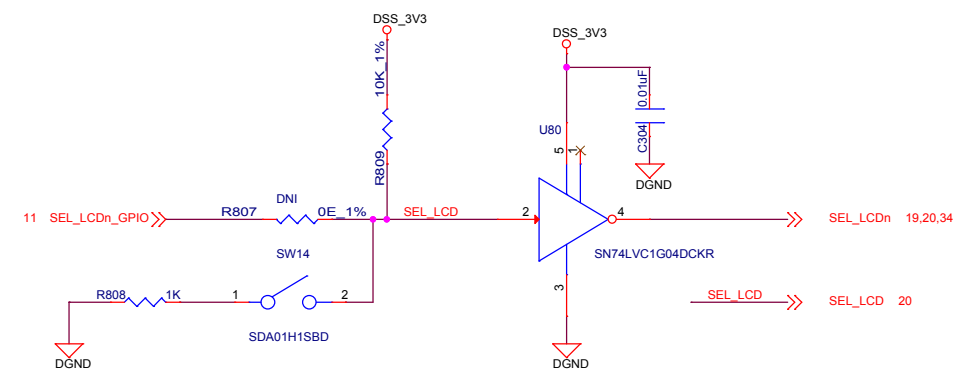
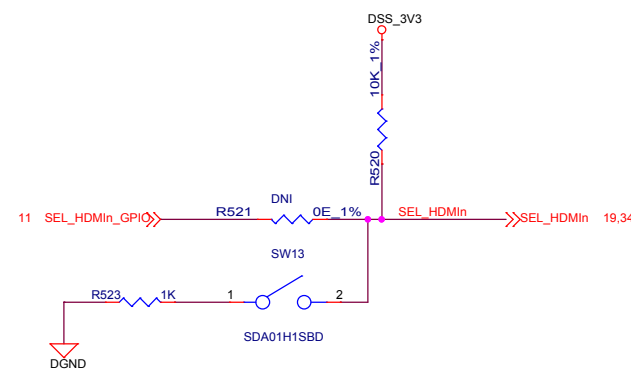
DSS BUFFER 2



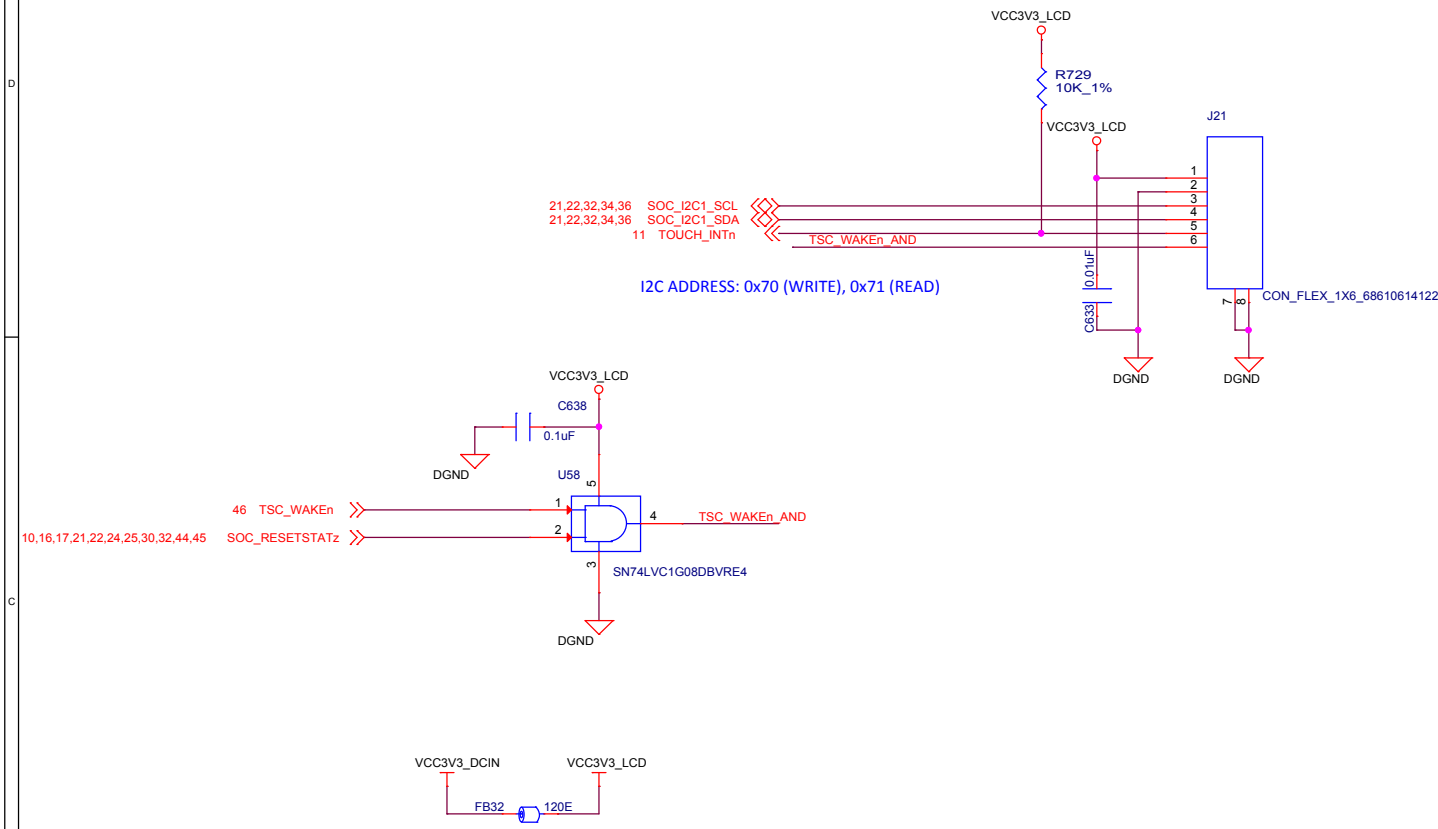
SELECTION LCD AND HDMI

HDMI/LCD SWITCH SELECTION

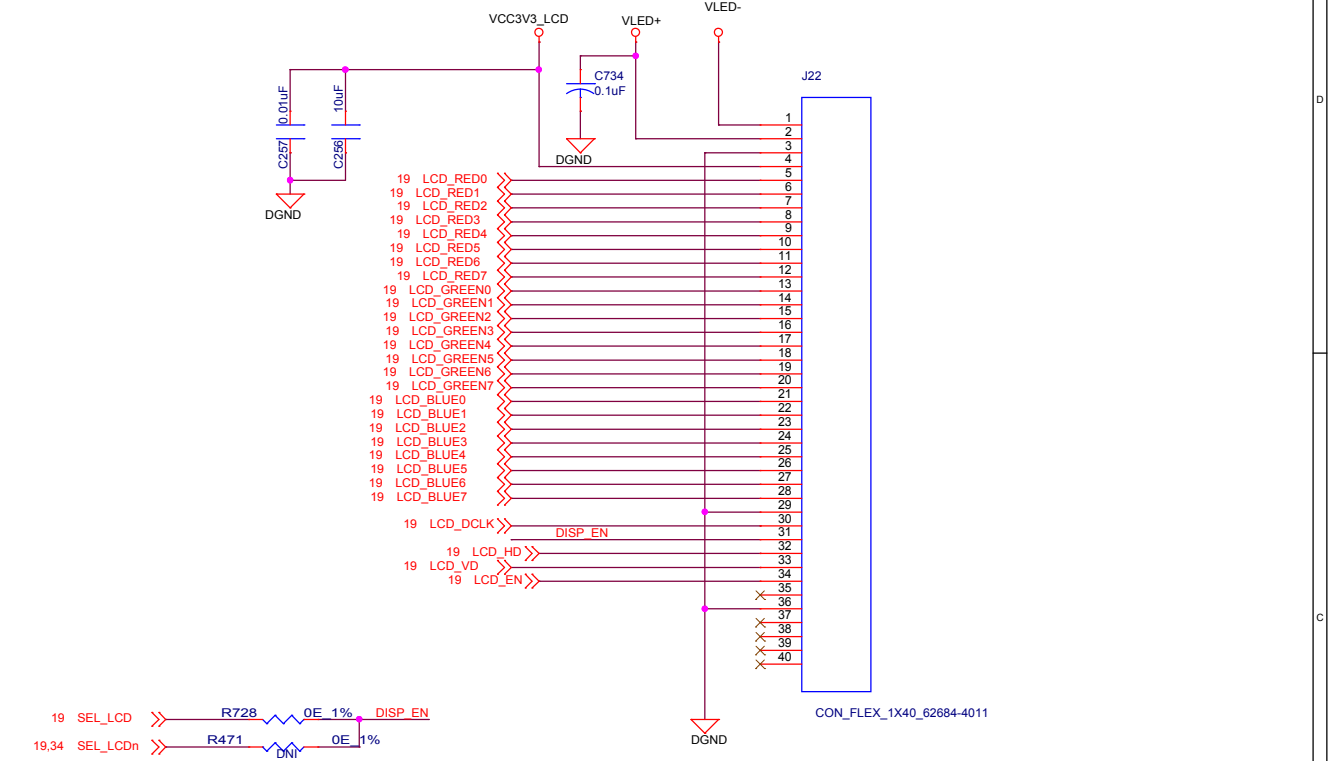
SW14	SW13	DEVICE
ON	ON	HDMI ON
OFF	OFF	LCD ON
OFF	ON	NOT VALID
ON	OFF	NOT VALID



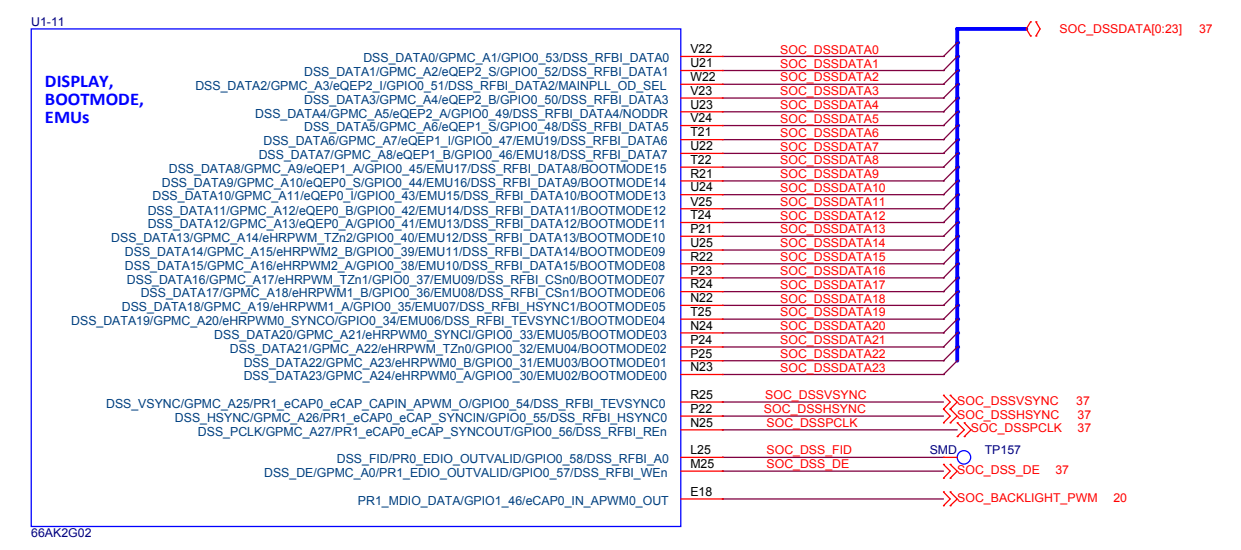
TOUCH SCREEN CONNECTOR



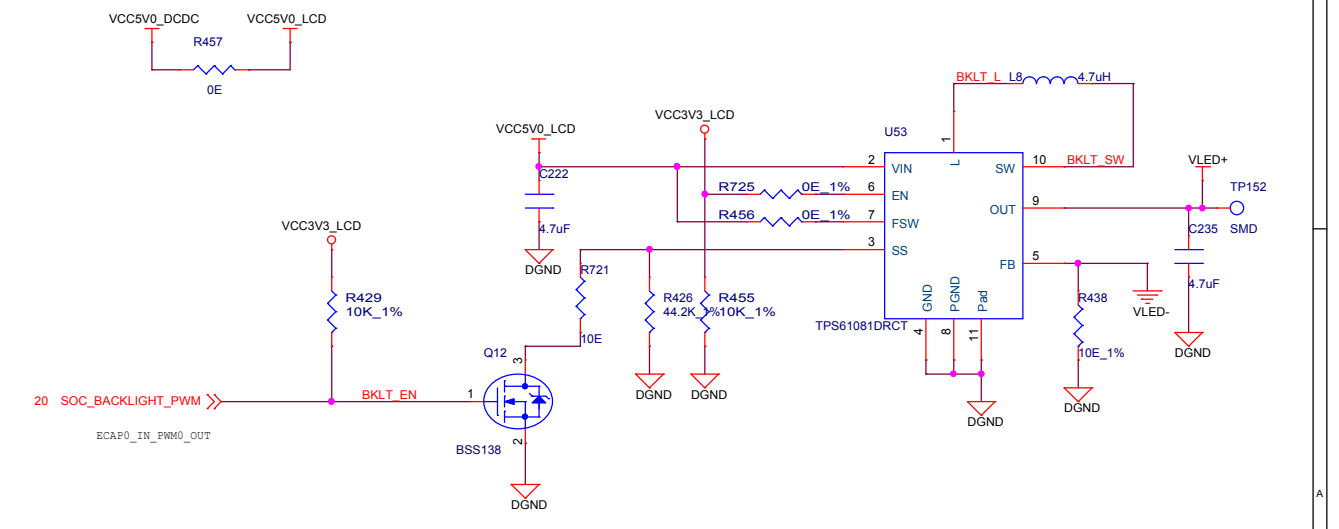
LCD CONNECTOR



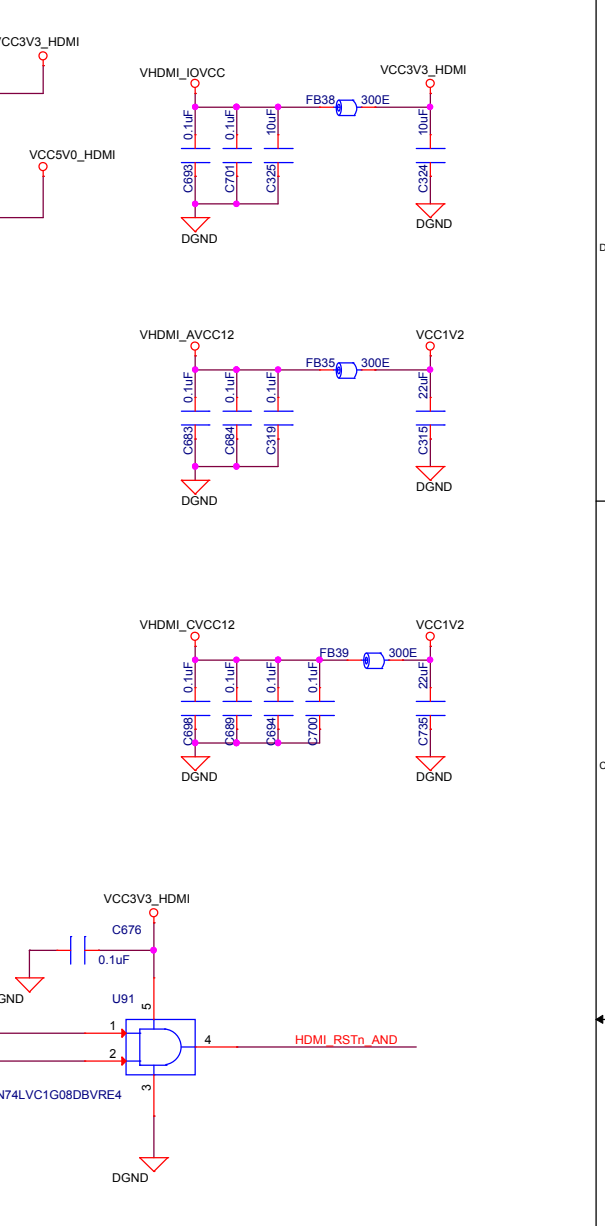
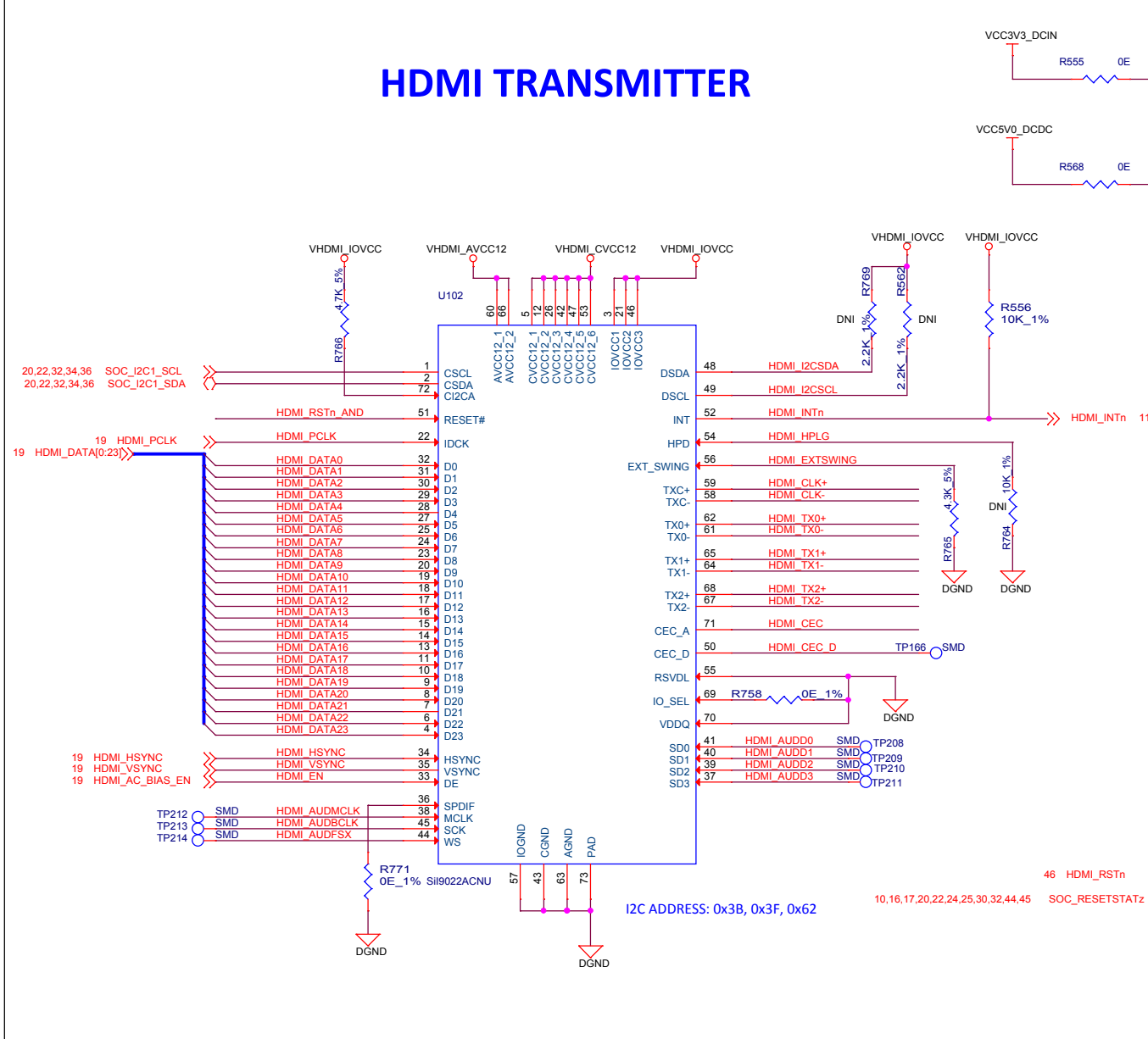
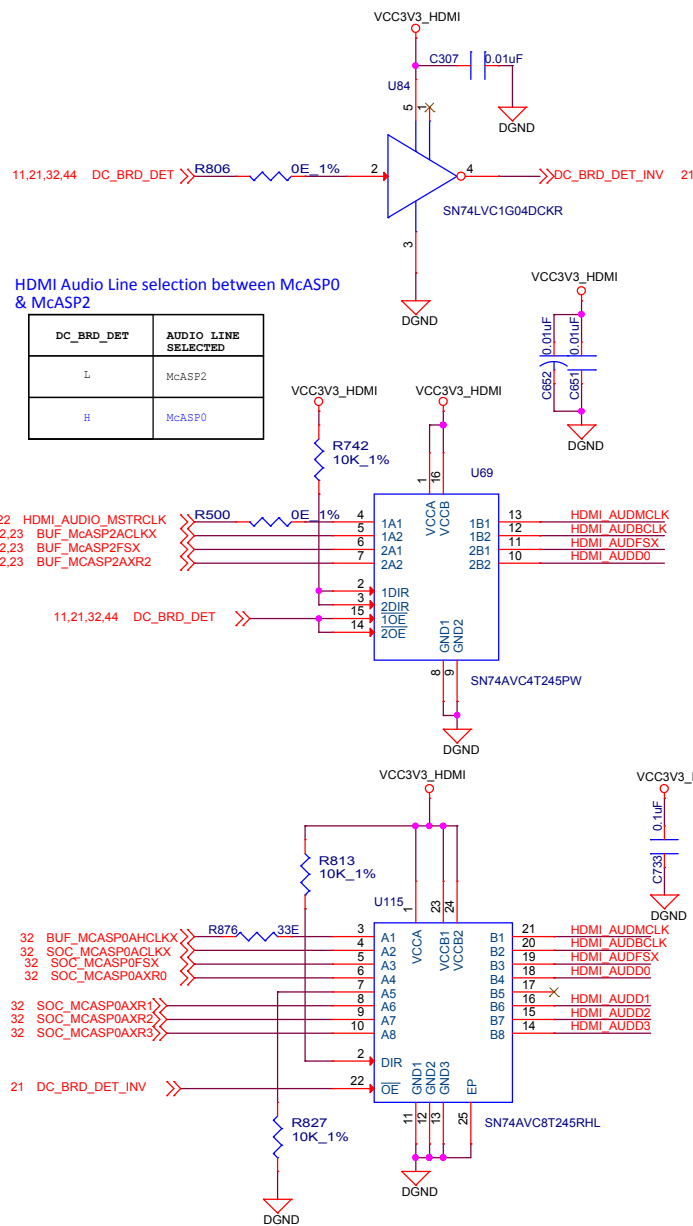
SOC DSS



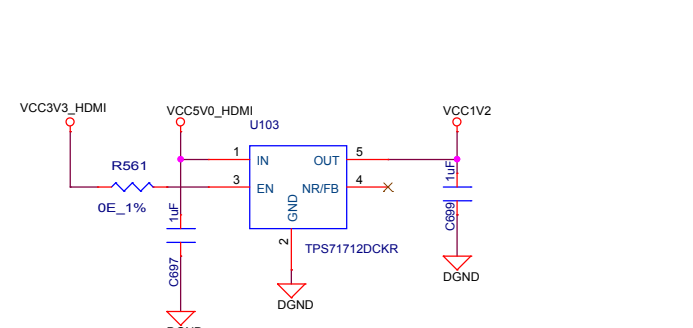
BACKLIGHT POWER



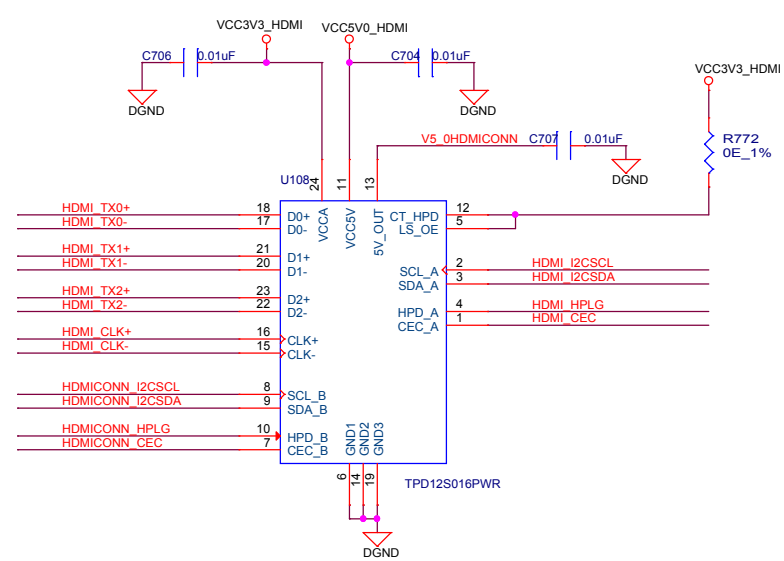
HDMI TRANSMITTER



HDMI 1.2V GENERATION

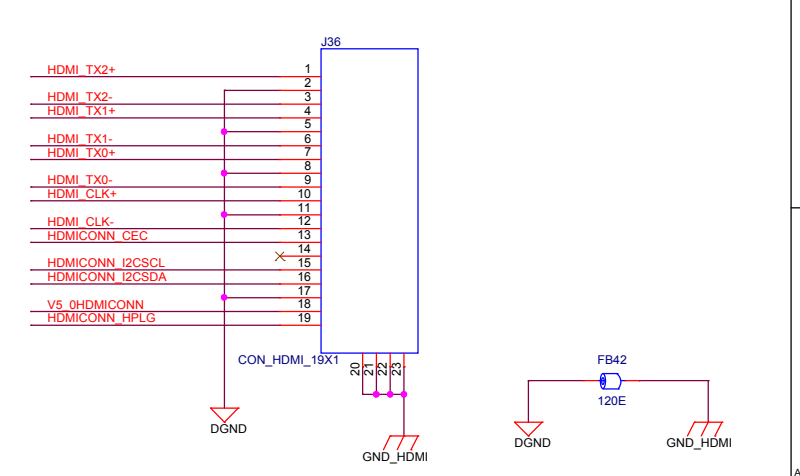


HDMI ESD DEVICE

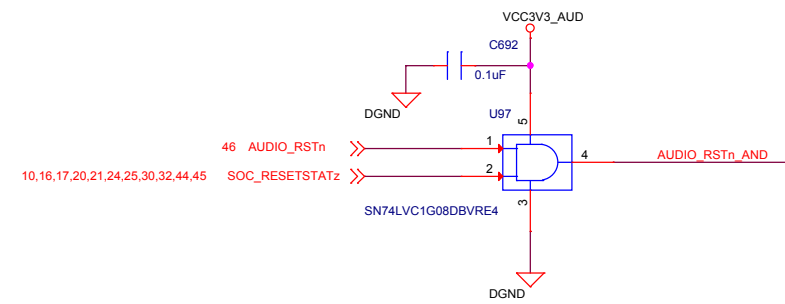


NOTE:
 TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR

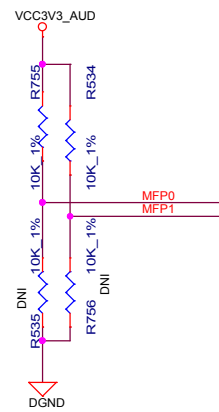


AUDIO CODEC RESET

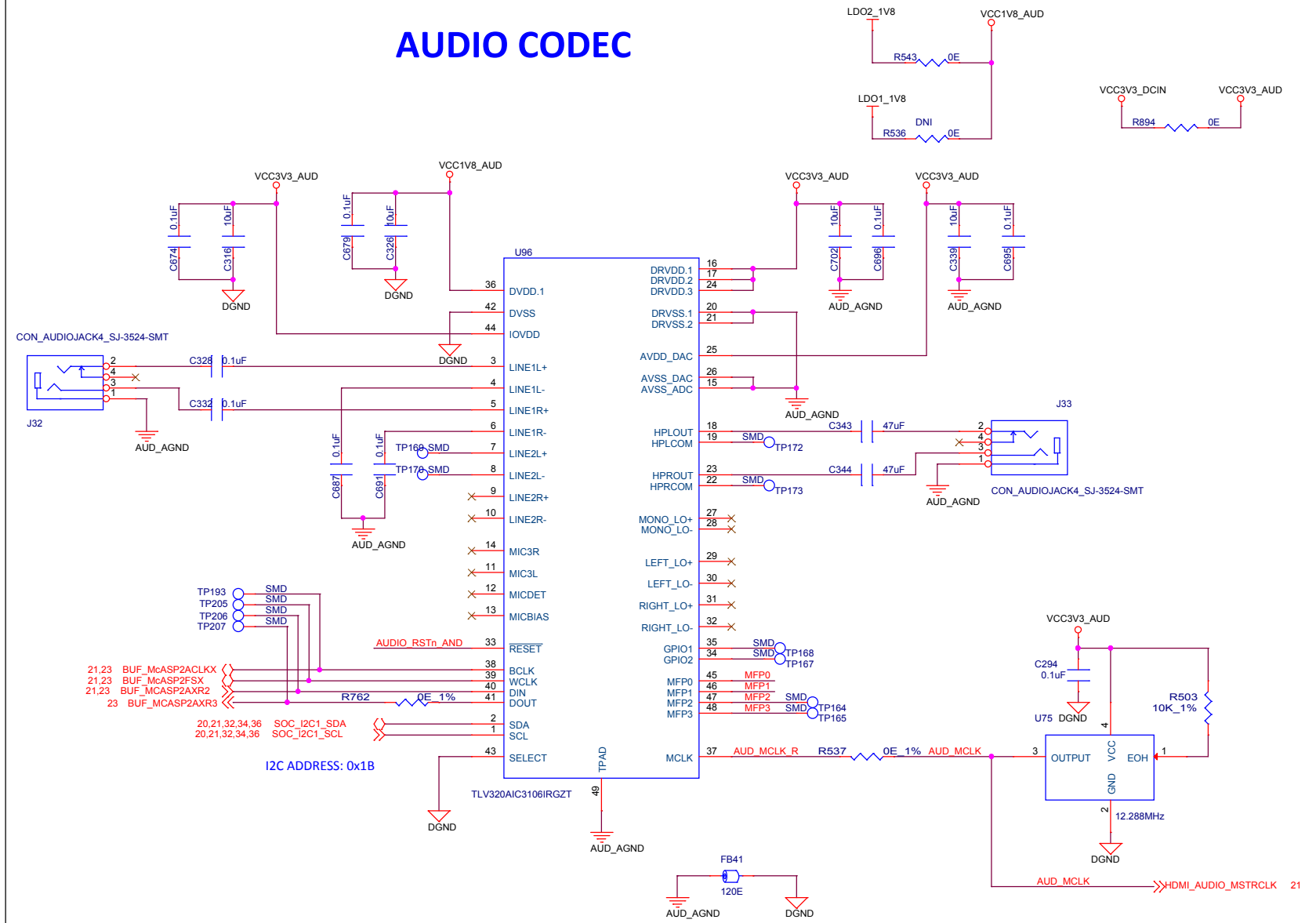


CODEC I2C ADDRESS SELECTION

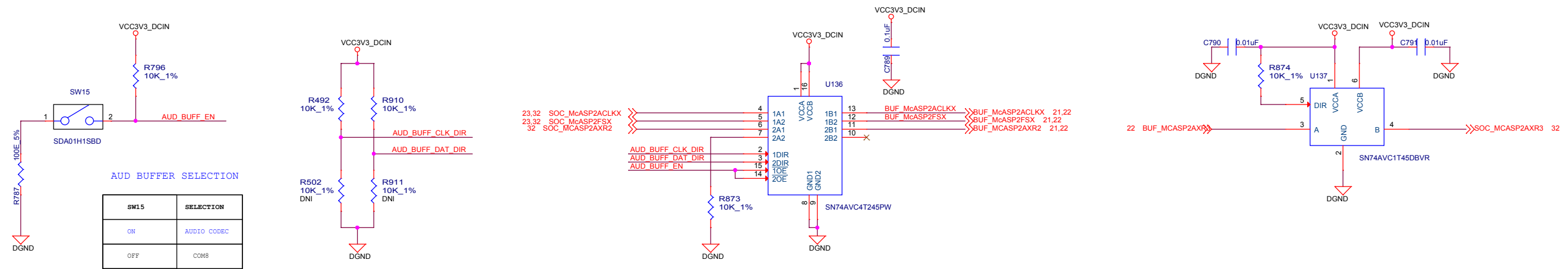
MFP0	MFP1	ADDRESS
L	L	1A
L	H	1B
H	L	1C
H	H	1D



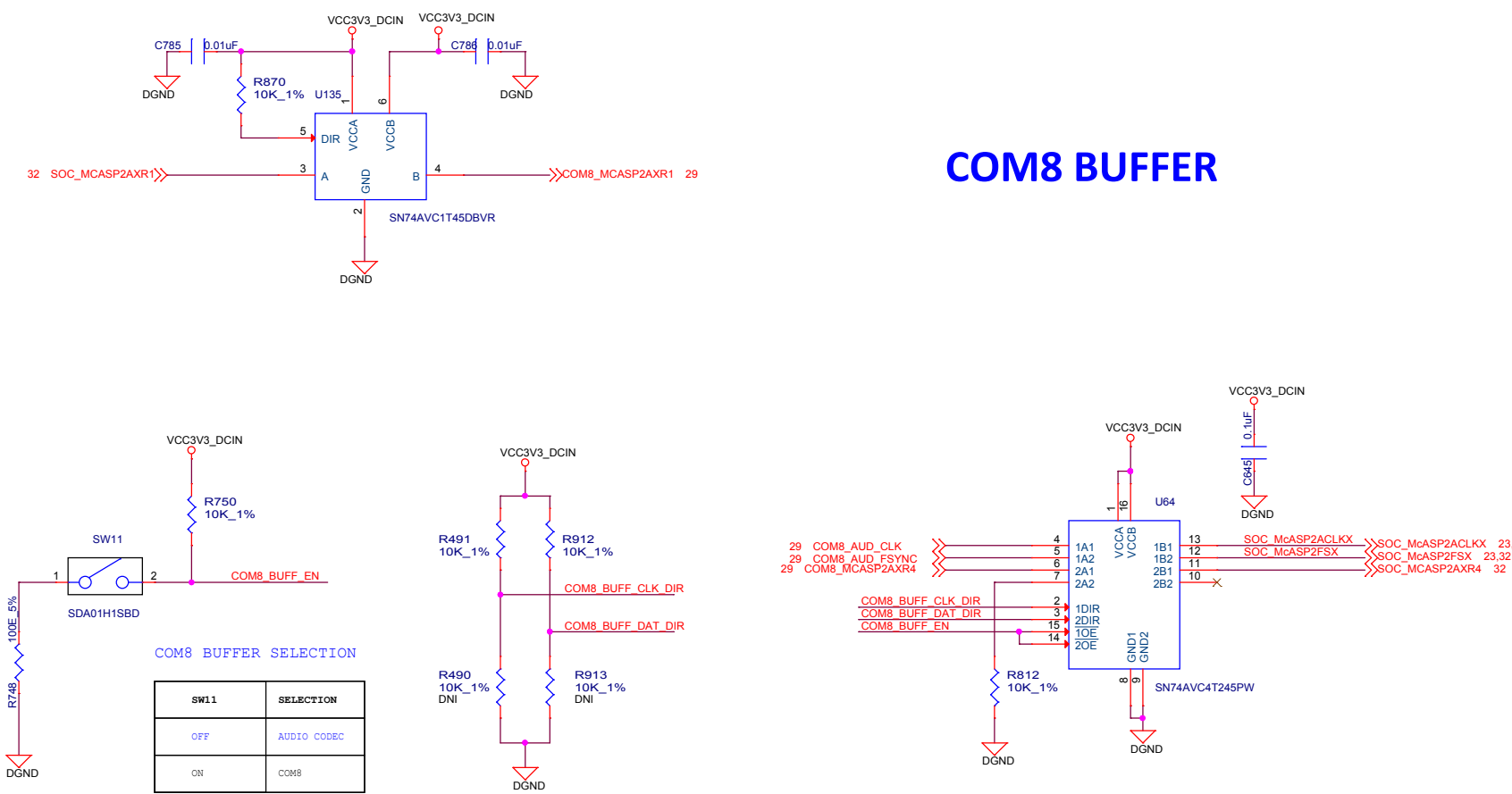
AUDIO CODEC



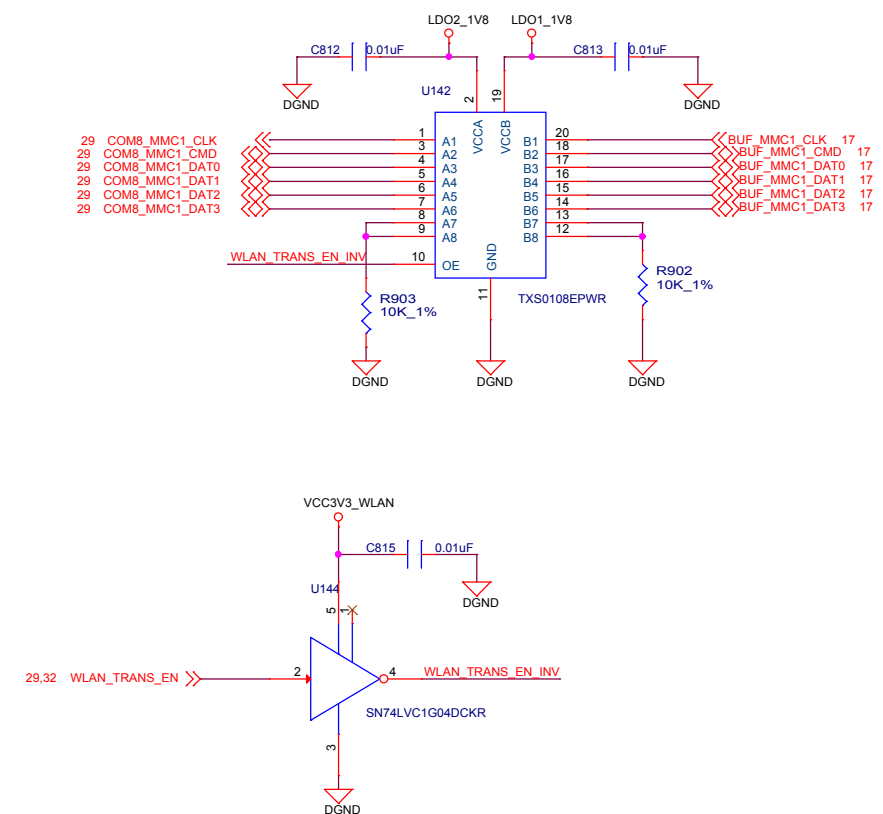
AUDIO BUFFER



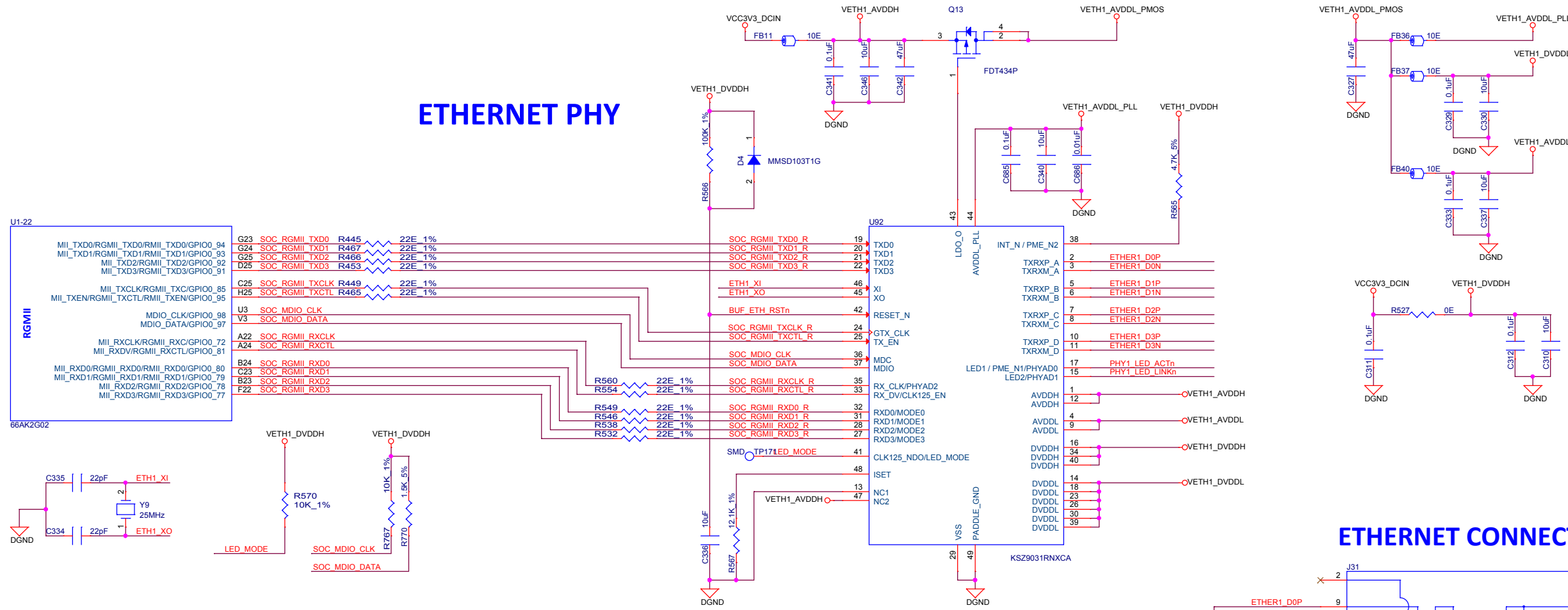
COM8 BUFFER



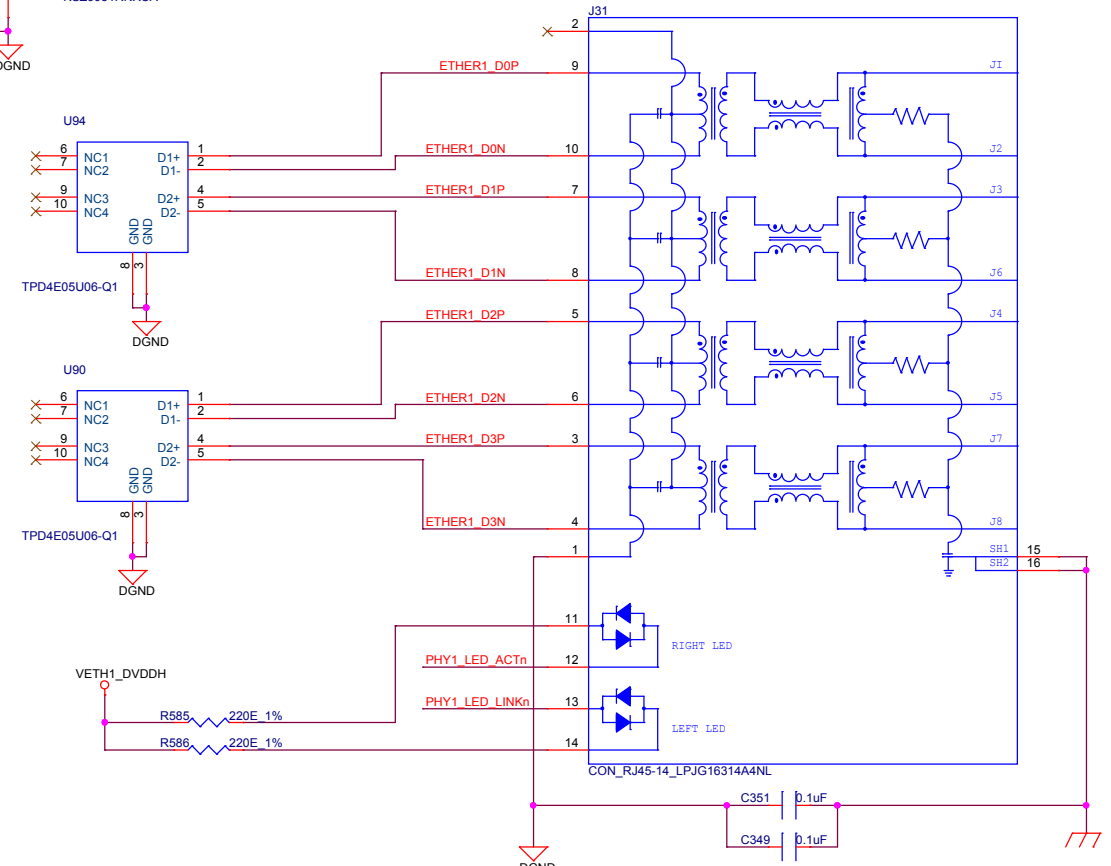
COM8 SDIO BUFFER



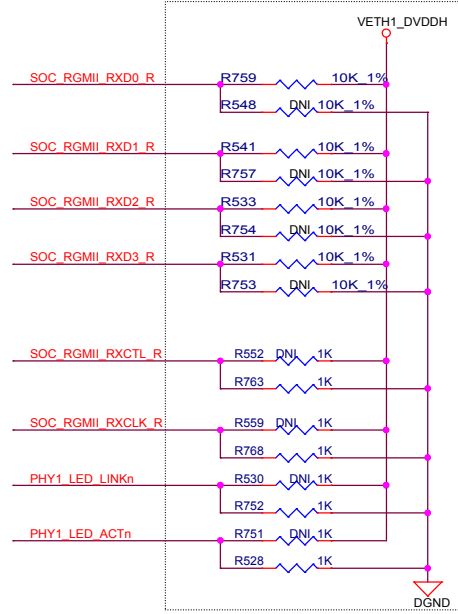
ETHERNET PHY



ETHERNET CONNECTOR

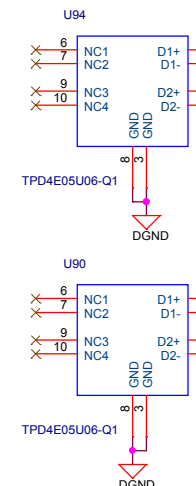


ETHERNET MODE CONFIGURATION

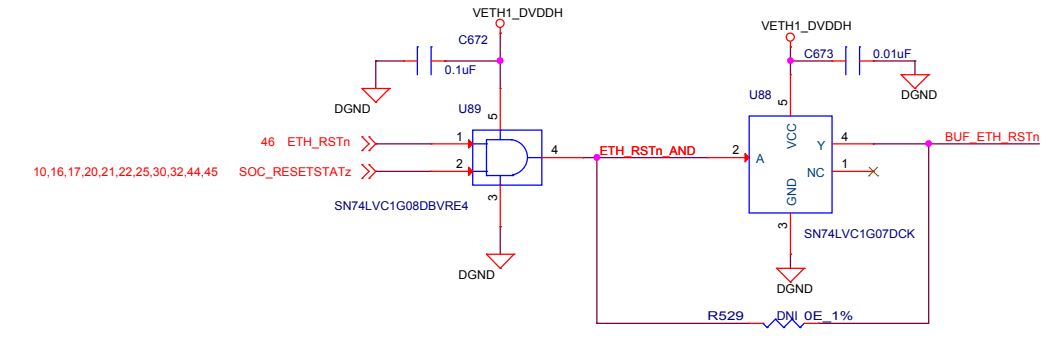


RXD[3:0]	MODE
0100	NAND TREE
0111	CHIP POWER DOWN
1100	RGMII MODE - ADVERTISE 1000 BASE-T FULL DUPLEX ONLY
1101	RGMII MODE- ADVERTISE 1000 BASE-T FULL & HALF DUPLEX ONLY
1110	RGMII MODE- ADVERTISE ALL CAPABILITIES (10/100/1000 SPEED HALF / FULL DUPLEX), EXCEPT 1000 BASE-T HALF DUPLEX
1111	RGMII MODE- ADVERTISE ALL CAPABILITIES (10/100/1000 SPEED HALF / FULL DUPLEX)

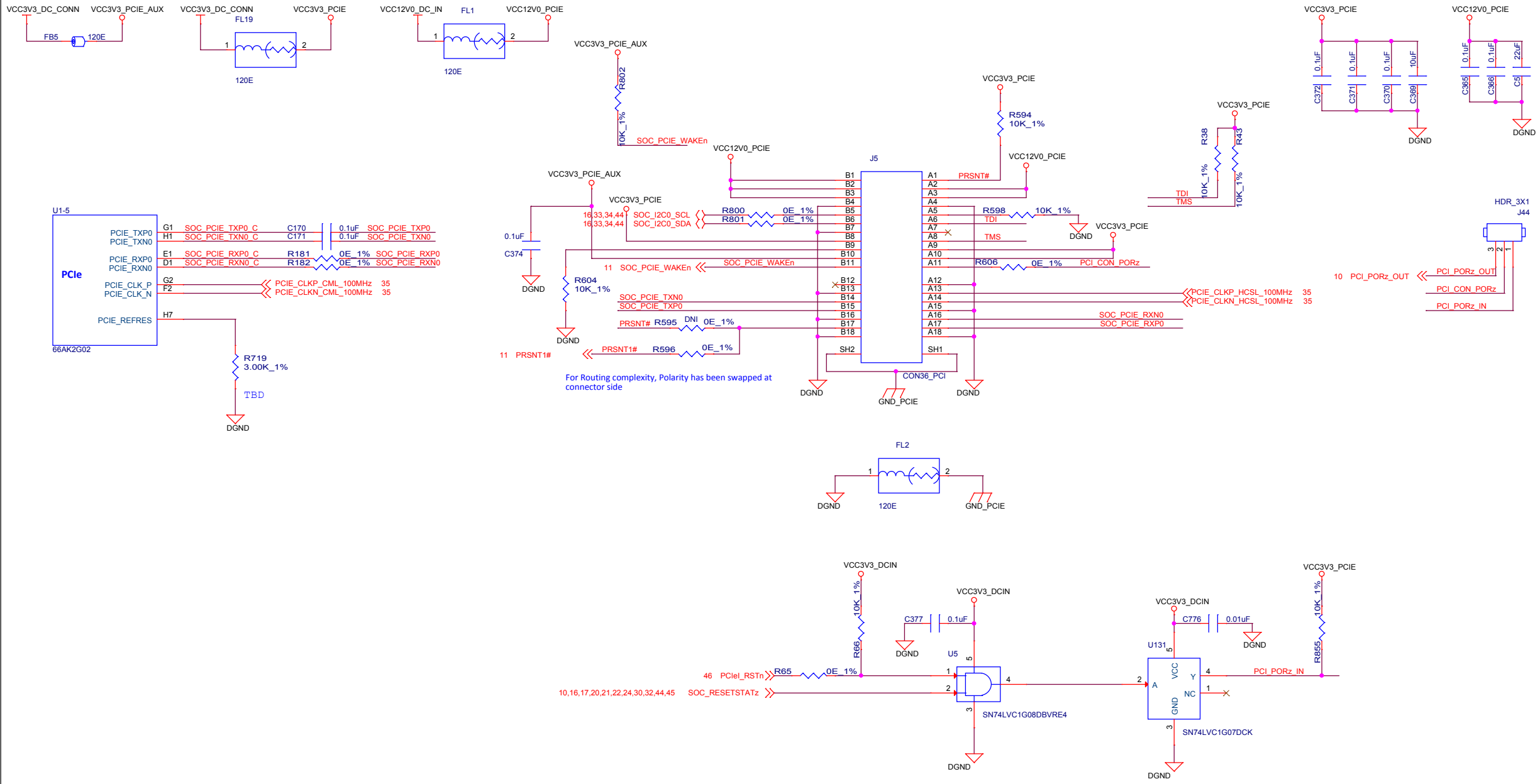
ETHERNET ESD DEVICES



ETHERNET RESET

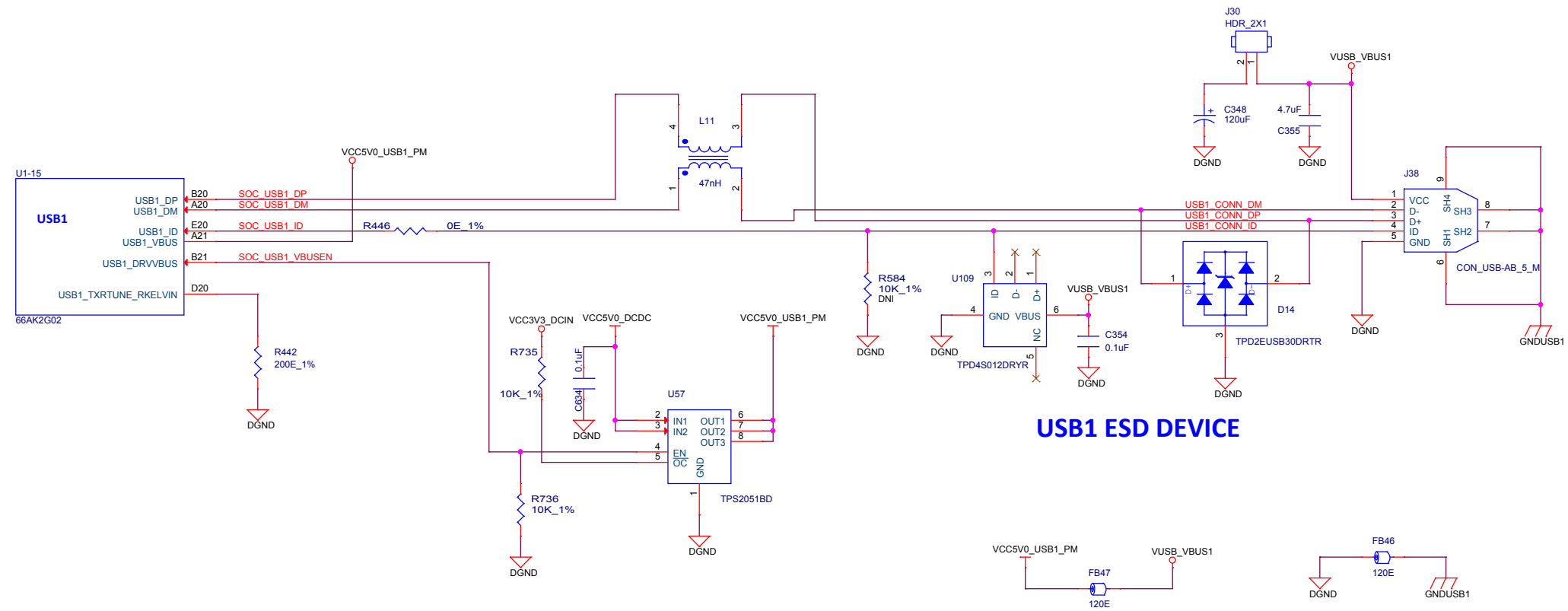


PCI EXPRESS x1 CONNECTOR

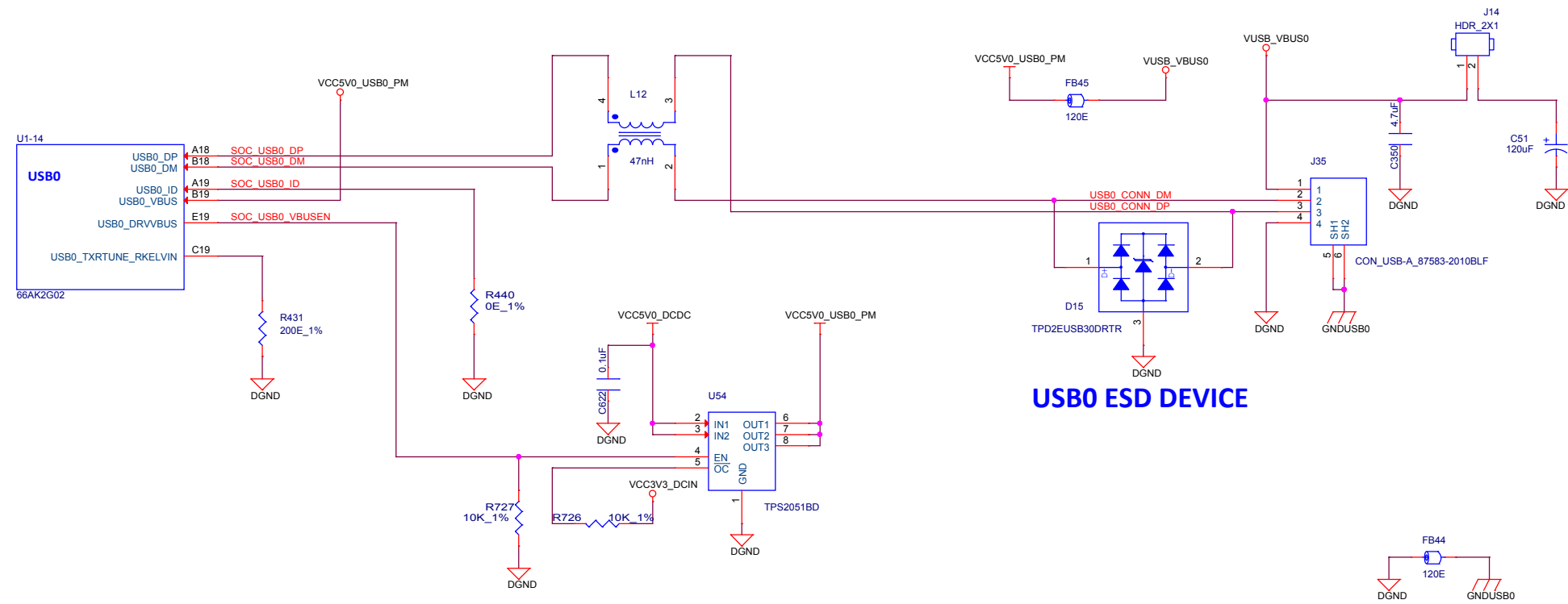


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title PCIe x1 CONNECTOR	
K2G EVM	 	Size Document Number	Rev
		C MS_TI_K2GEVM_SCH_REV D	D
Date:	Thursday, April 14, 2016	Sheet 25 of 50	

USB1 DUAL ROLE

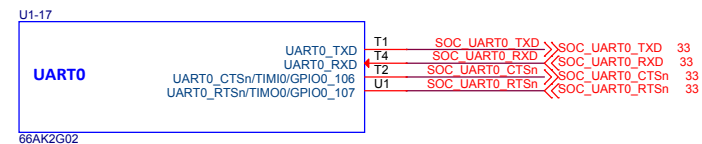


USB0 HOST

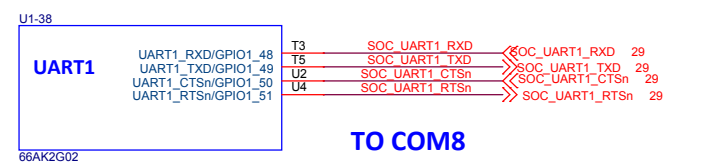


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title USB DUAL ROLE & HOST	
K2G EVM		Size	Rev
		Document Number	D
		MS_TI_K2GEVM_SCH_REVD	
		Date: Thursday, April 14, 2016	Sheet 26 of 50

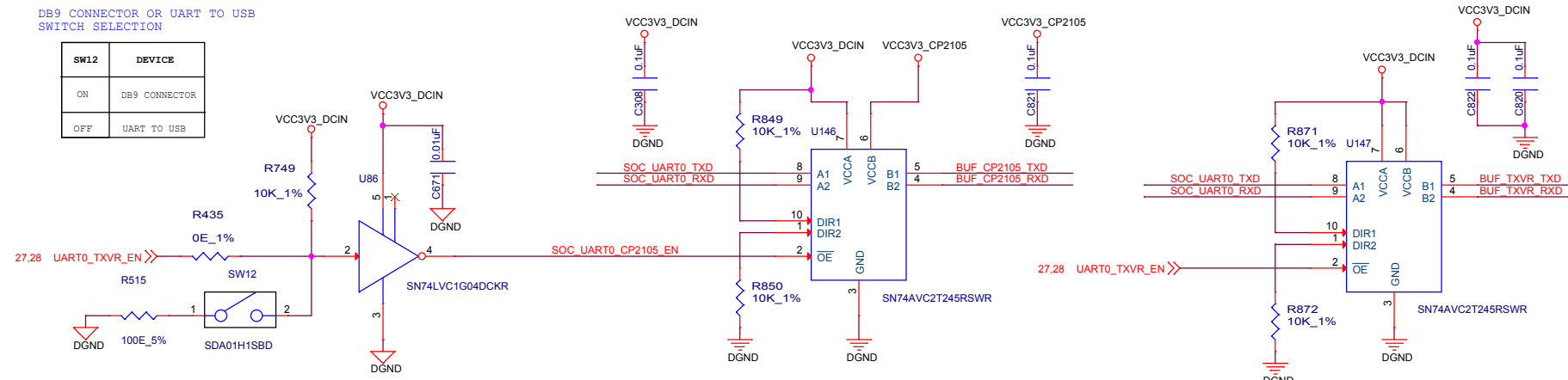
SoC UART0



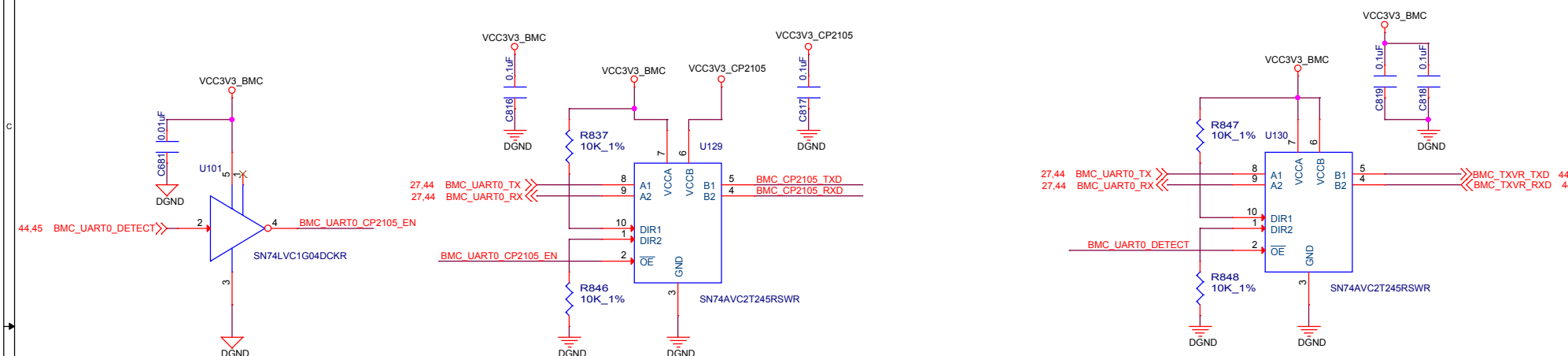
SoC UART1



SoC_UART0 MUX: CP2105 or DB9



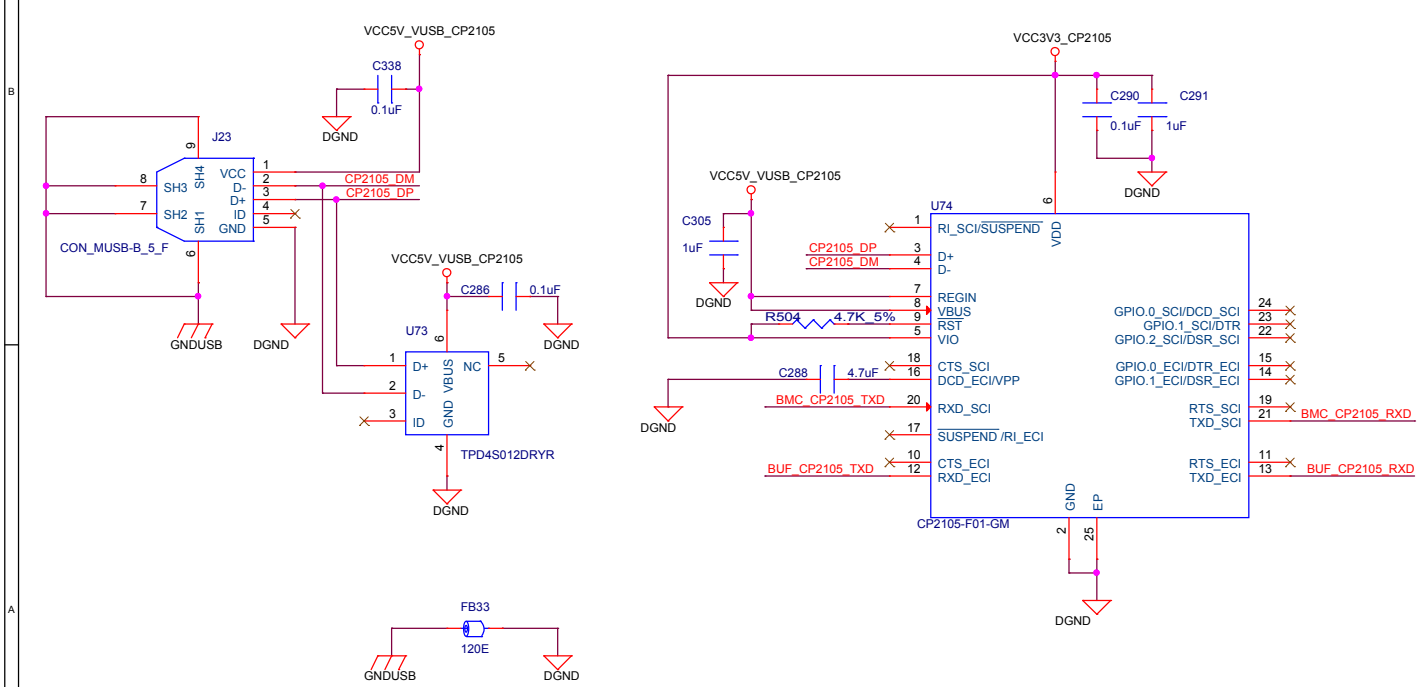
MUX BETWEEN BMC UART0 TO USB & 4 PIN HDR



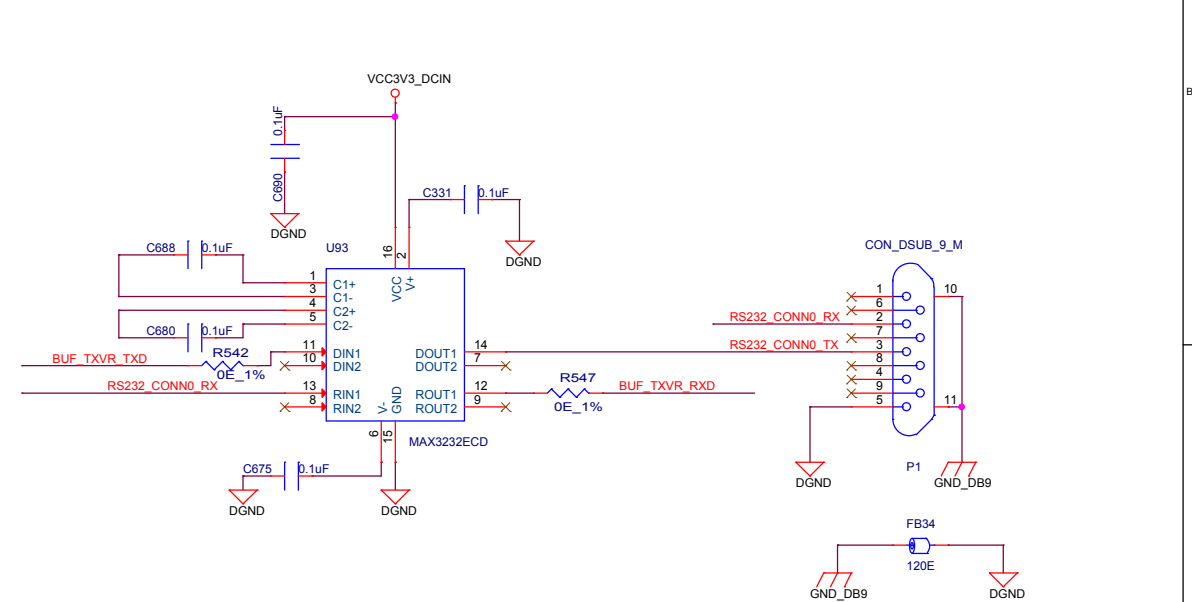
SoC_UART0 MUX SELECTION

SOC_UART0_CP2105_EN	SoC_UART0 Connected to
L	CP2105 (USB-to-UART)
H	UART TRANSCIEVER DB9 CONNECTOR

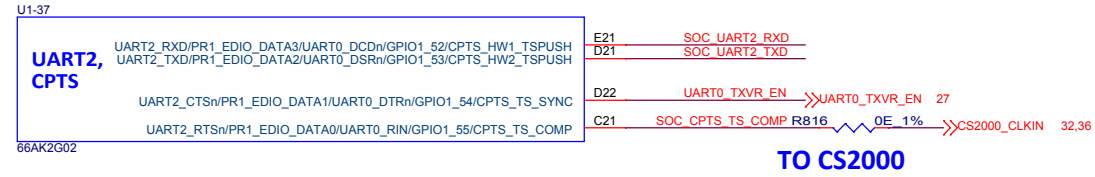
SoC UART0 & BMC CONSOLE OVER USB



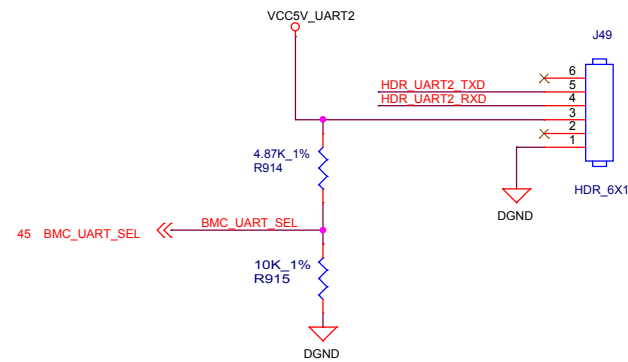
UART0 DB9 CON



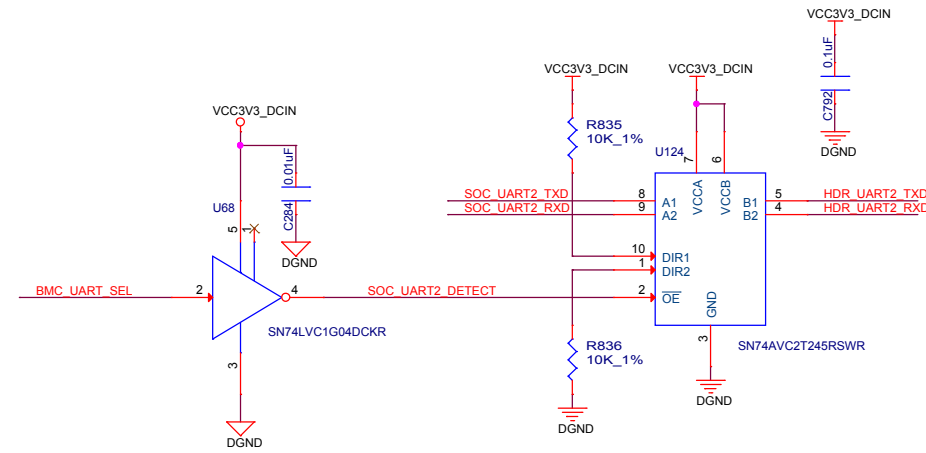
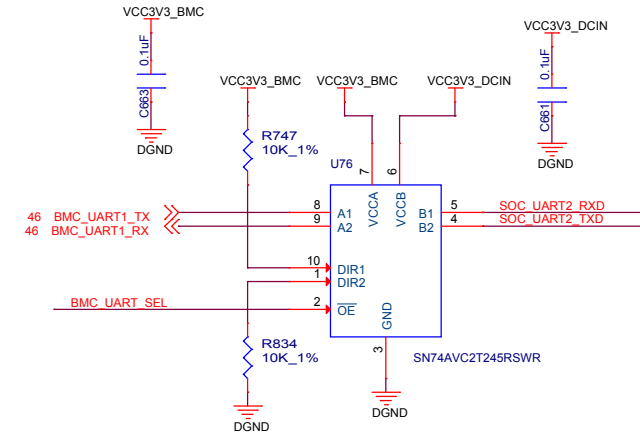
SoC UART2



UART2 HEADER



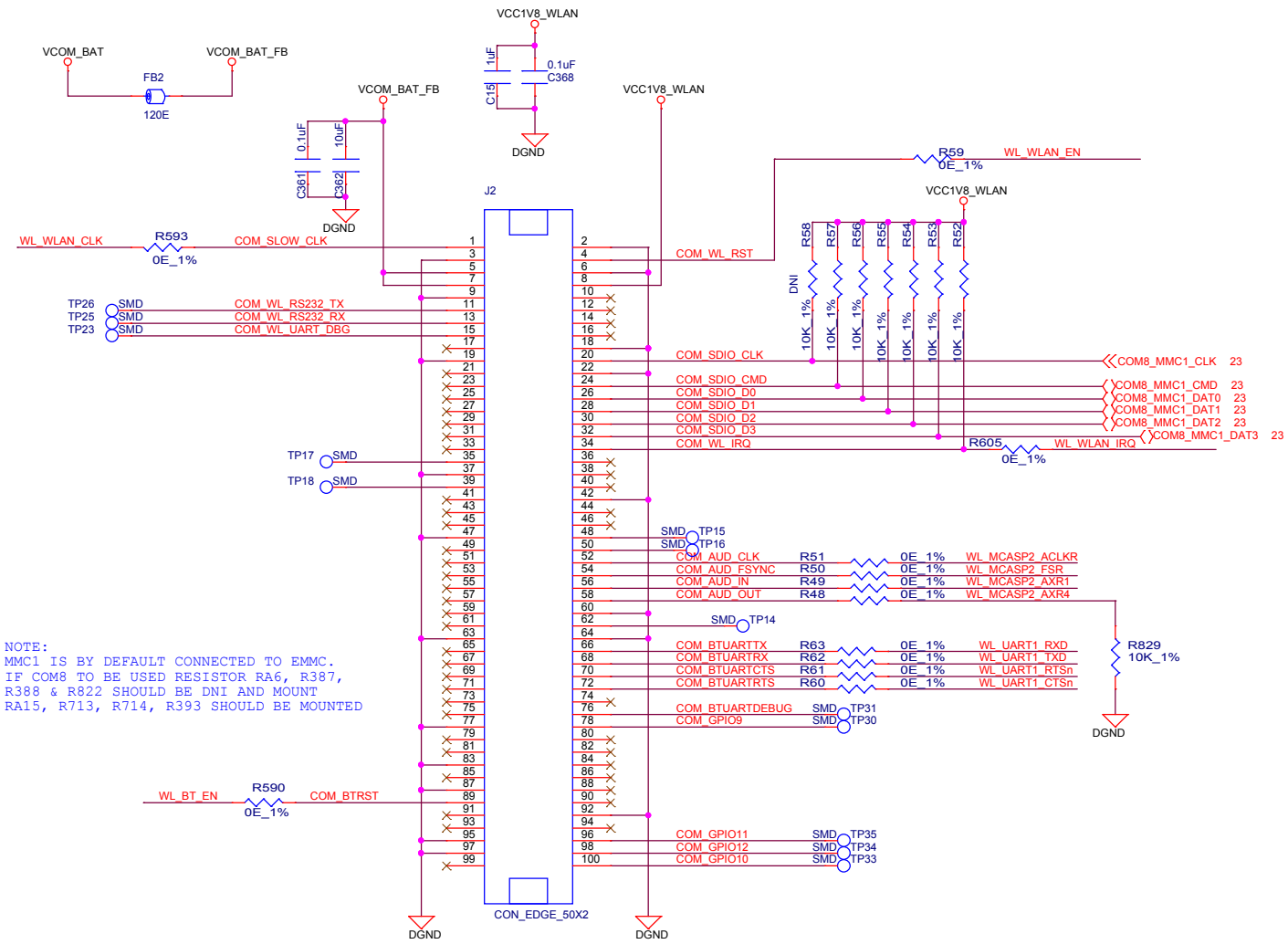
SoC UART2 MUX - BMC or UART2 Header



SoC_UART2 MUX SELECTION

BMC_UART_SEL	SoC_UART2 Connected to
L	BMC
H	UART2 HEADER (J49)

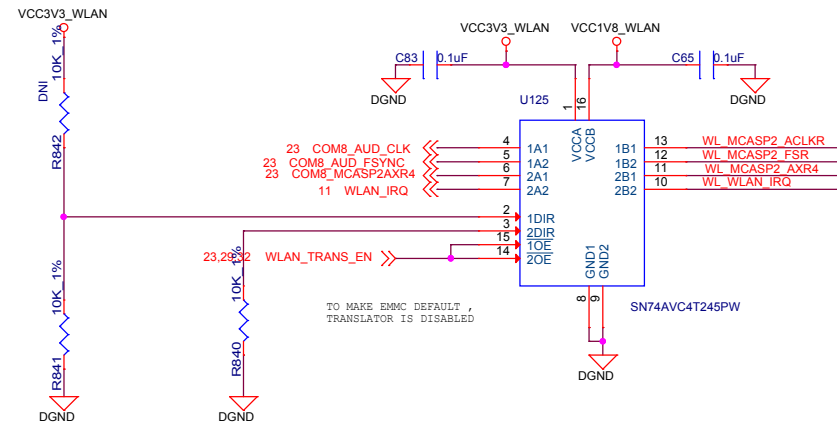
COM8 CONNECTOR



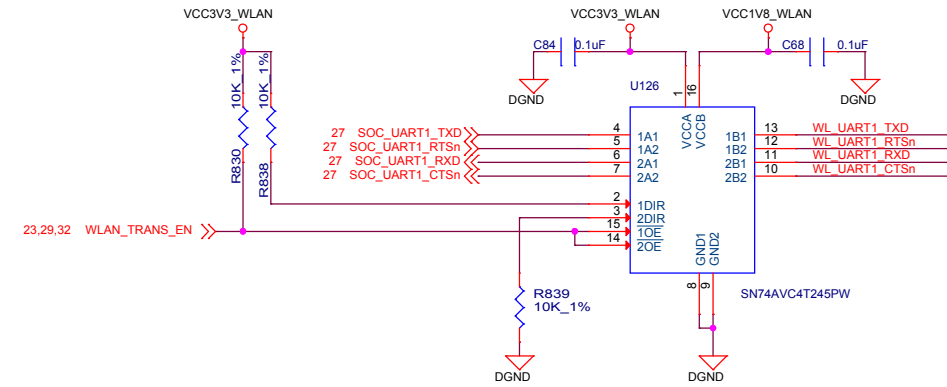
NOTE:
MMC1 IS BY DEFAULT CONNECTED TO EMMC.
IF COM8 TO BE USED RESISTOR RA6, R387,
R388 & R822 SHOULD BE DNI AND MOUNT
RA15, R713, R714, R393 SHOULD BE MOUNTED

CONNECTION ON COM8 IS FOLLOWED AS PER
AM437x GP EVM. THESE ARE GPIOs ARE NOT USED
IN AM437x GP EVM, SO WE PROVIDED AS TEST POINTS

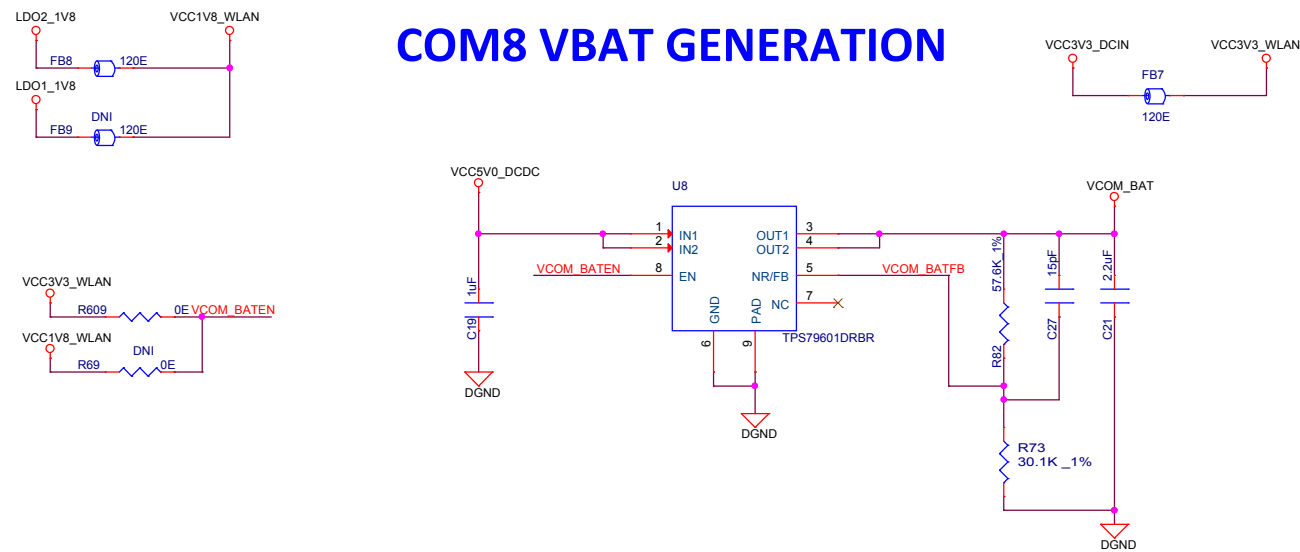
COM8 LEVEL TRANSLATOR1



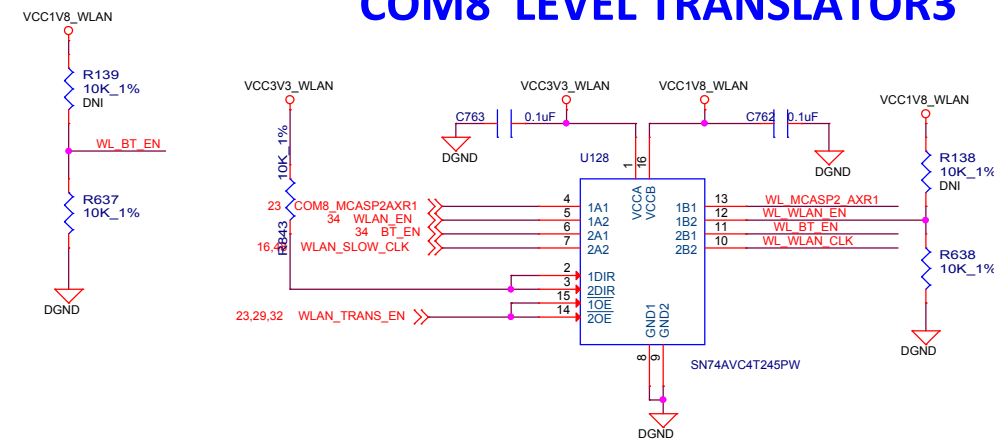
COM8 LEVEL TRANSLATOR2



COM8 VBAT GENERATION

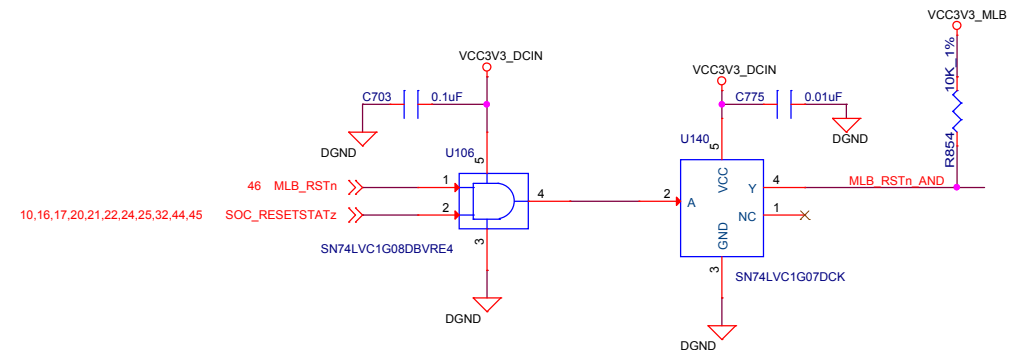
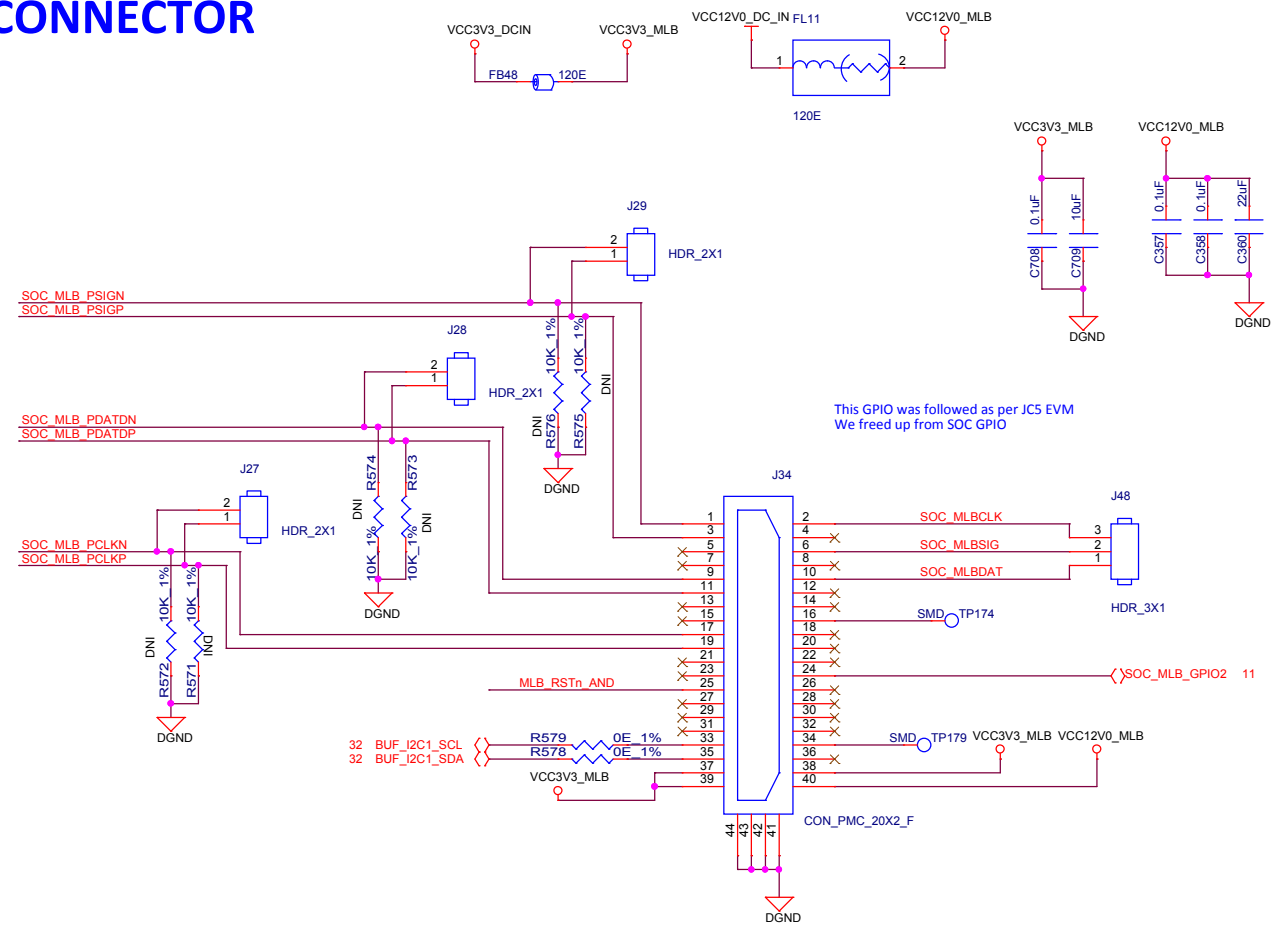
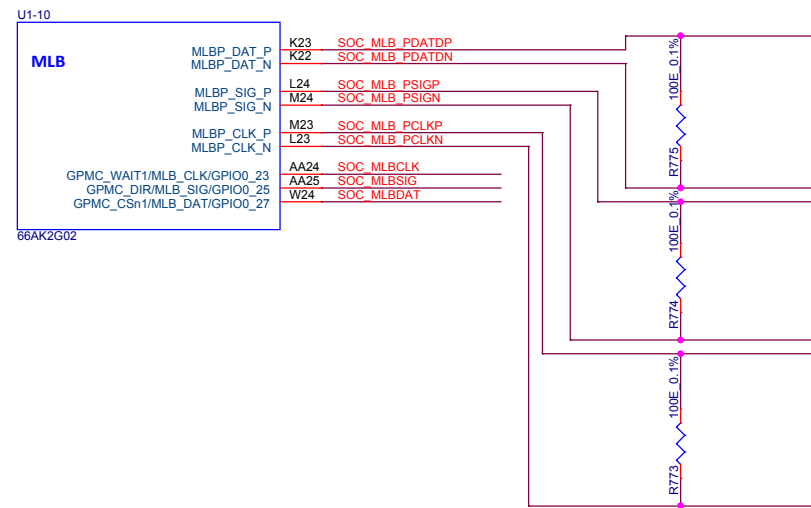


COM8 LEVEL TRANSLATOR3



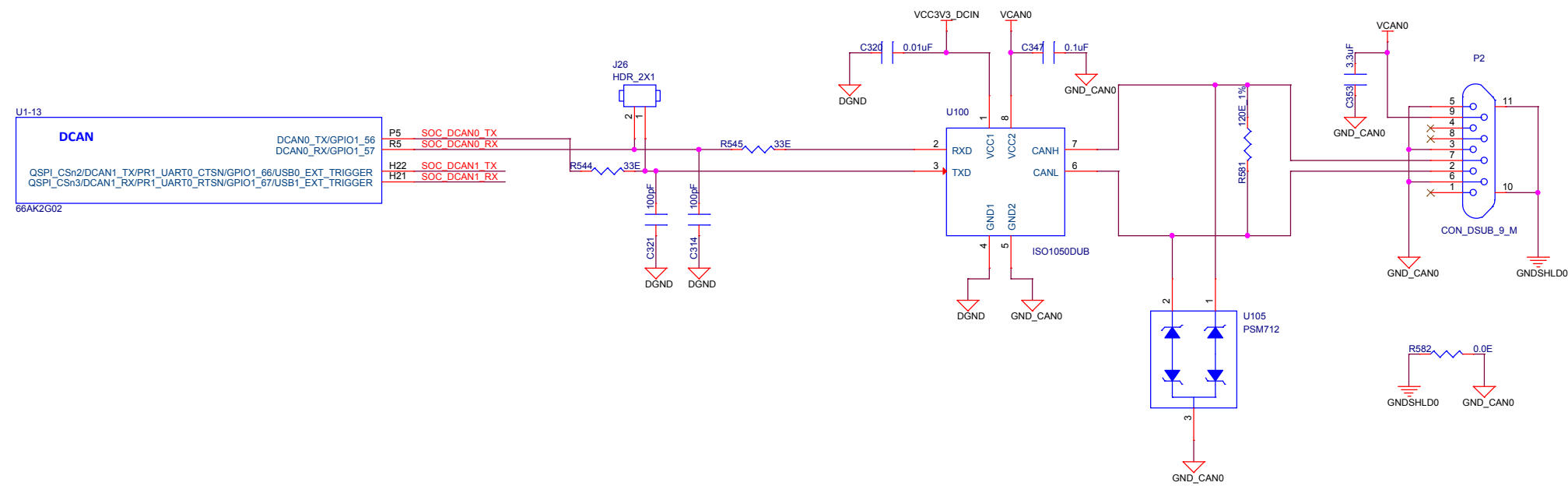
Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title COM8 CONNECTOR	
K2G EVM	 	Size Document Number	Rev
		C MS_TI_K2GEVM_SCH_REV D	D
		Date: Wednesday, April 13, 2016	Sheet 29 of 50

MLB CONNECTOR

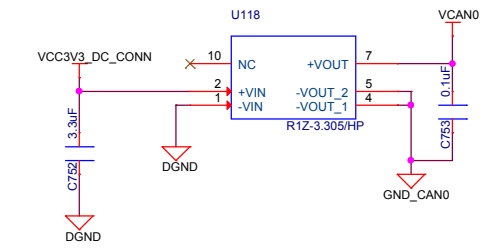


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title MLB CONNECTOR	
K2G EVM		Size C	Document Number MS_TI_K2GEVM_SCH_REV D
		Date: Thursday, April 14, 2016	Rev D
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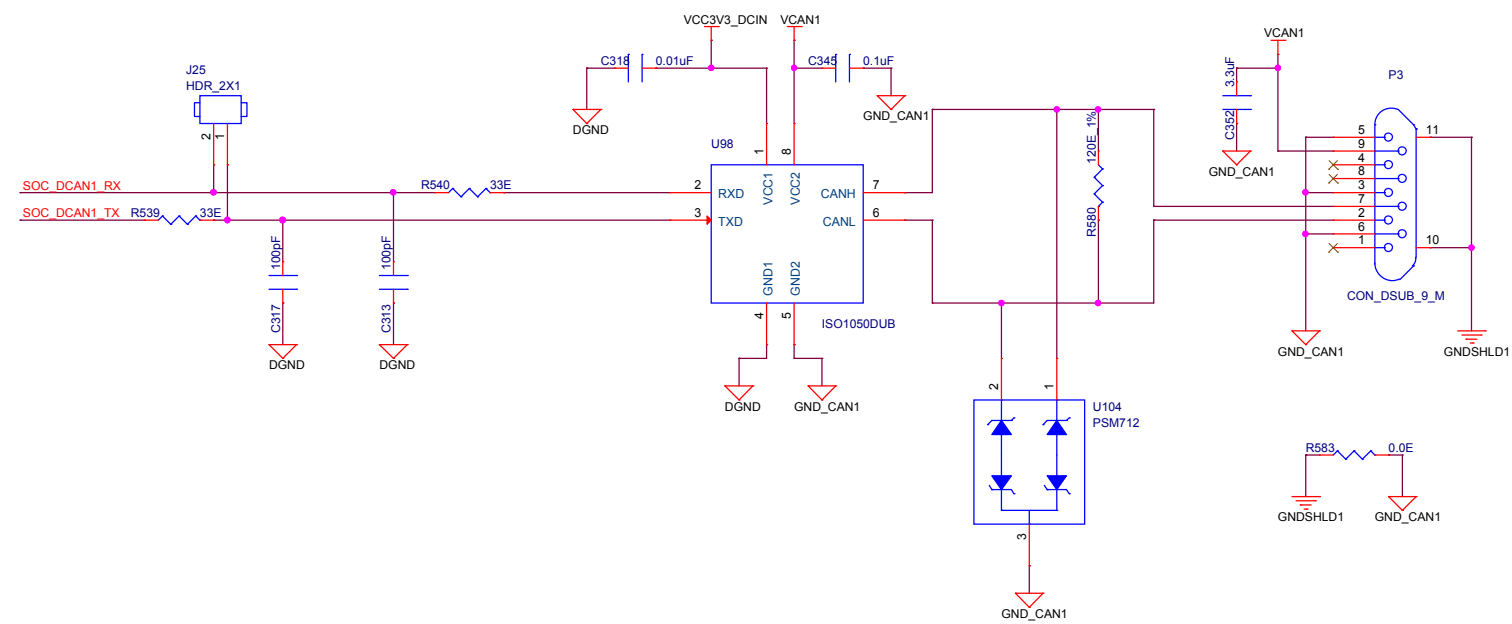
DCAN0



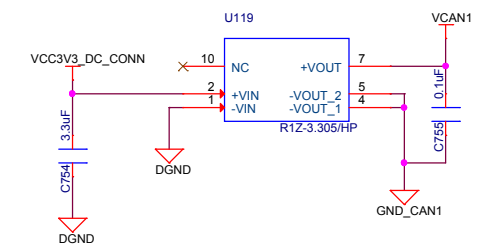
DCAN0 POWER



DCAN1

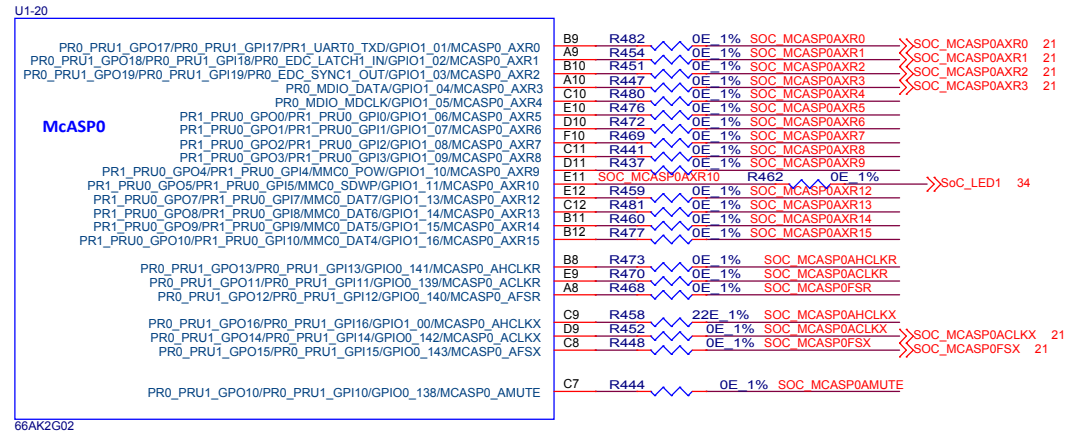


DCAN1 POWER

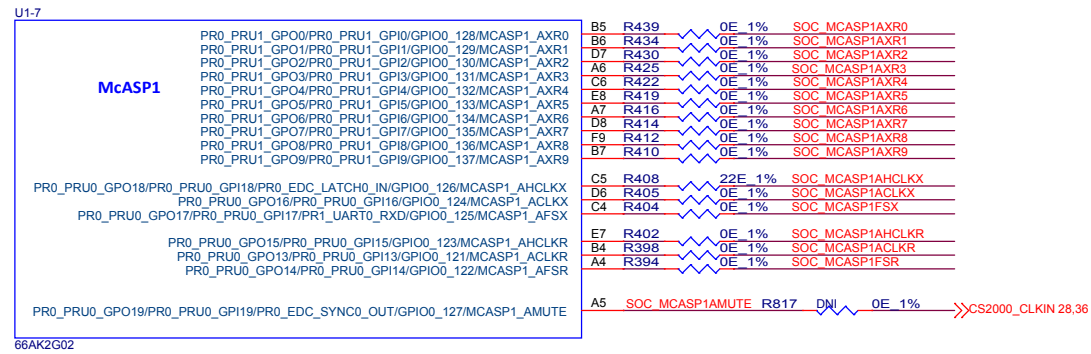


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title DCAN CONNECTOR	
K2G EVM	 	Size Document Number	Rev
		C MS_TI_K2GEVM_SCH_REVD	D
Date: Thursday, April 14, 2016	Sheet 31 of 50		

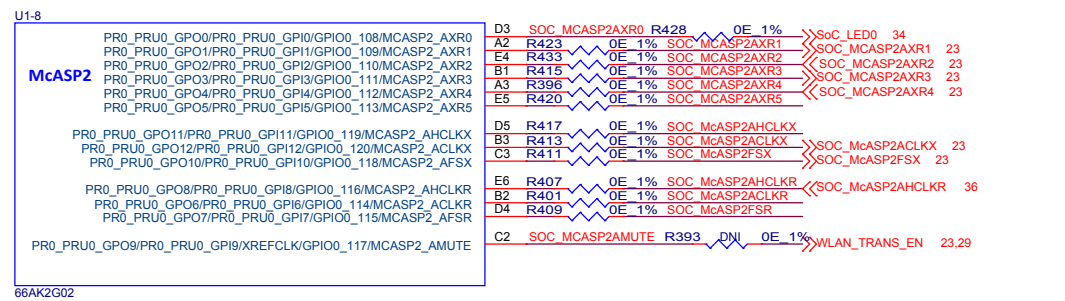
SOC MCASP



SOC_MCASP0AXR10 R820 DNI OE 1% SOC_MCASP0AXR10_R
SOC_MCASP0AHCLKX SOC_MCASP0AHCLKX

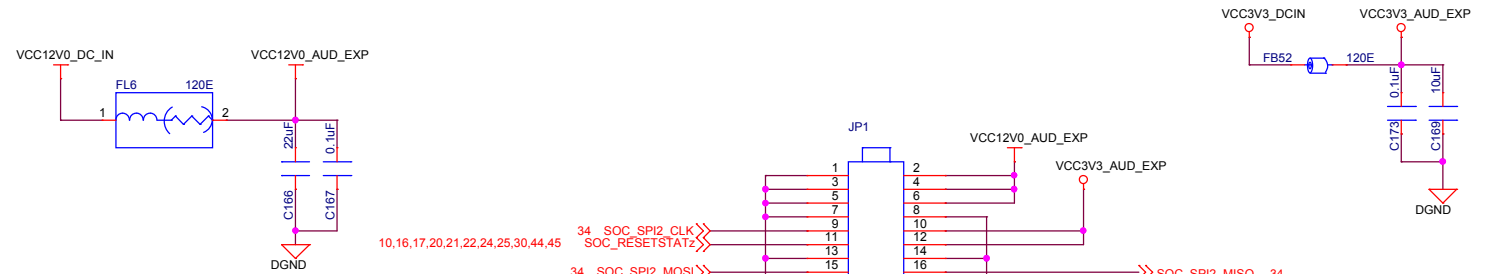


SOC_MCASP1AMUTE R823 OE 1% SOC_MCASP1AMUTE_R

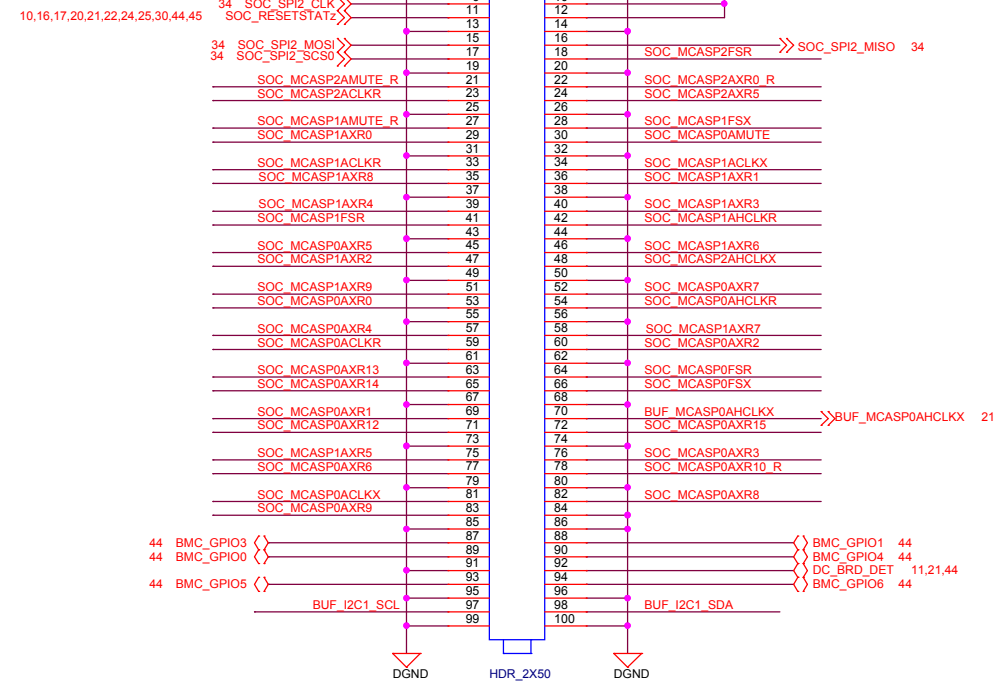


SOC_MCASP2AXR0 R821 DNI OE 1% SOC_MCASP2AXR0_R
SOC_MCASP2AMUTE R822 DNI OE 1% SOC_MCASP2AMUTE_R

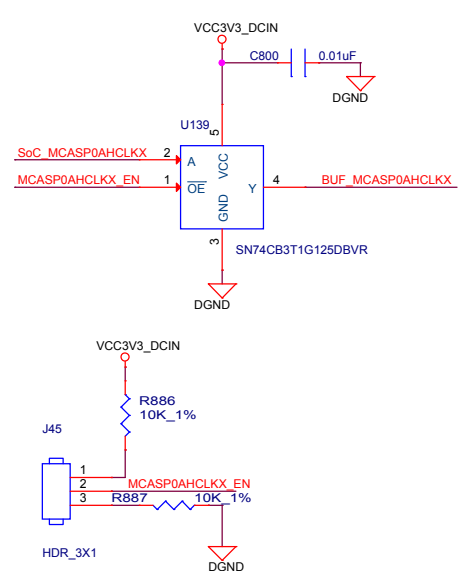
AUDIO EXP CONNECTOR



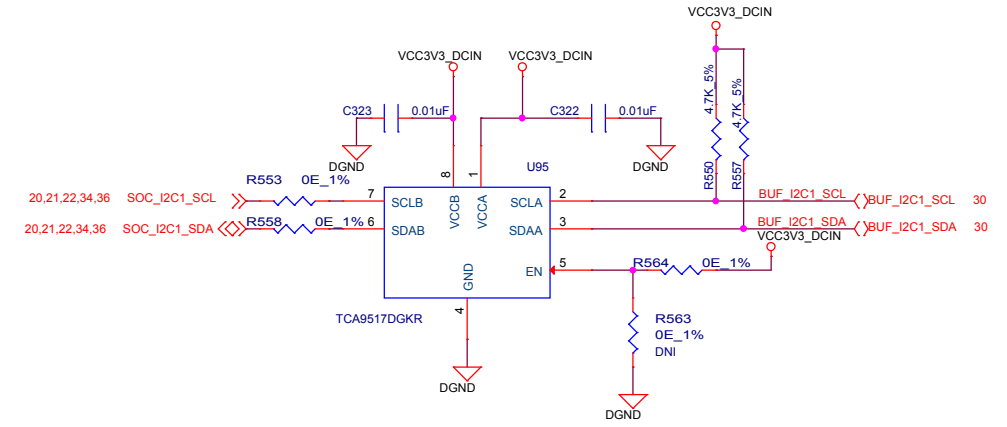
SOC SIGNAL	GPIOs ON AUDIO CARD
SOC_MCASP0AXR8/GPIO1_09	DIR_RST#
SOC_MCASP0AXR9/GPIO1_10	PCMI690_RST#
SOC_McASP0_AMUTE	DAC0_AMUTEI#, DAC1_AMUTEI#
SOC_MCASP1AXR4/GPIO0_132	McASP_CLK_SEL
SOC_MCASP1AXR6/GPIO0_134	DIR_AUDIO#
SOC_MCASP1AXR7/GPIO0_135	DIR_EMPH
SOC_MCASP1AXR8/GPIO0_136	DIR_ERROR
SOC_MCASP1AXR5/GPIO0_133	DIR_CLKST
SOC_MCASP1ACLKX/GPIO0_124	DIR_FSOUT0
SOC_MCASP1FSX / GPIO0_125	DIR_FSOUT1
SOC_SPI2_MOSI / GPIO0_105	I2SHDR_GPIO0
SOC_SPI2_MISO / GPIO0_104	I2SHDR_GPIO1



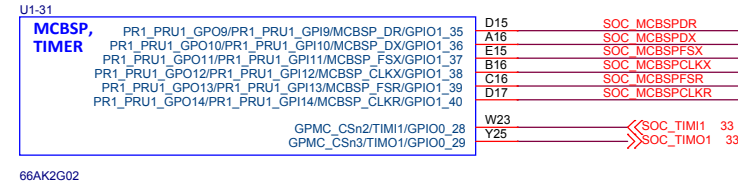
McASP0AHCLKX_BUFFER



I2C BUFFER



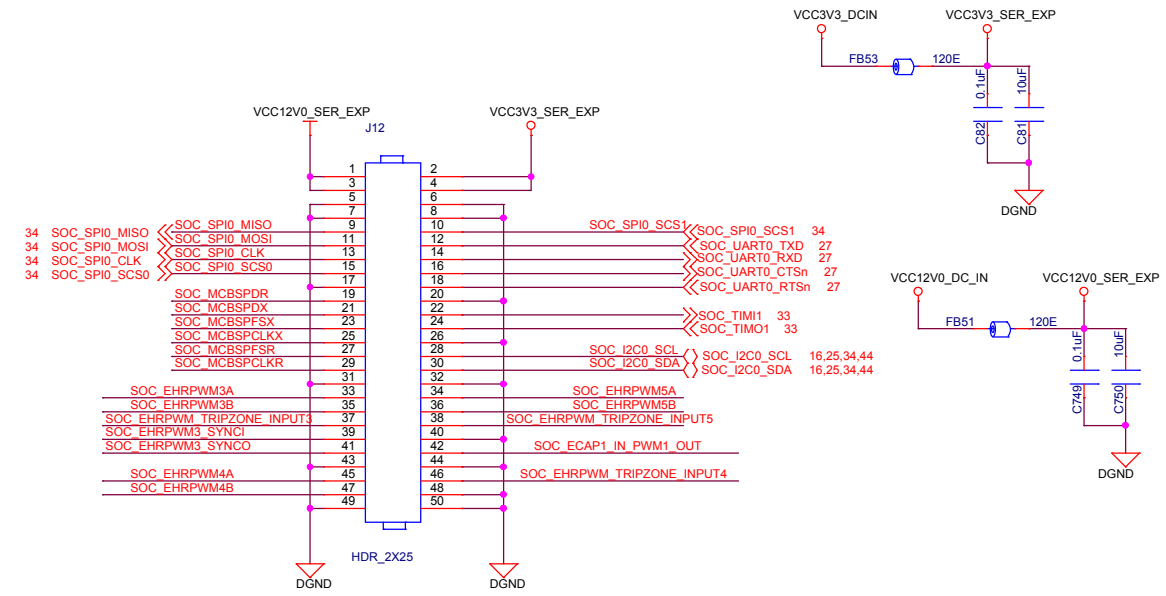
SoC McBSP



SoC PWM



SERIAL EXPANSION CONNECTOR



Project :

K2G EVM

Designed for TI by Mistral Solutions Pvt Ltd



Title SERIAL & EHRPWM EXP CONNECTOR

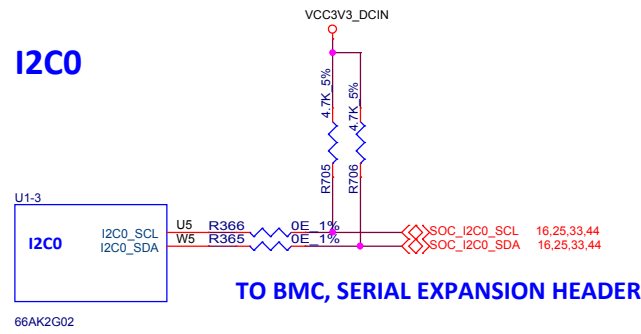
Size Document Number
C MS_TI_K2GEVM_SCH_REVD

Date: Thursday, April 14, 2016

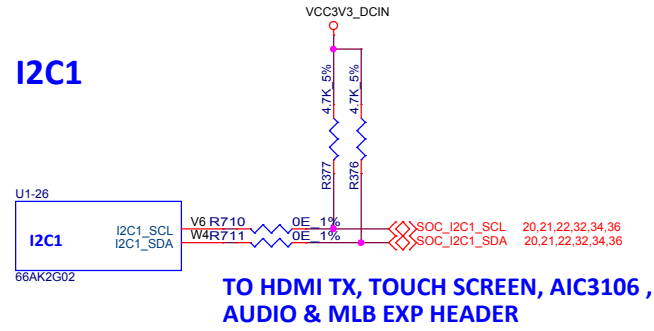
Sheet 33 of 50

Rev
D

I2C0

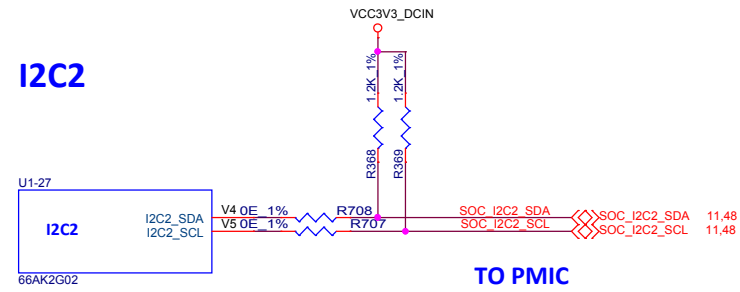


I2C1

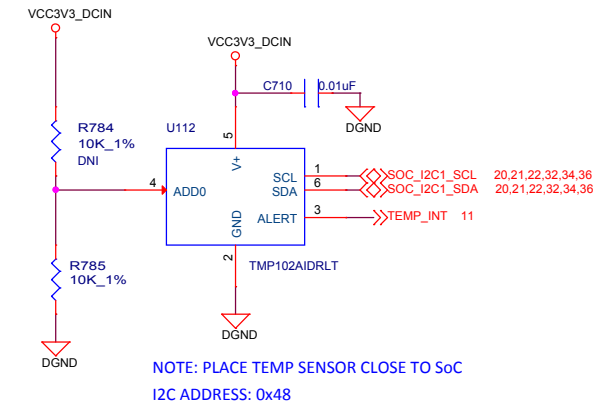


SoC I2C

I2C2

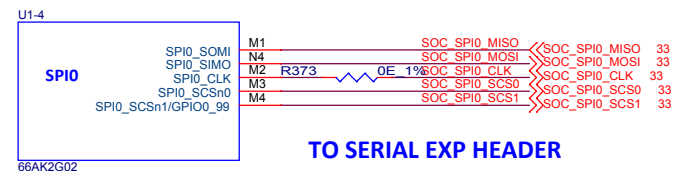


TEMPERATURE SENSOR

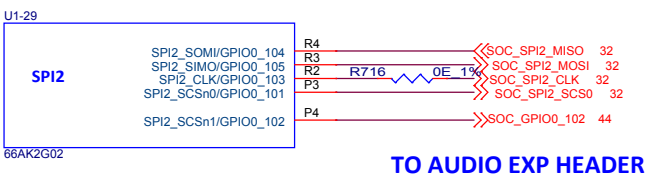


SoC SPI

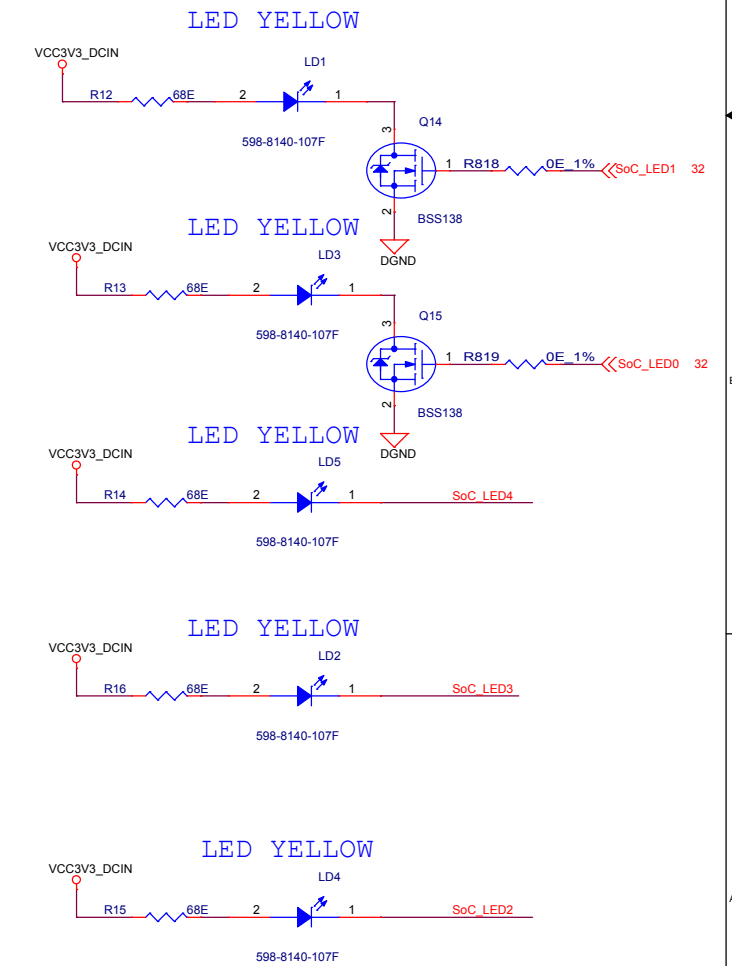
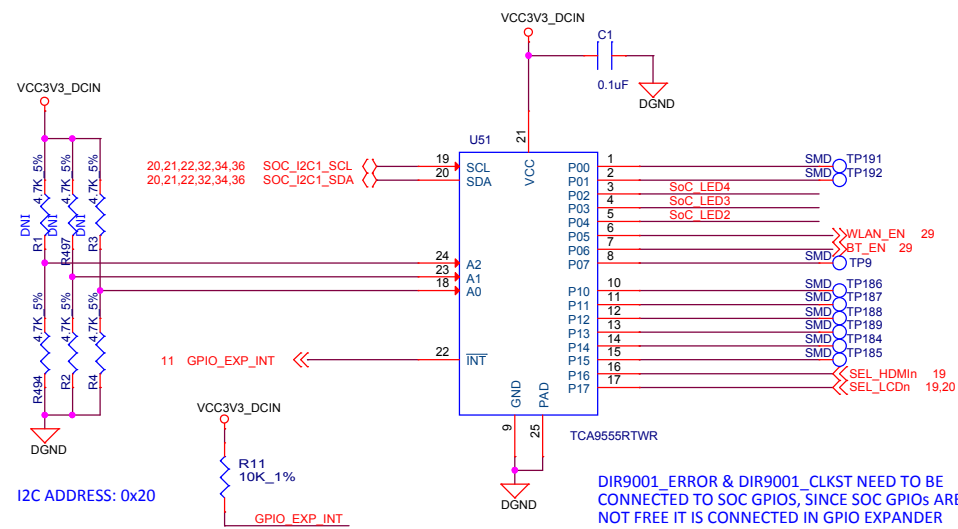
SPI0



SPI2

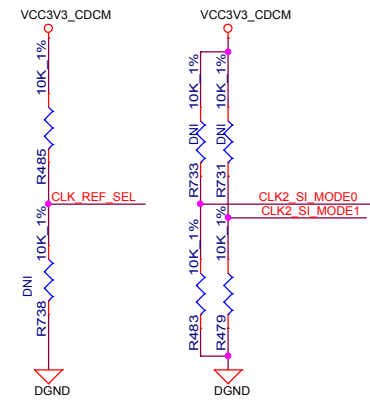


GPIO EXPANDER & LEDs



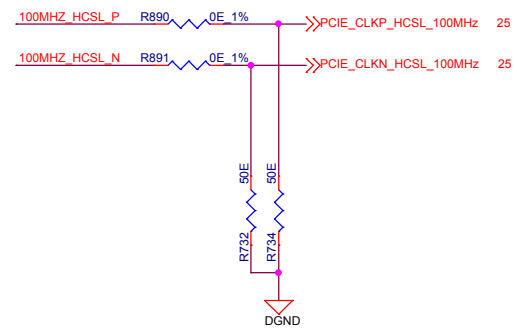
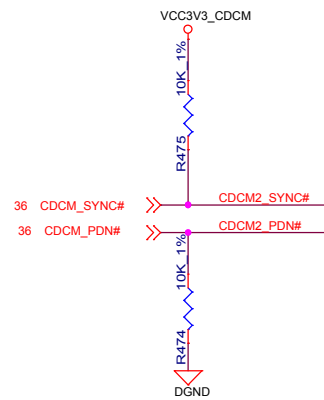
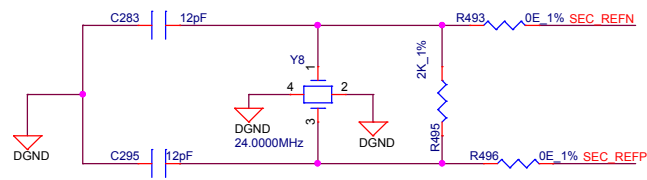
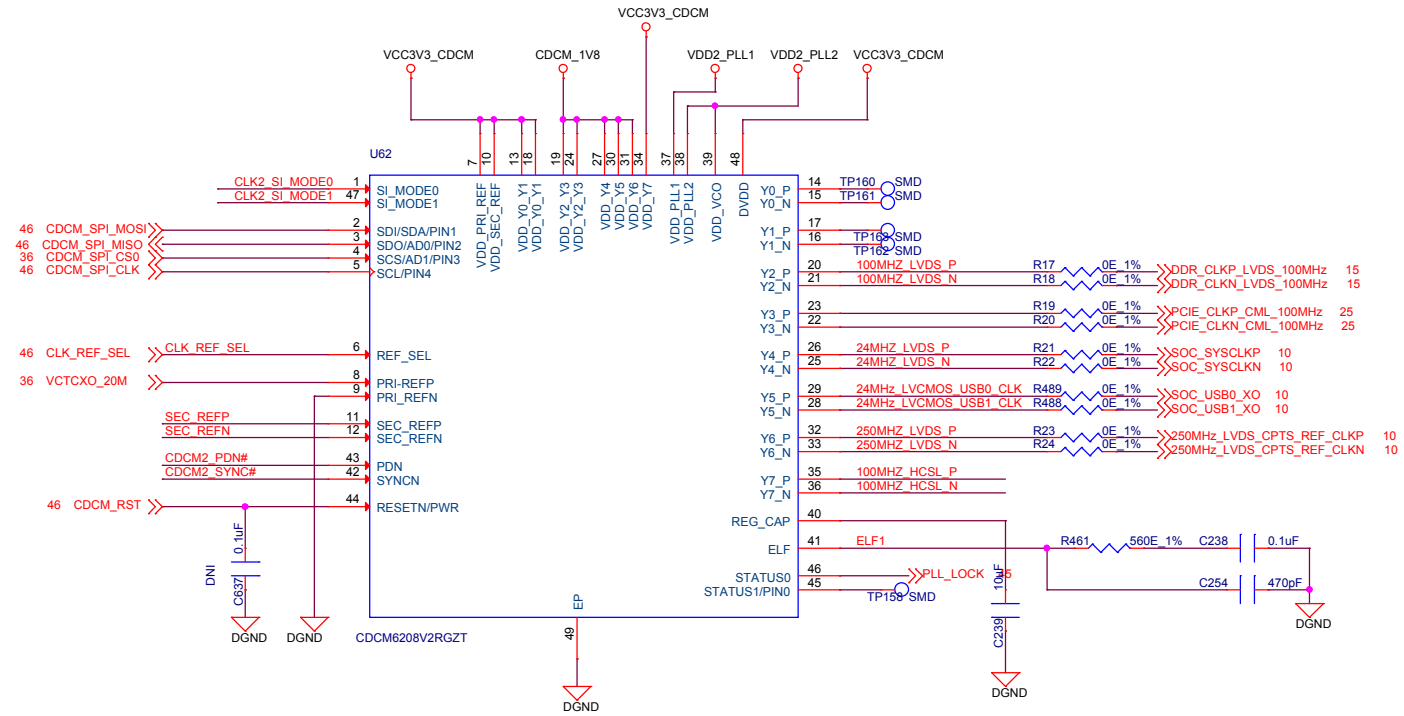
Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title SERIAL CONTROL INTERFACE	
K2G EVM		Size	Document Number
		C	MS_TI_K2GEVM_SCH_REV D
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CLOCK GENERATOR

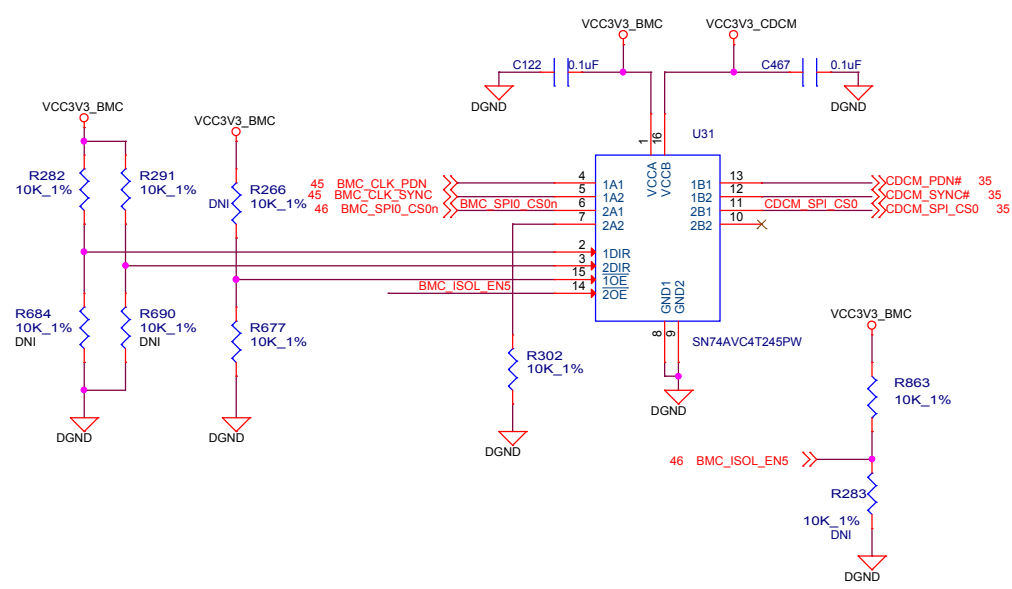


MODE SELECTION FOR CDCM DEVICE

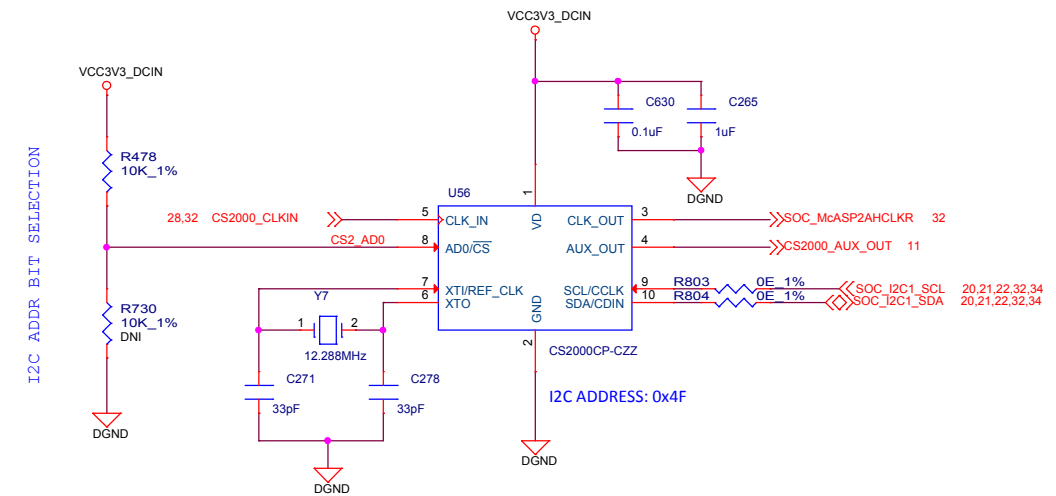
SI_MODE1	SI_MODE0	MODE SELECTED
0	0	SPI MODE
0	1	I2C MODE
1	0	PIN MODE (NO SERIAL PROGRAMMING)
1	1	RESERVED



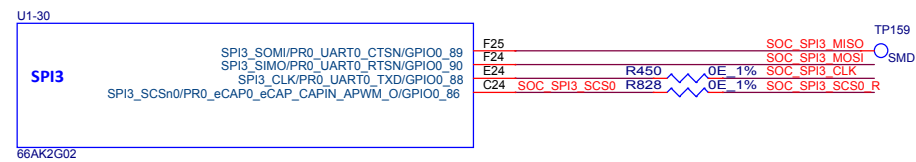
BMC ISOLATOR 5



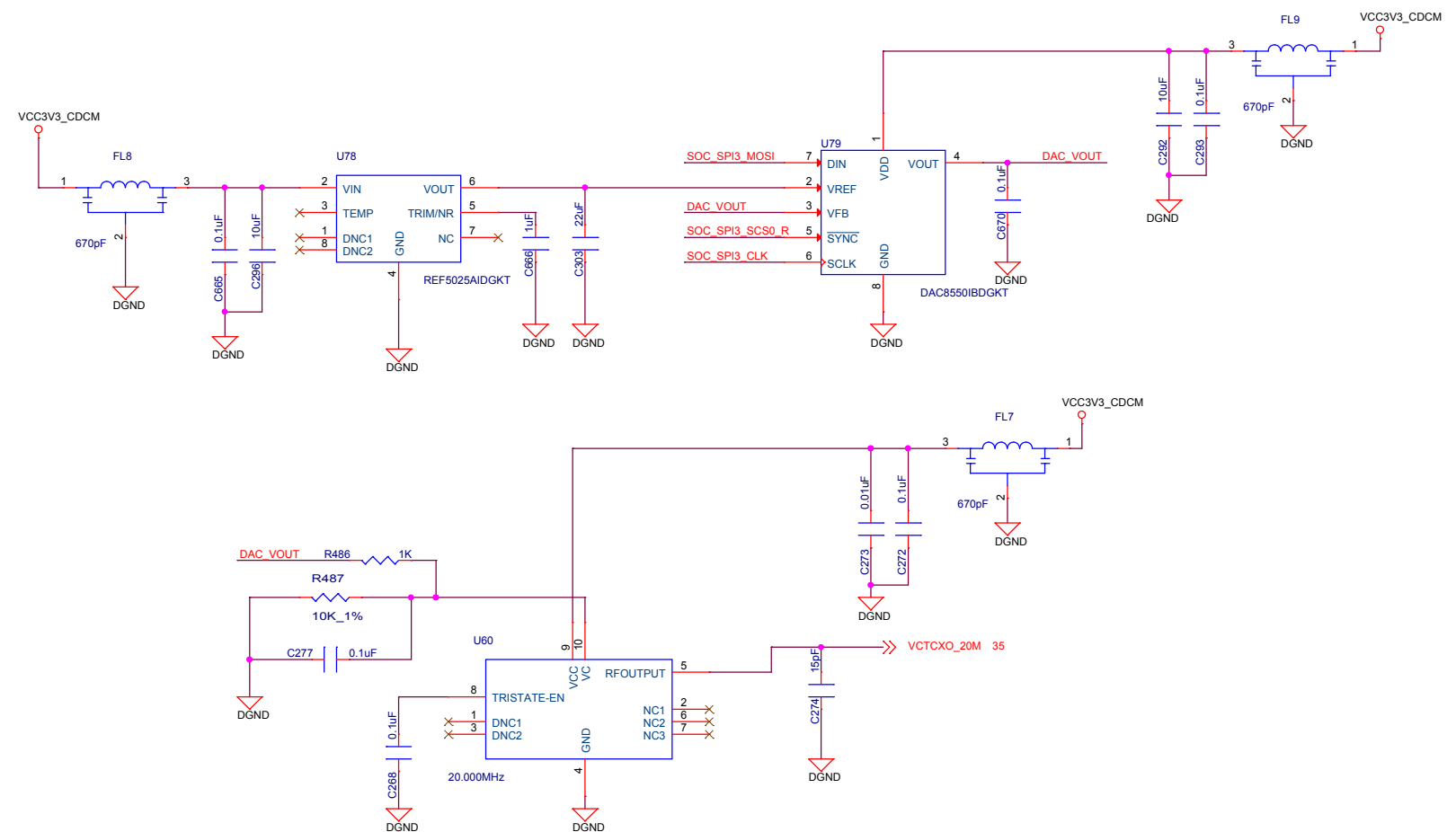
GENERATOR - AUDIO CLOCK DOMAIN

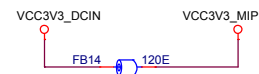


SoC SPI3

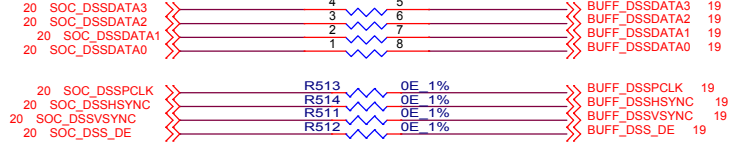
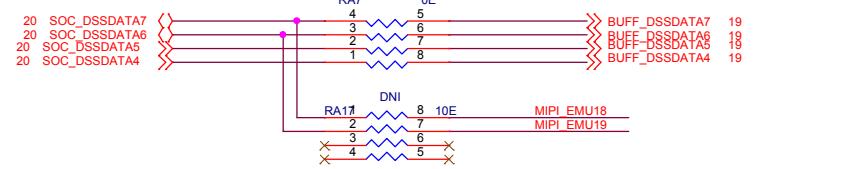
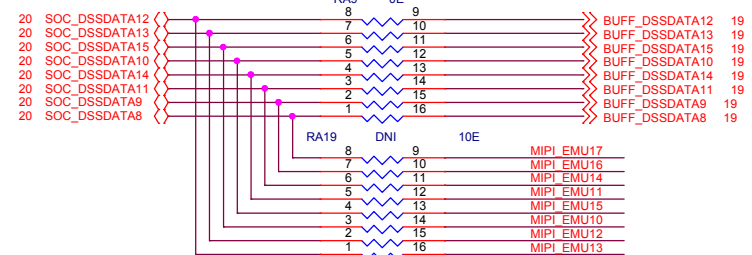
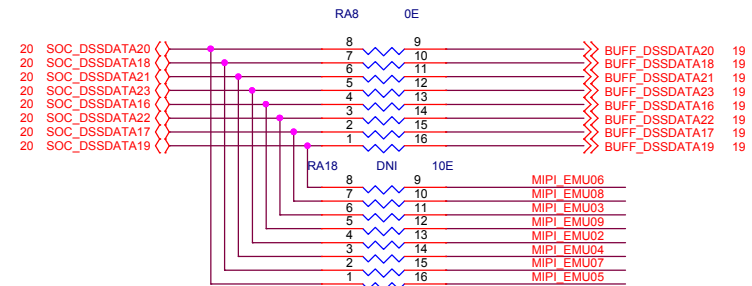
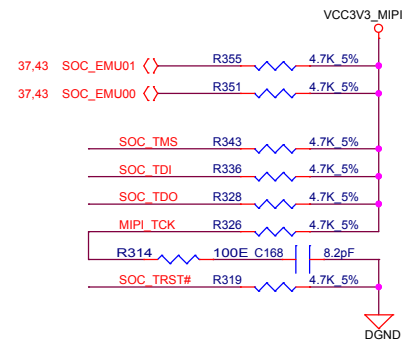
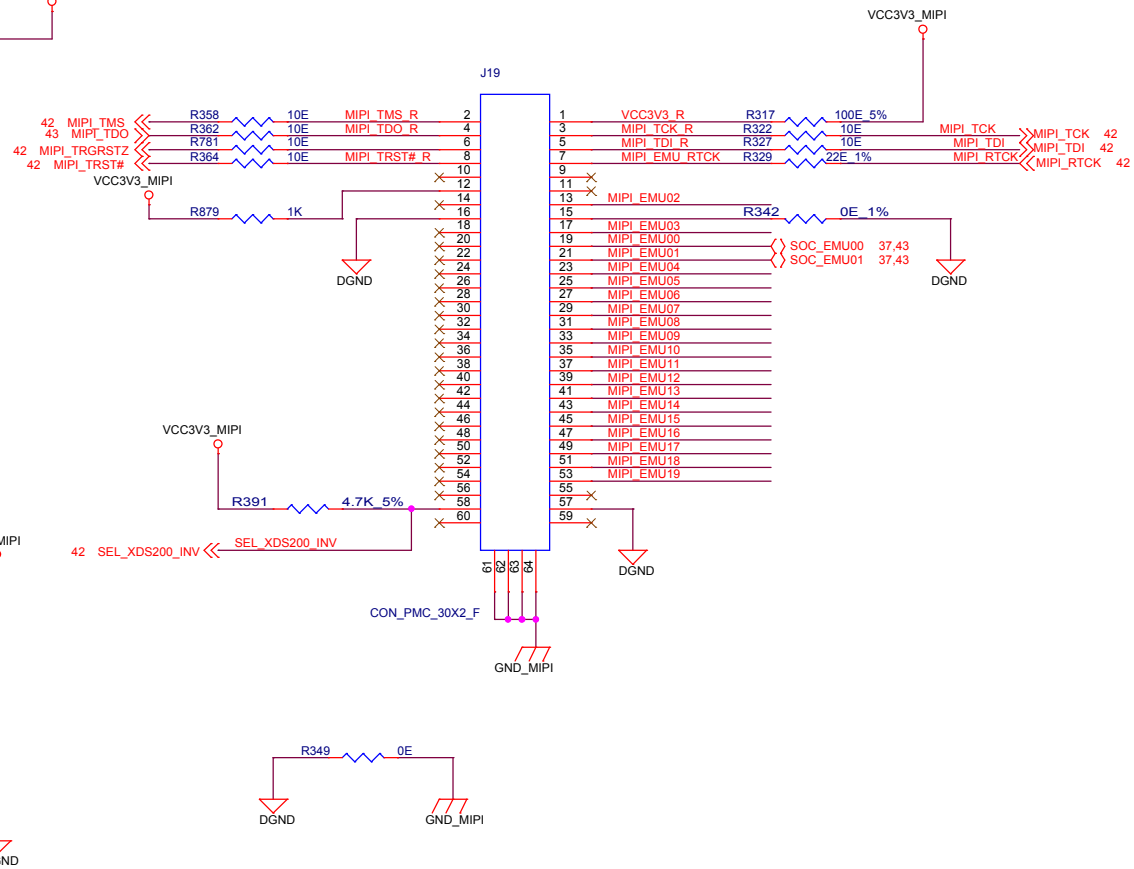


AVB CLOCK GENERATOR- 1588 CLOCK DOMAIN



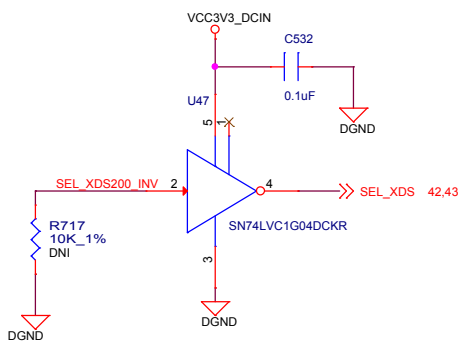
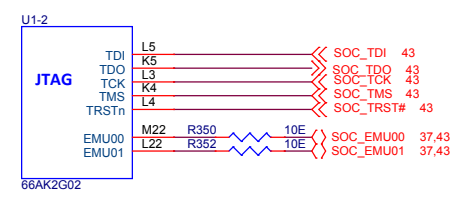


MIPI 60

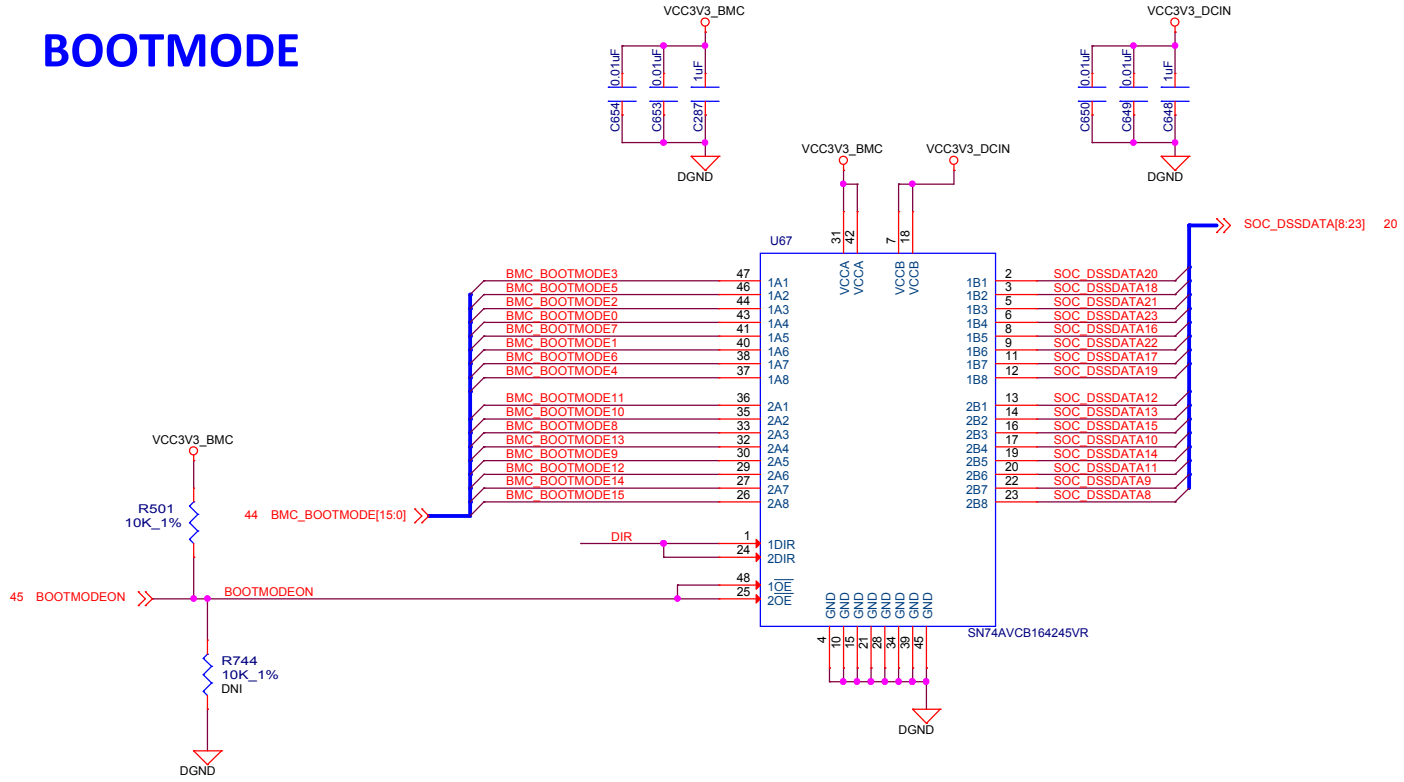
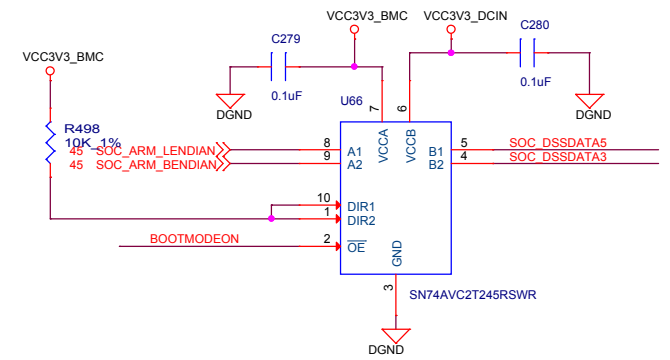


Res MUX between Display and JTAG TRACE Functionality
 -For display, install RA7, RA8 & RA9 . DNI RA17,RA18 & RA19
 -For TRACE, install RA17, RA18 & RA19. DNI RA7, RA8 & RA9

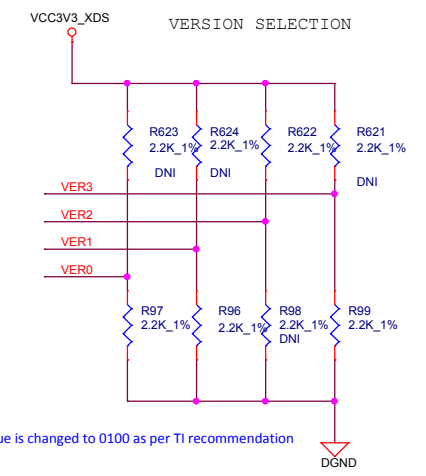
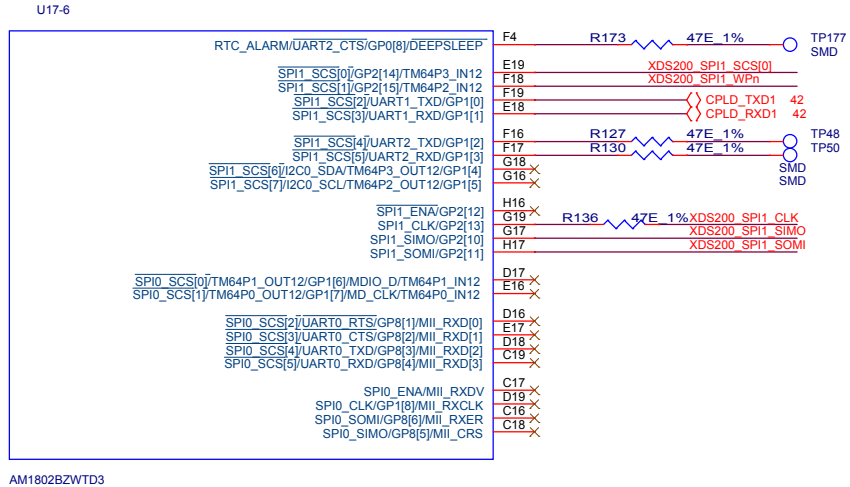
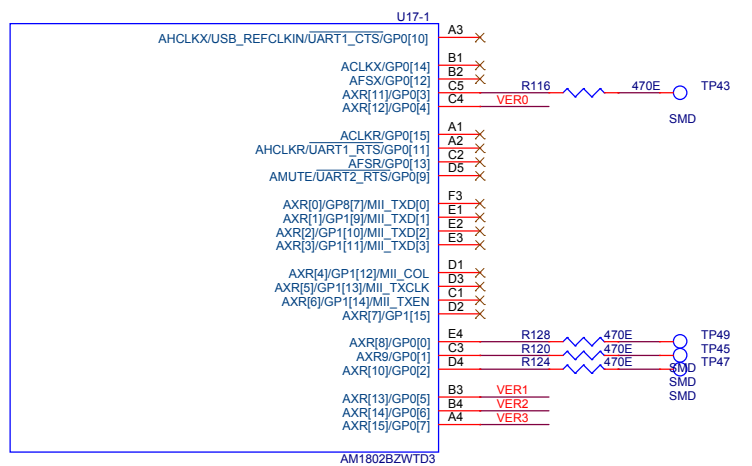
SoC JTAG



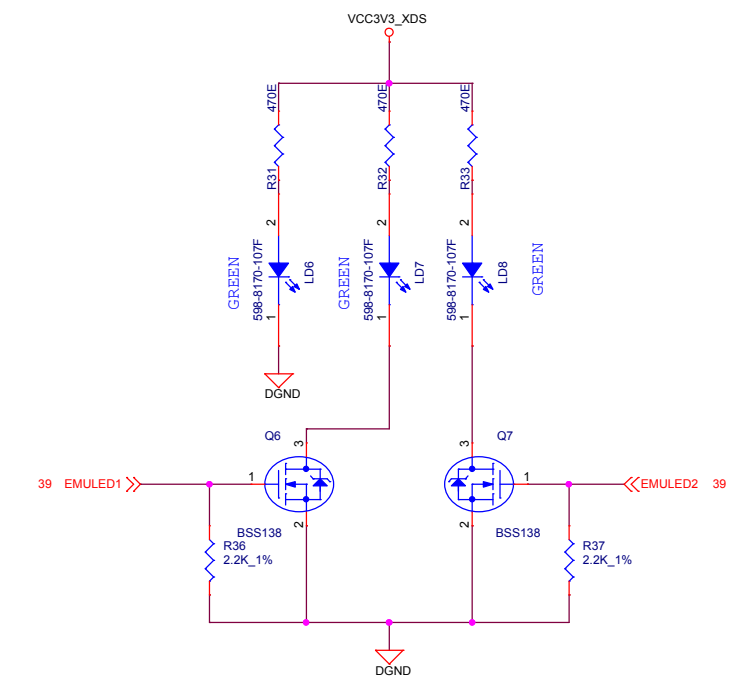
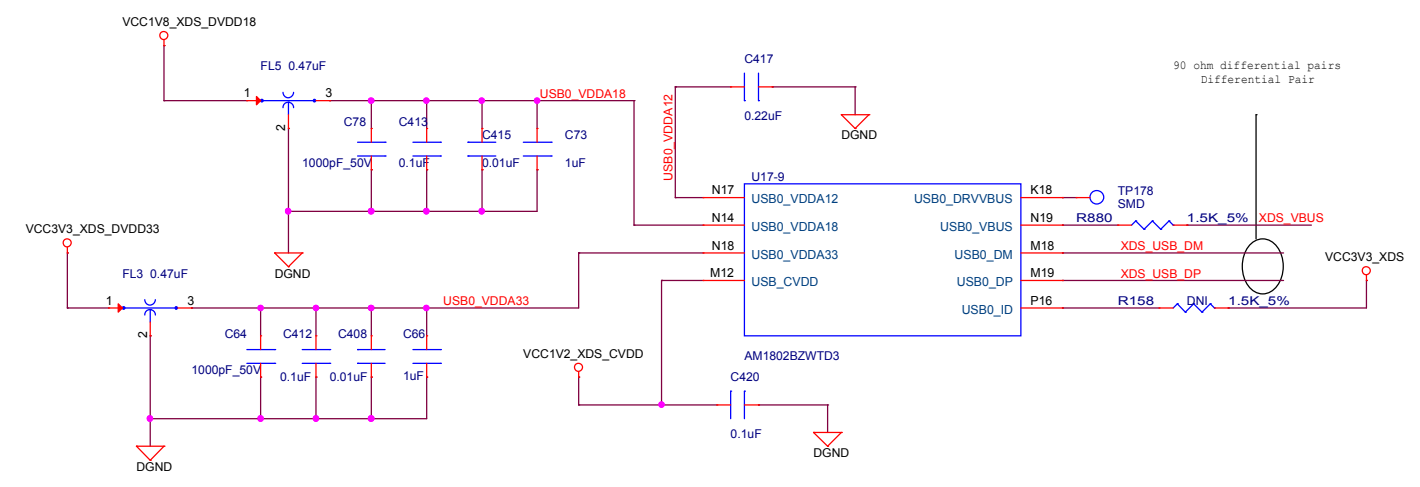
BOOTMODE



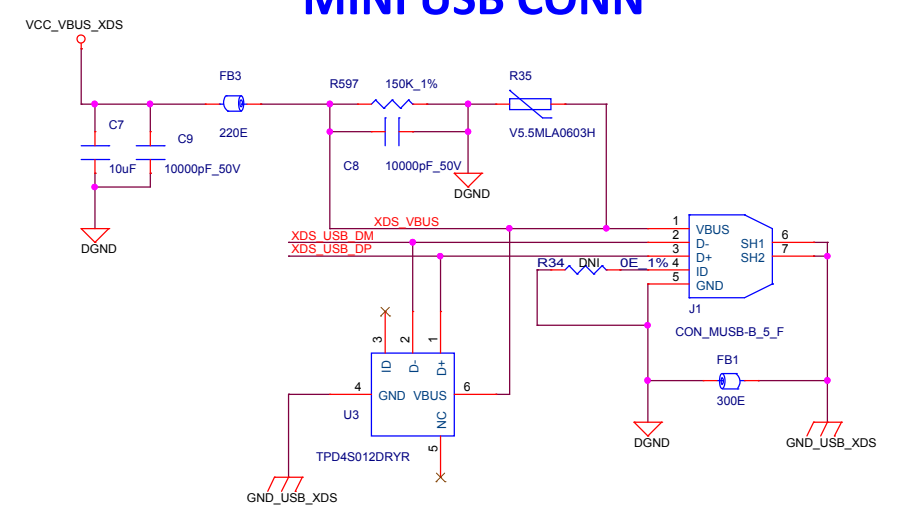
Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title		EMU & MIPI60 CONNECTOR
K2G EVM		Size	Document Number	Rev
		C	MS_TI_K2GEVM_SCH_REV D	D
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XDS200

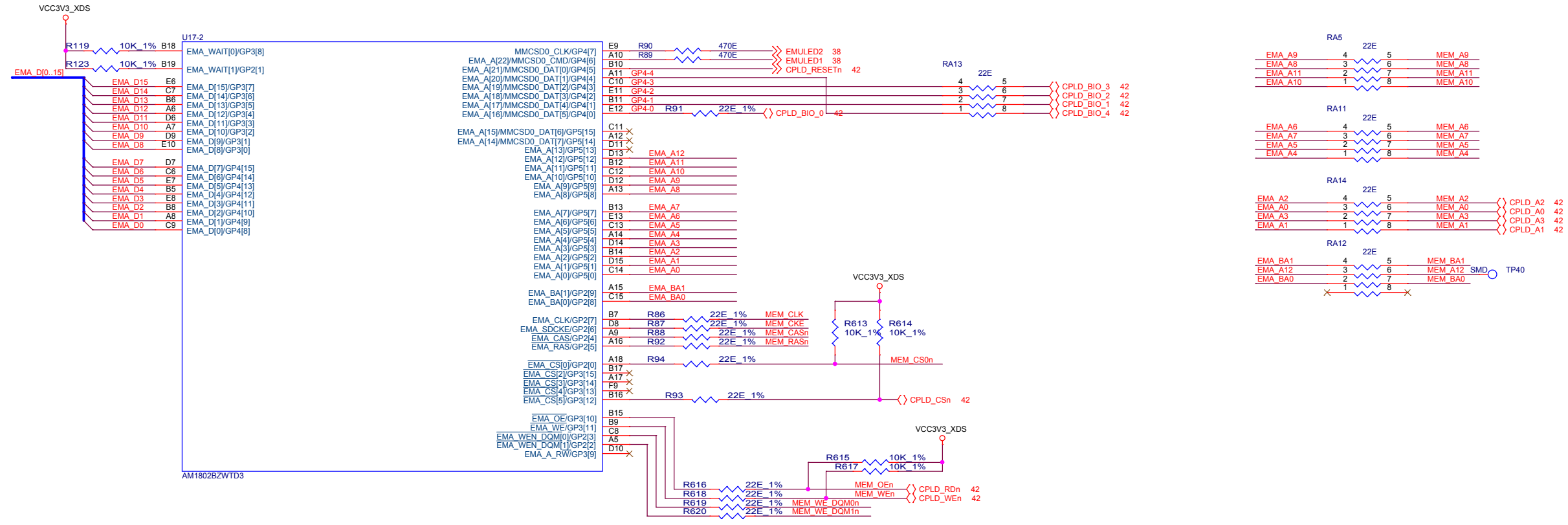


MINI USB CONN

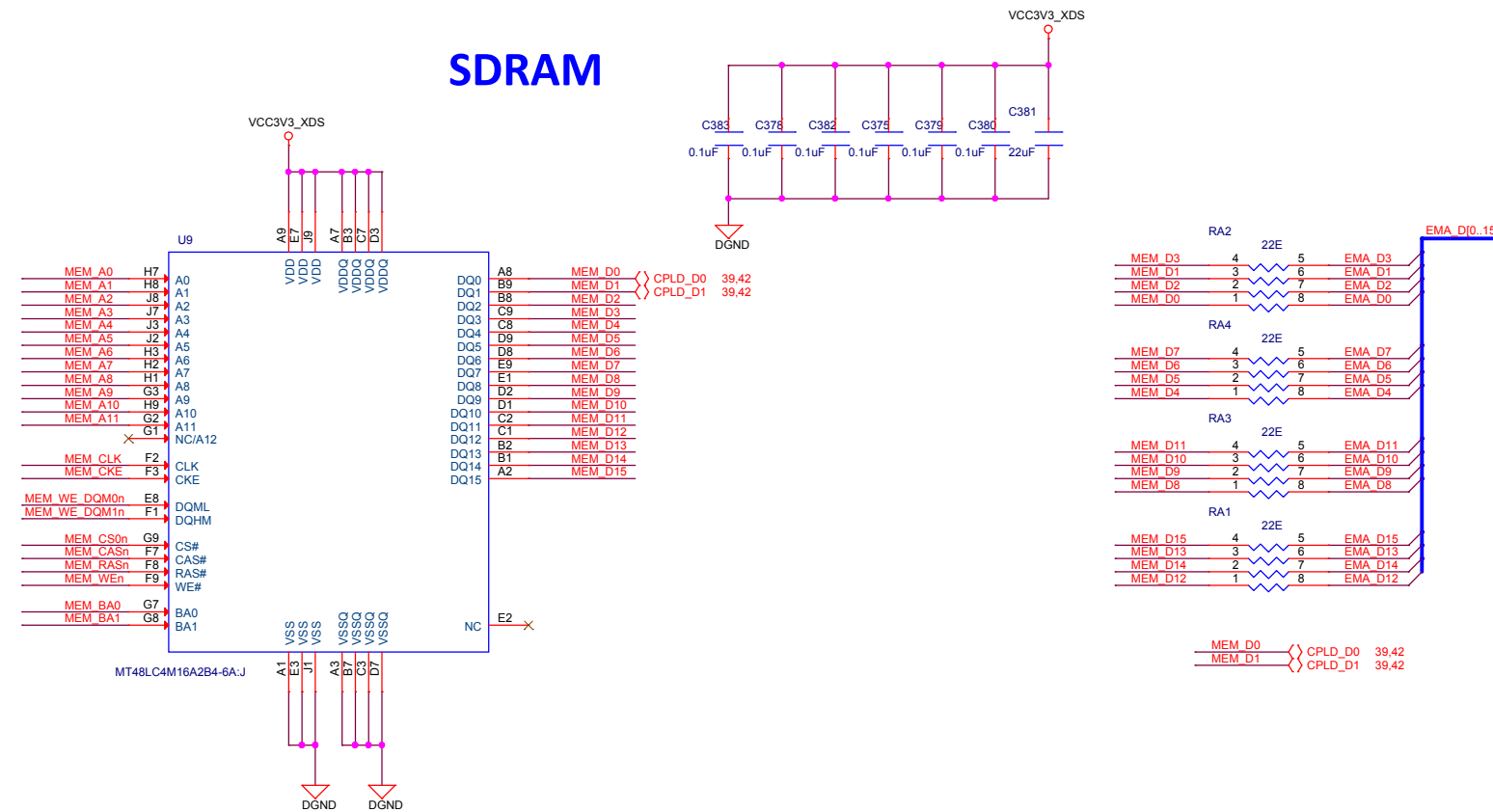


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title	XDS200
K2G EVM		Size	Document Number
		C	MS_TI_K2GEVM_SCH_REV D
		Date:	Wednesday, April 13, 2016
		Sheet	38 of 50
		Rev	D

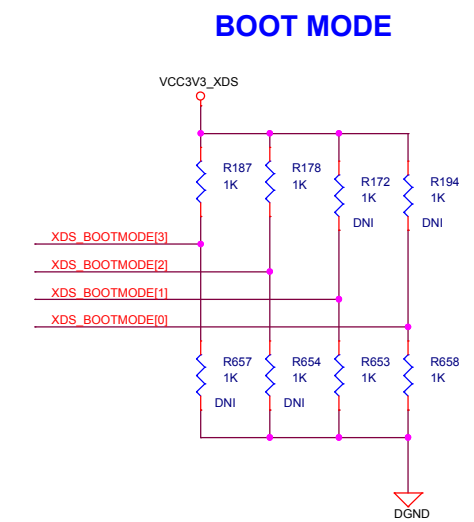
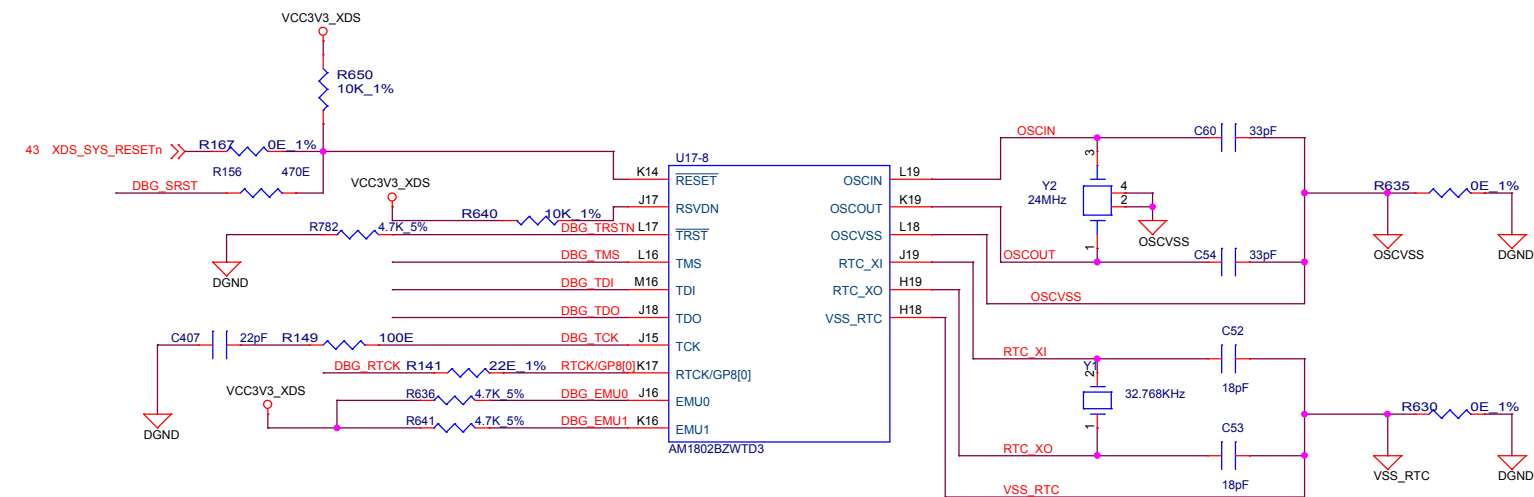
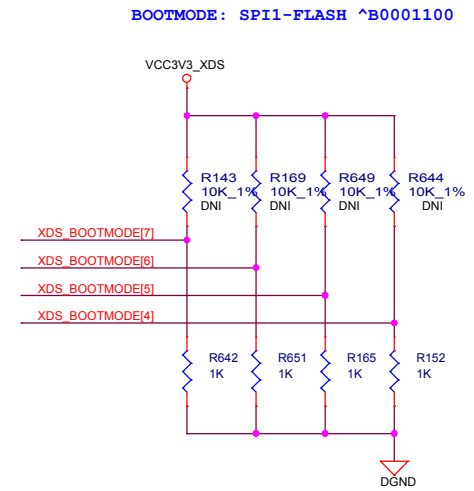
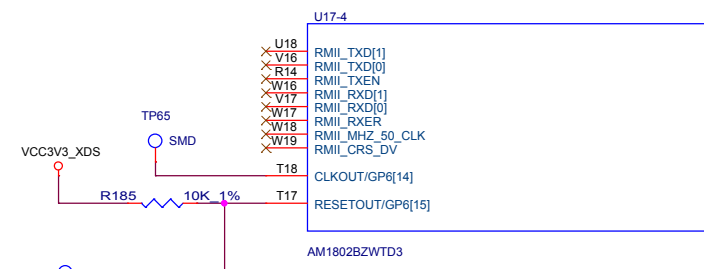
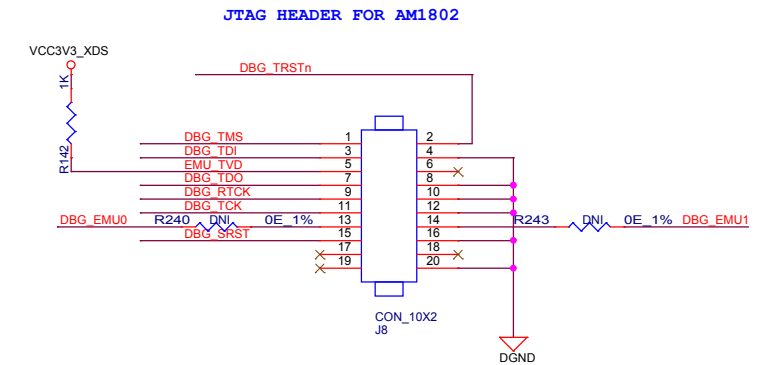
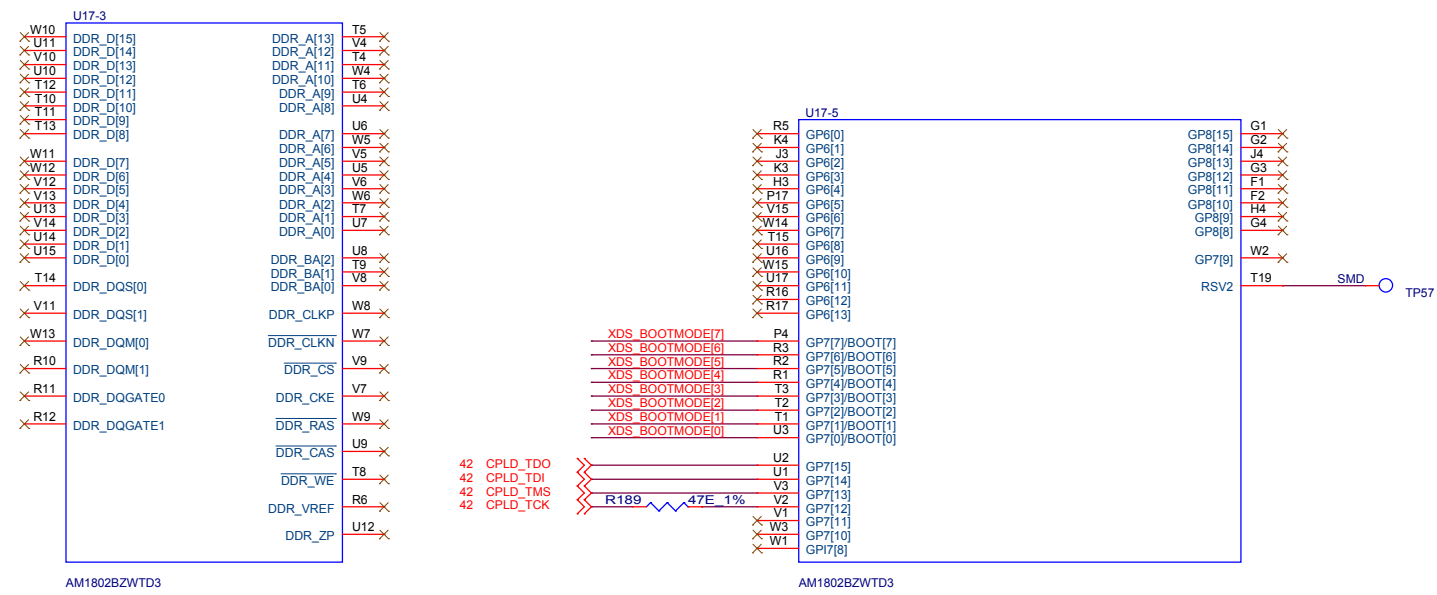
XDS200



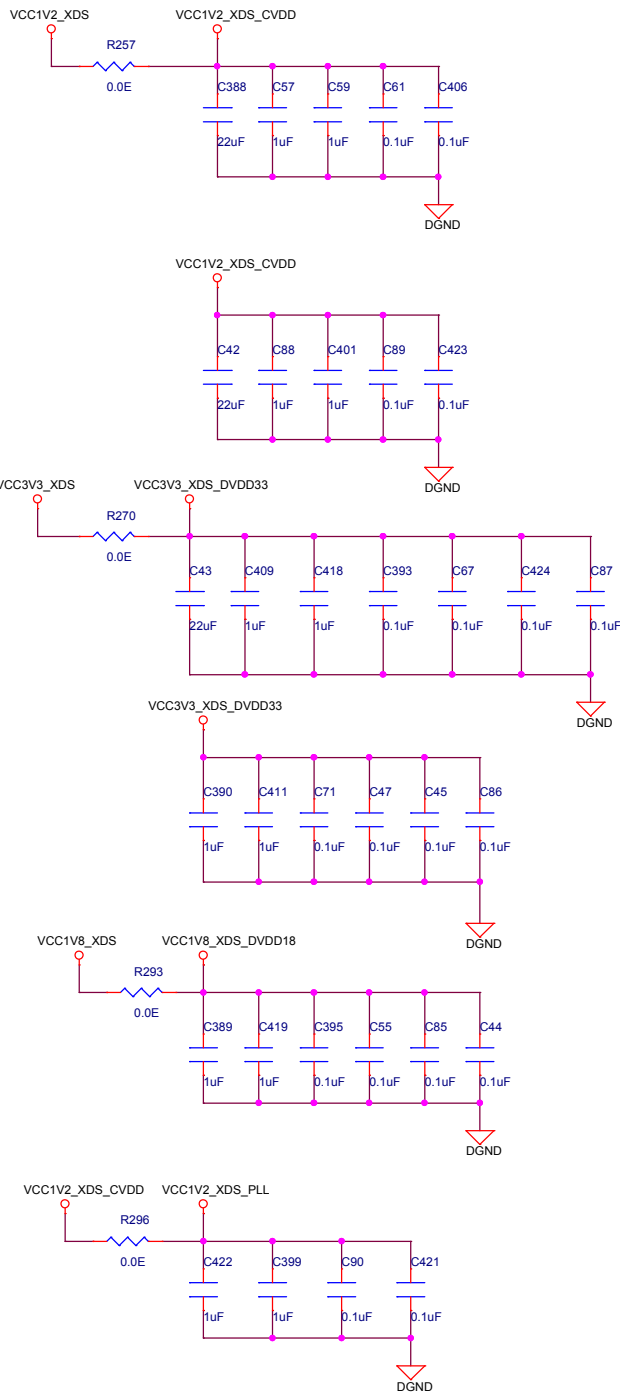
SDRAM



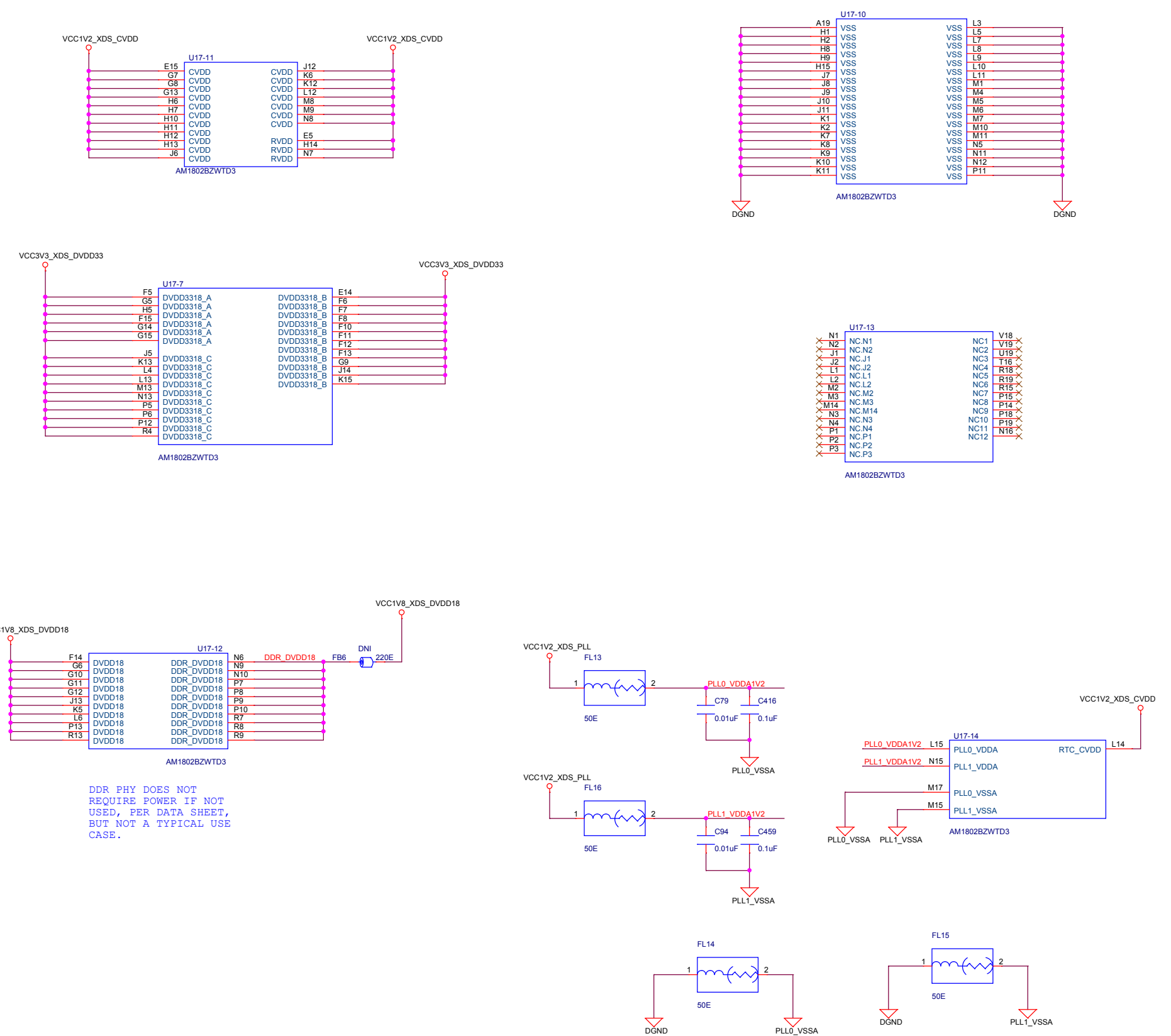
XDS200



XDS200 DECAPS

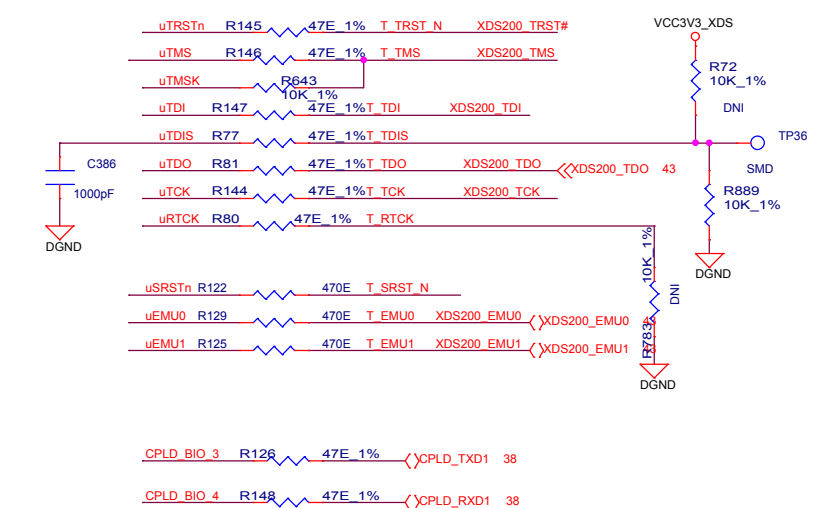
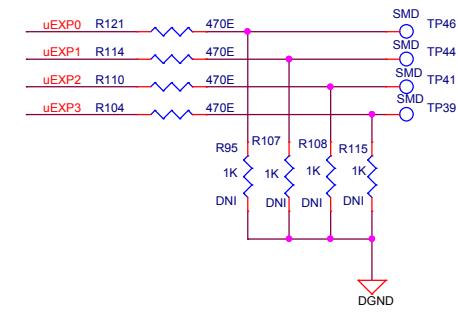
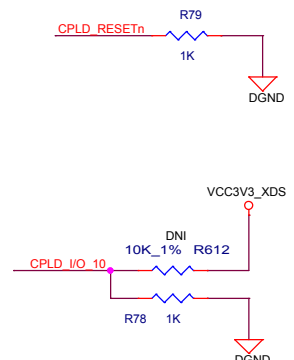
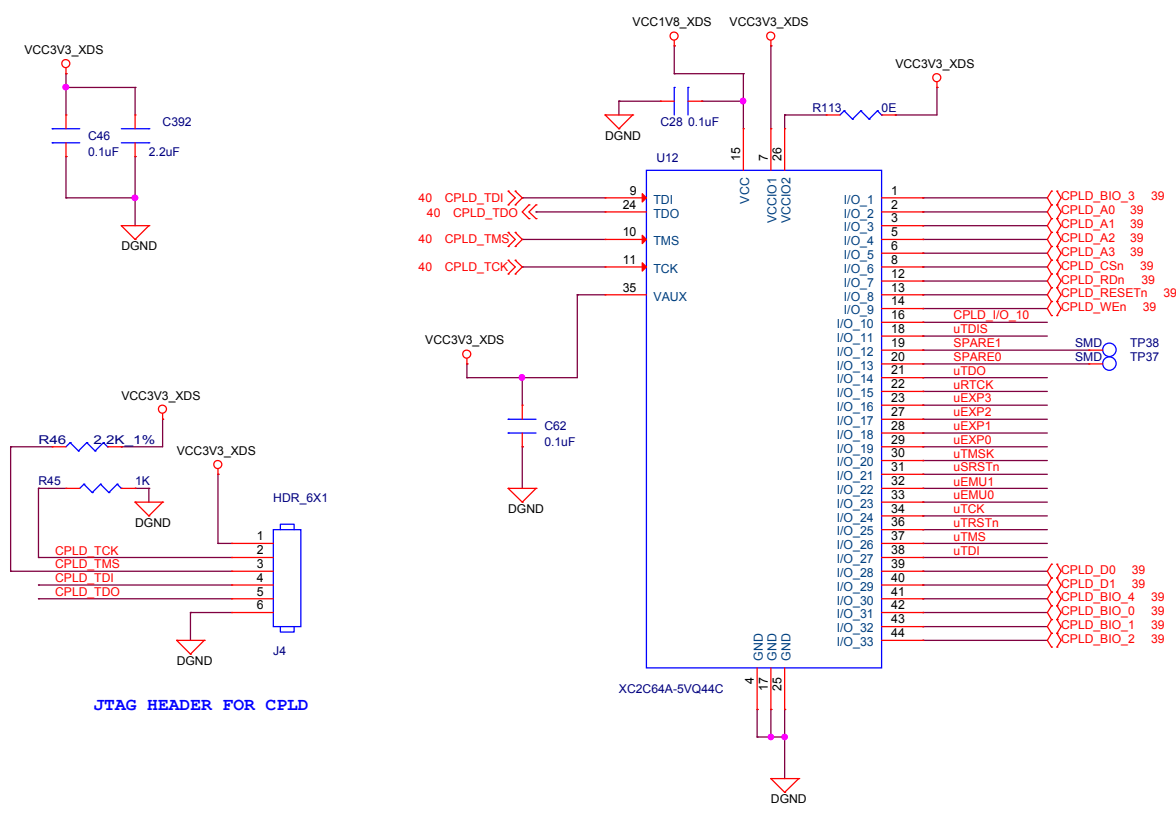


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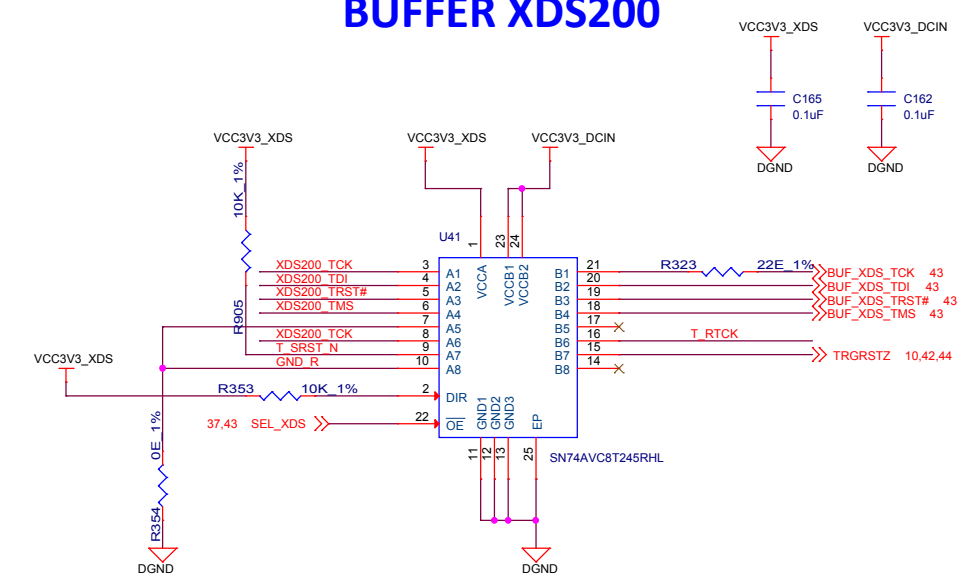


DDR PHY DOES NOT REQUIRE POWER IF NOT USED, PER DATA SHEET, BUT NOT A TYPICAL USE CASE.

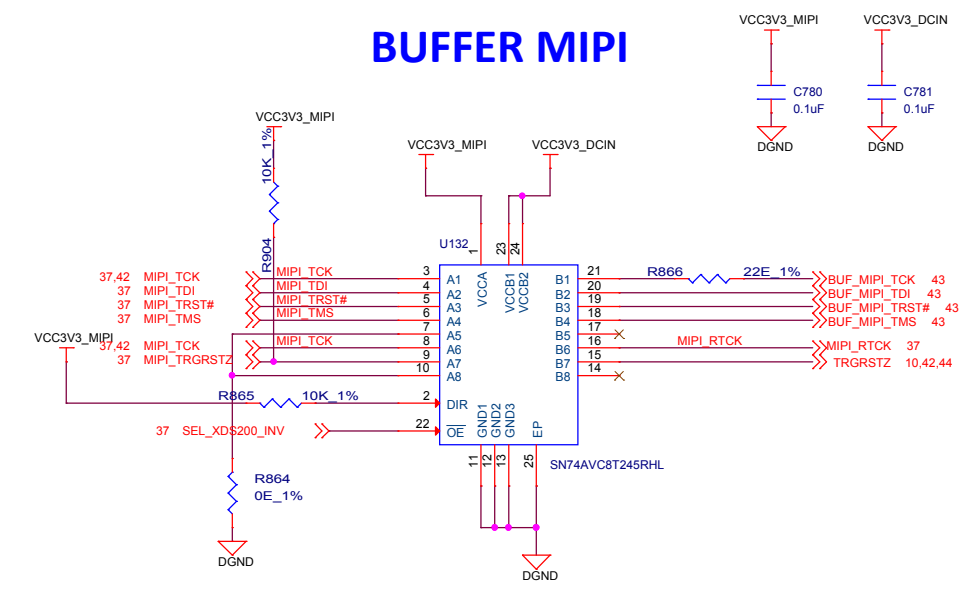
XDS200 CPLD



BUFFER XDS200

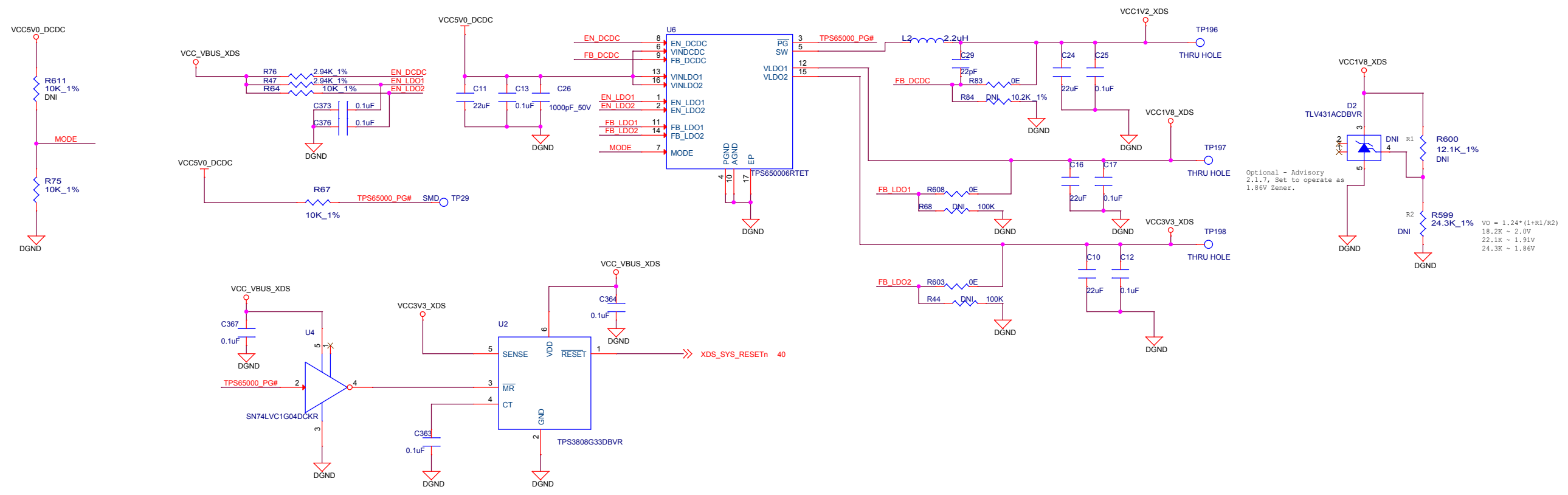


BUFFER MIPI

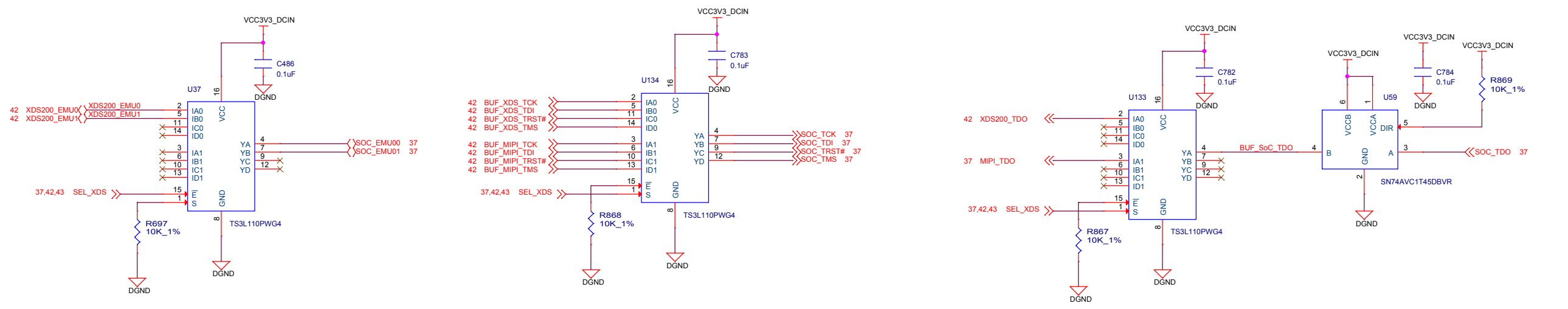


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title	JTAG_XDS200_CPLD	
K2G EVM	 	Size	Document Number	Rev
		C	MS_TI_K2GEVM_SCH_REV D	D
		Date:	Wednesday, April 13, 2016	Sheet 42 of 50

XDS200 POWER

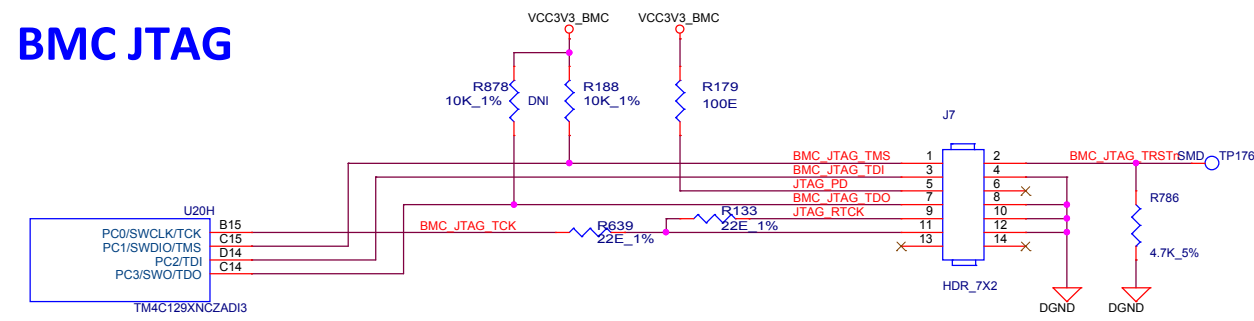


JTAG FET SWITCH

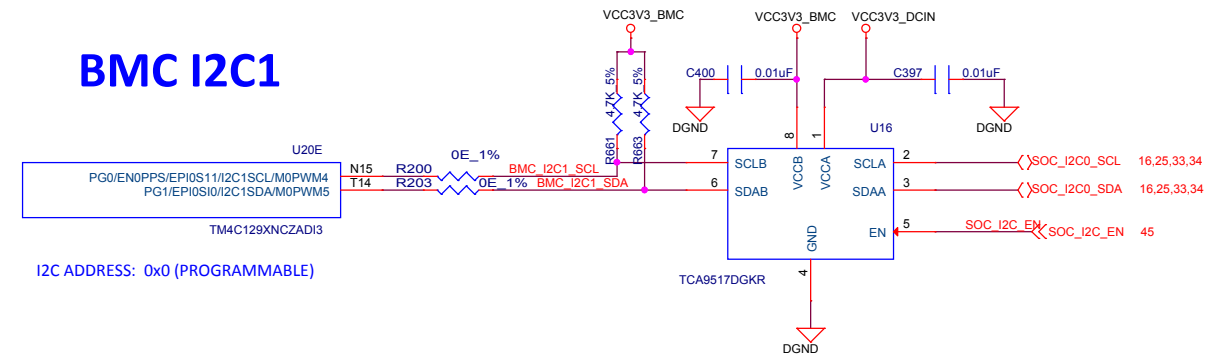


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title	XDS200 POWER	
K2G EVM	 	Size	Document Number	Rev
		C	MS_TI_K2GEVM_SCH_REVD	D
		Date:	Wednesday, April 13, 2016	Sheet 43 of 50

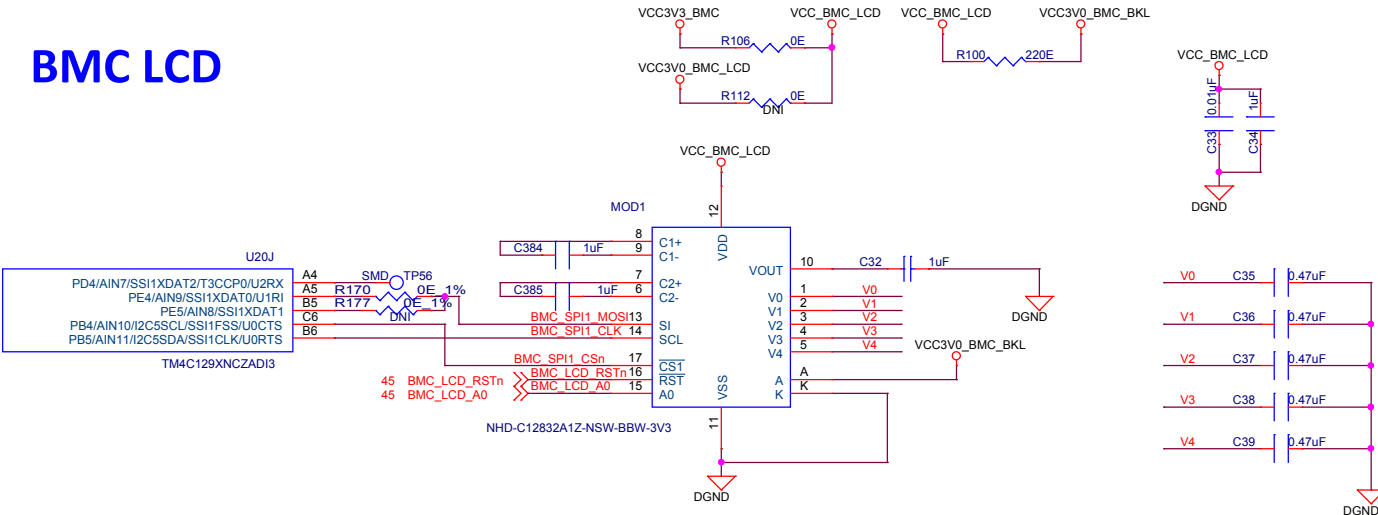
BMC JTAG



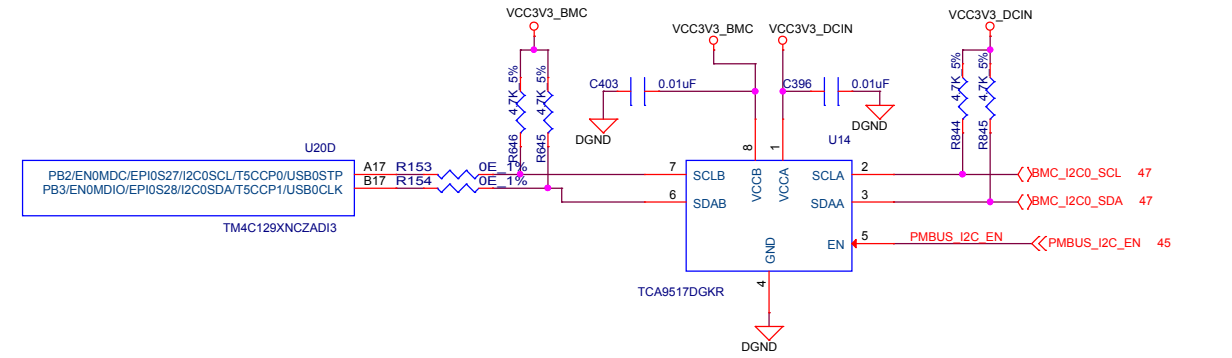
BMC I2C1



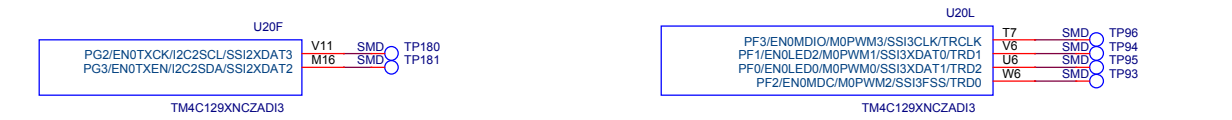
BMC LCD



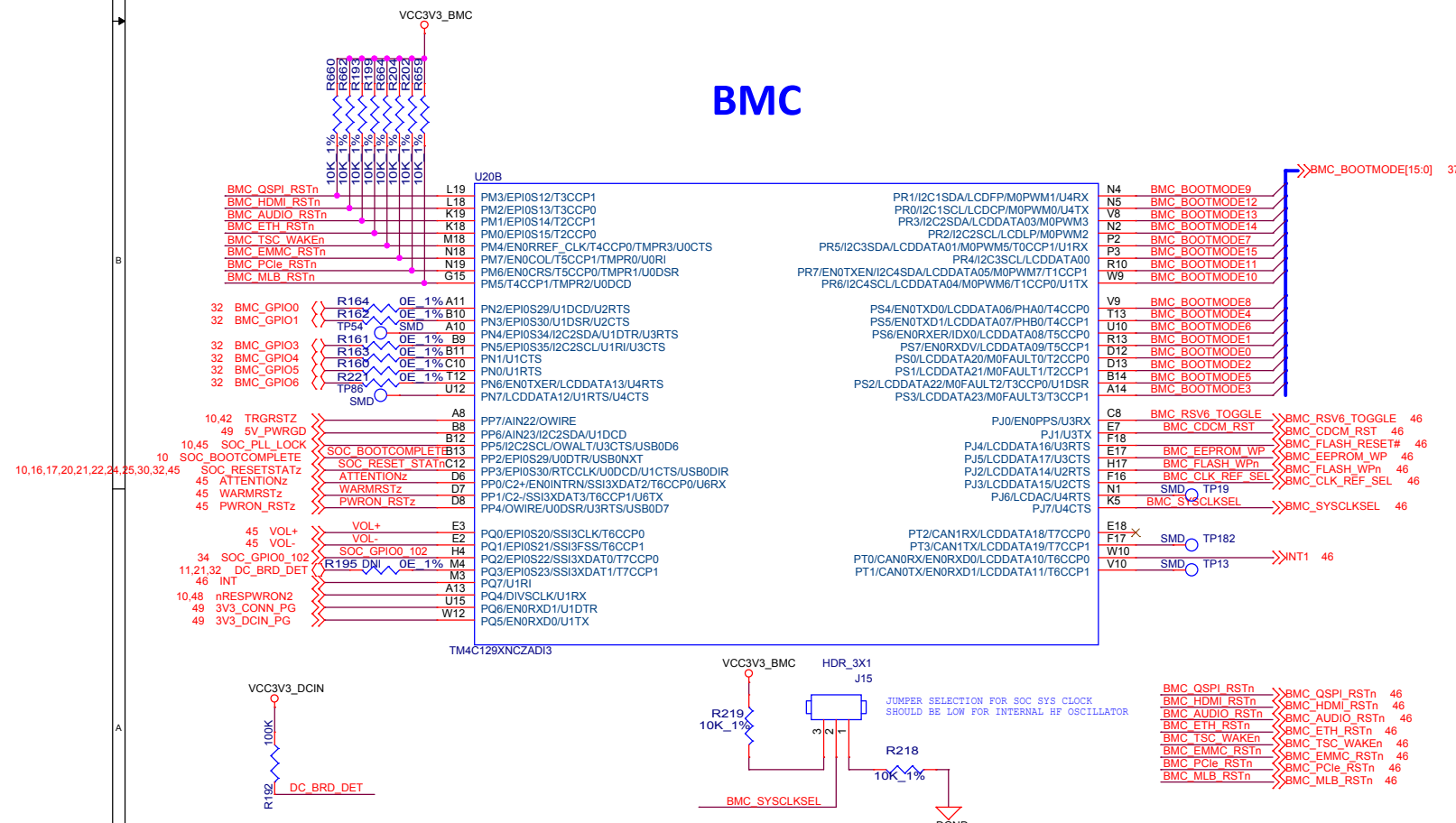
BMC I2C0



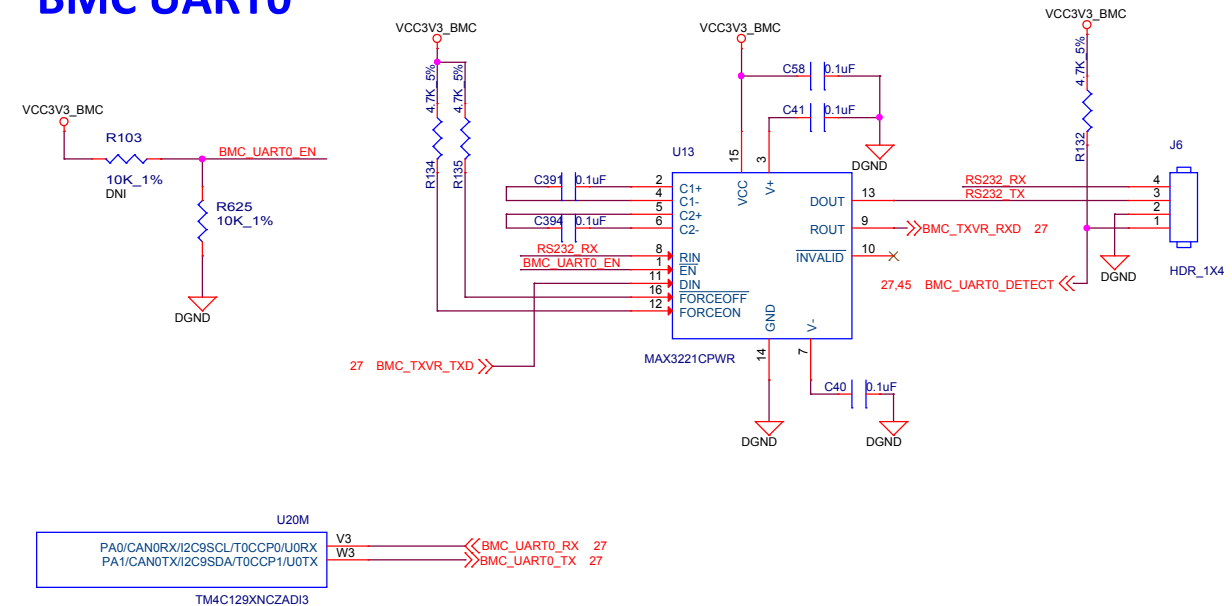
BMC TEST POINTS



BMC

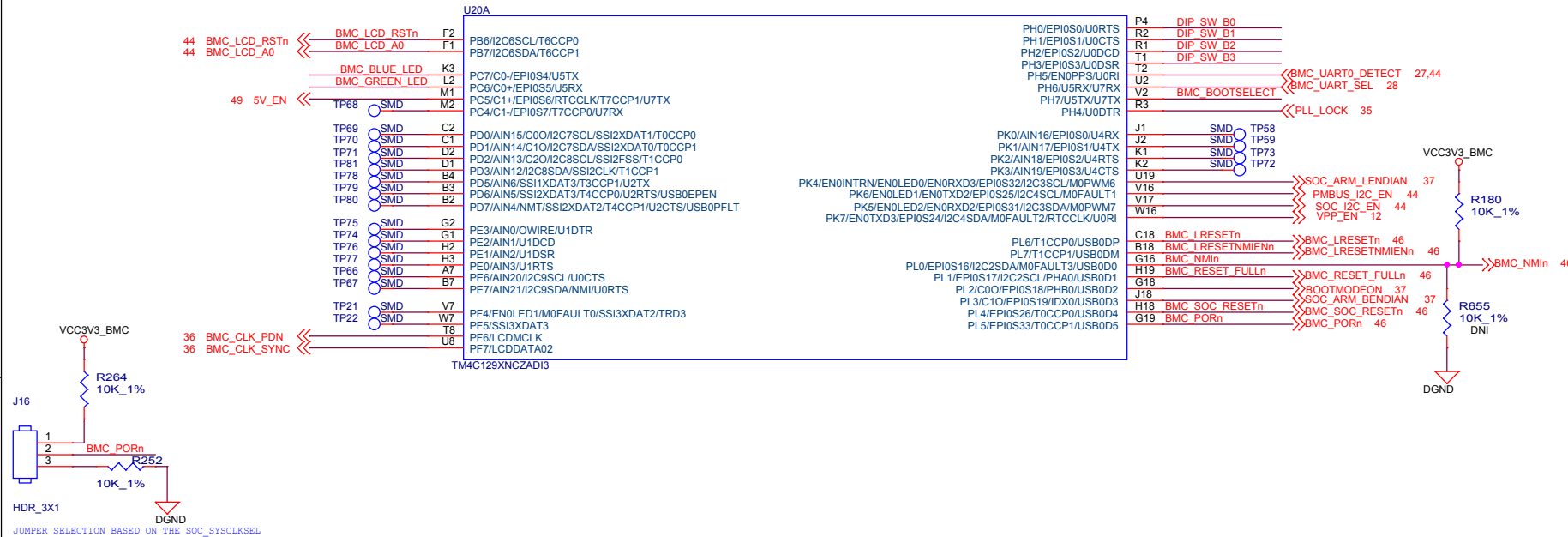


BMC UART0

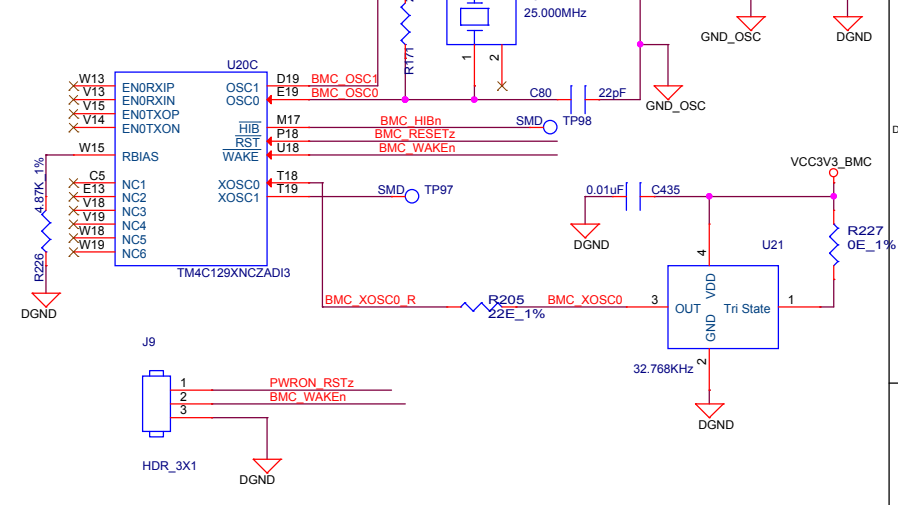


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title	BOARD MANAGEMENT CONTROL_1	
K2G EVM		Size	Document Number	Rev
		C	MS_TI_K2GEVM_SCH_REV D	D
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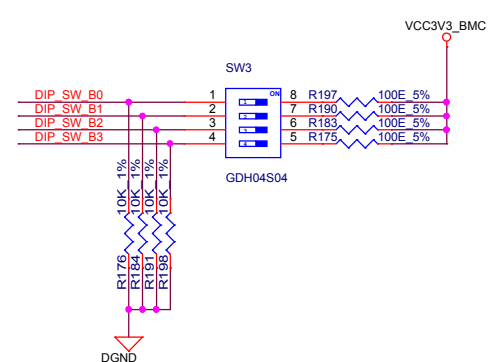
BMC



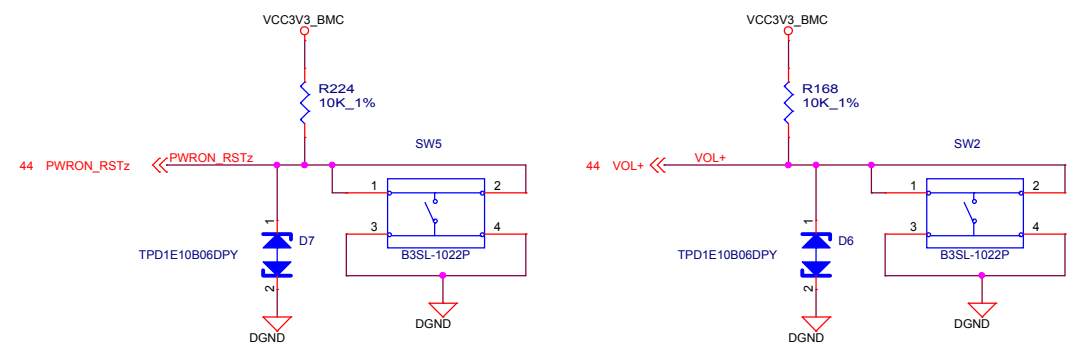
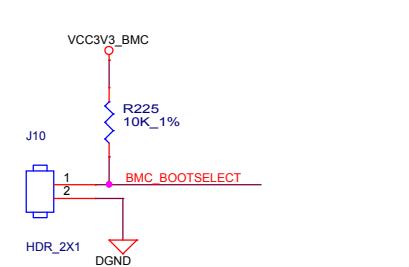
BMC CLOCK



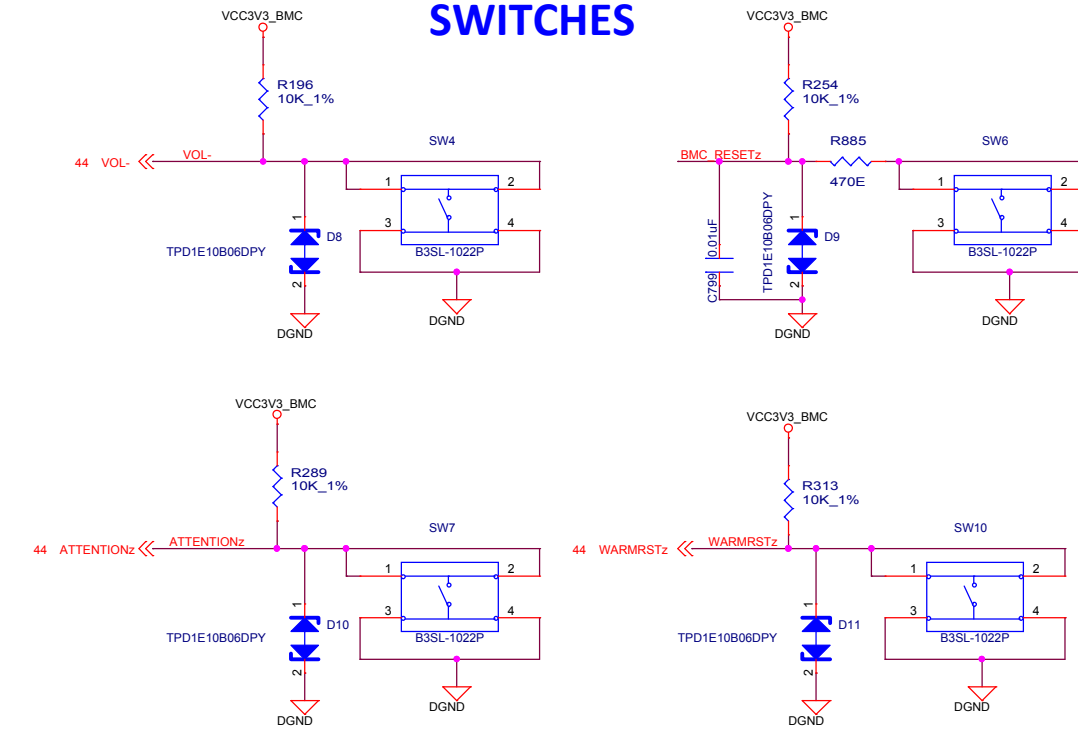
DIP SWITCH



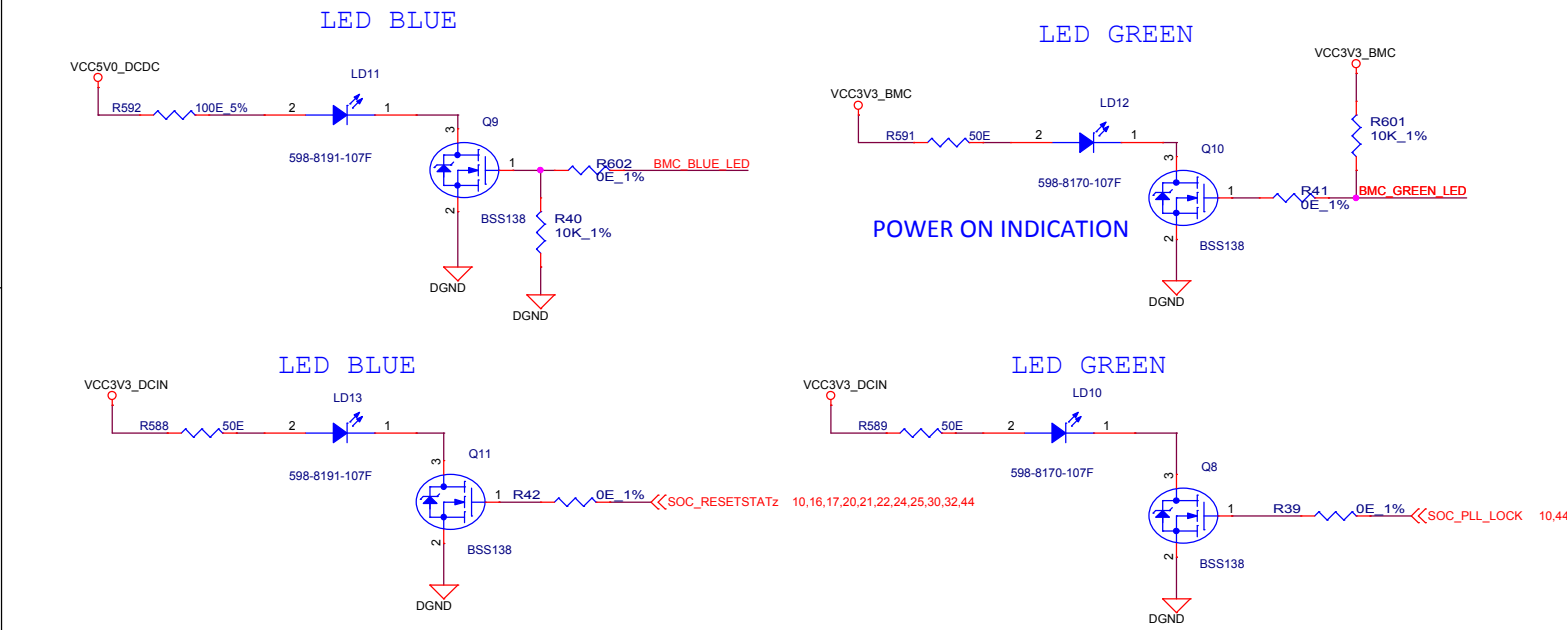
BMC BOOT SELECT



PUSH BUTTON SWITCHES

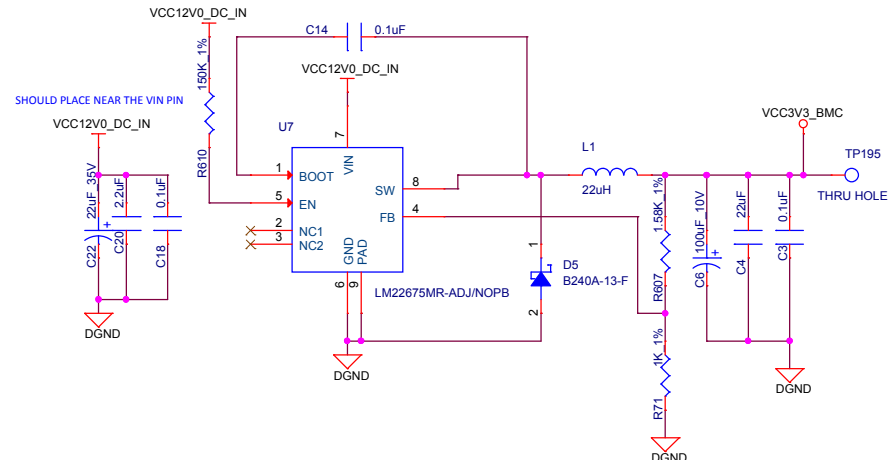


LEDS

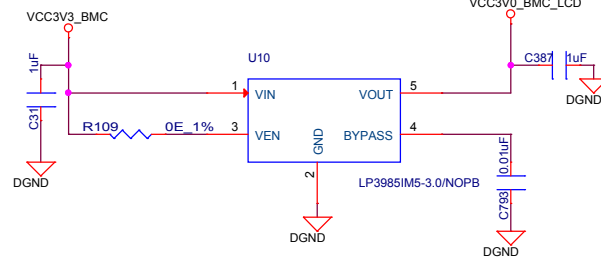


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title	BOARD MANAGEMENT CONTROL_2
K2G EVM	 	Size	Document Number
		C	MS_TI_K2GEVM_SCH_REV D
		Date:	Wednesday, April 13, 2016
		Sheet	45 of 50
		Rev	D

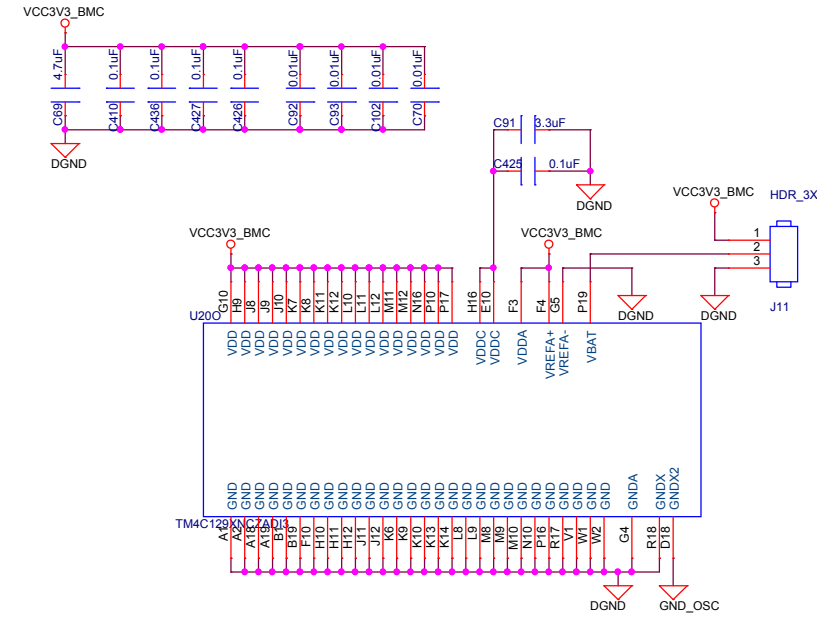
BMC 3.3V GENERATOR



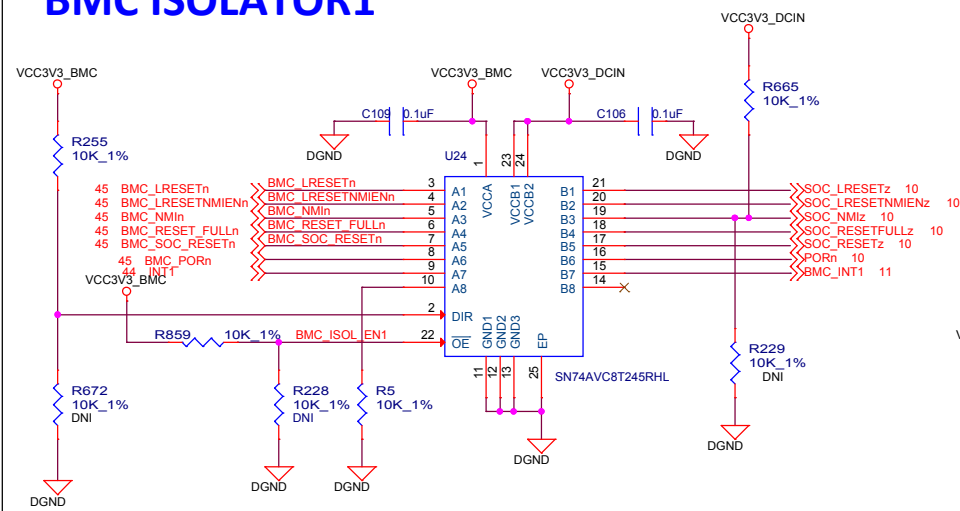
BMC LCD 3V GENERATOR



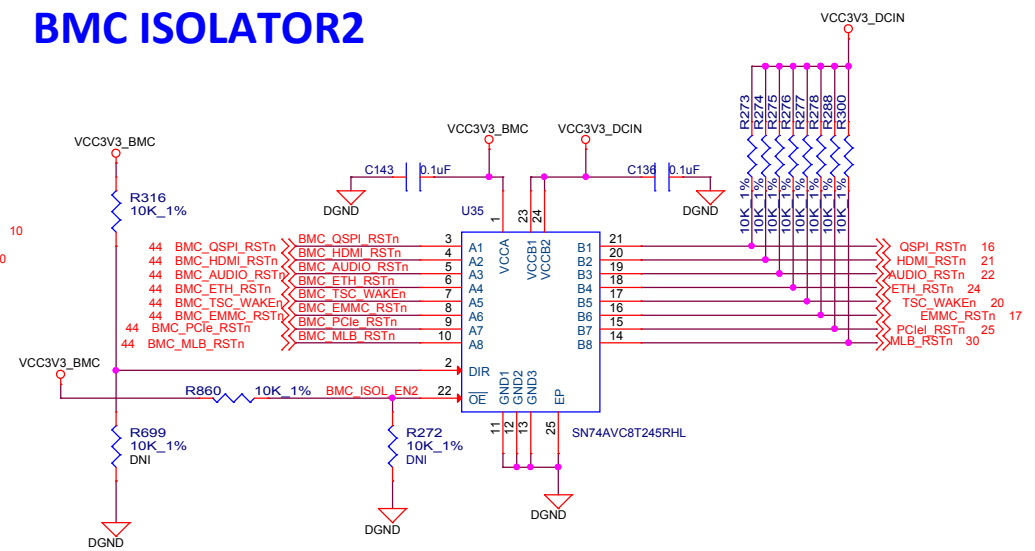
BMC POWER



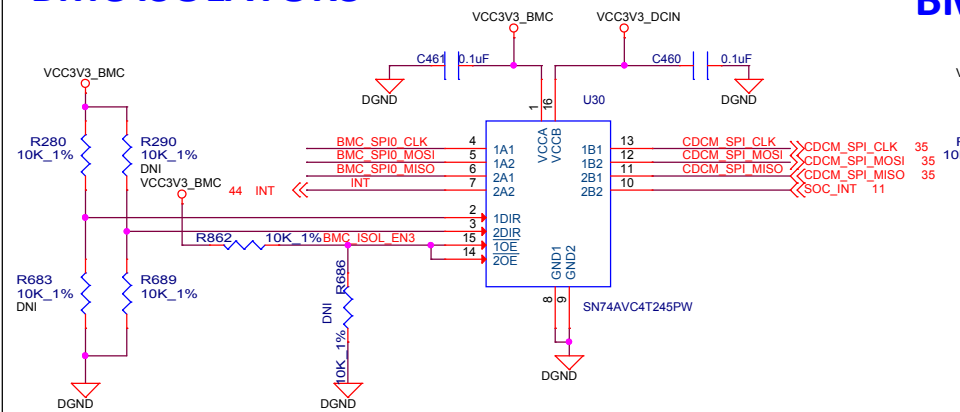
BMC ISOLATOR1



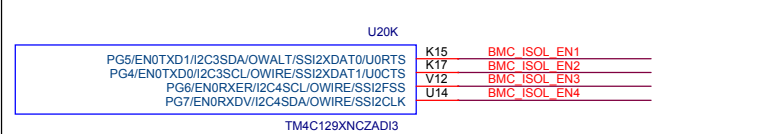
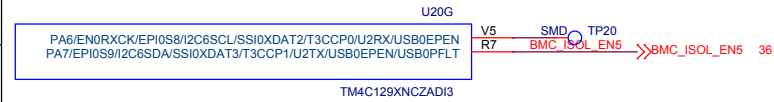
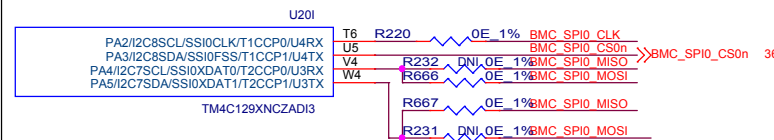
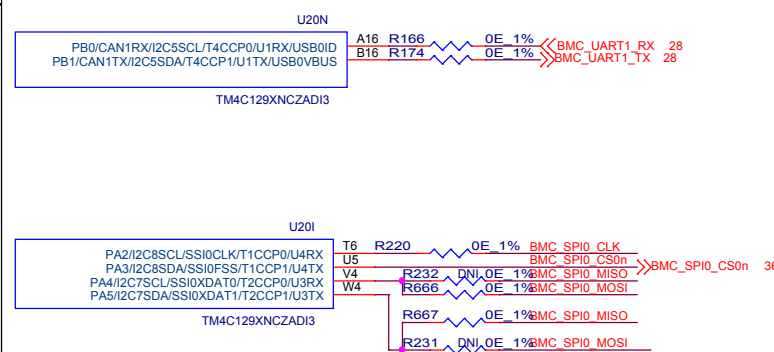
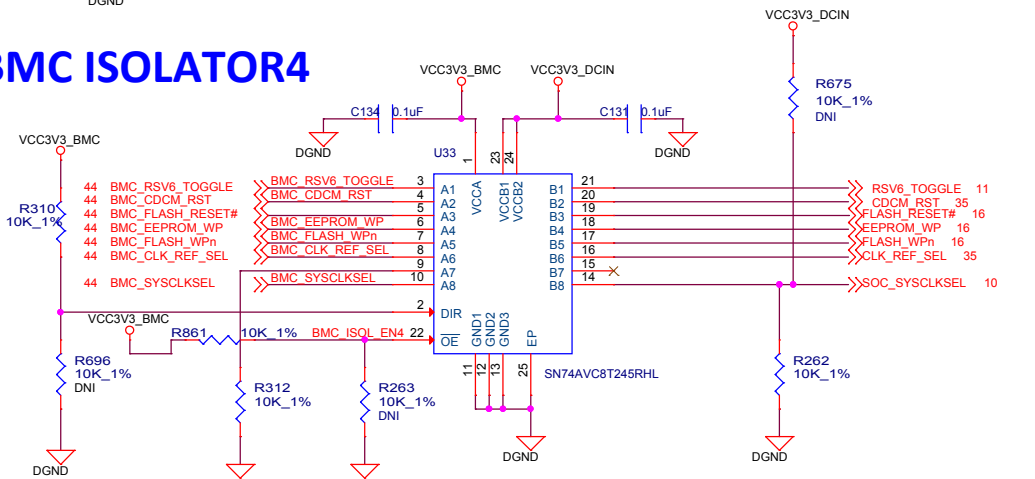
BMC ISOLATOR2



BMC ISOLATOR3

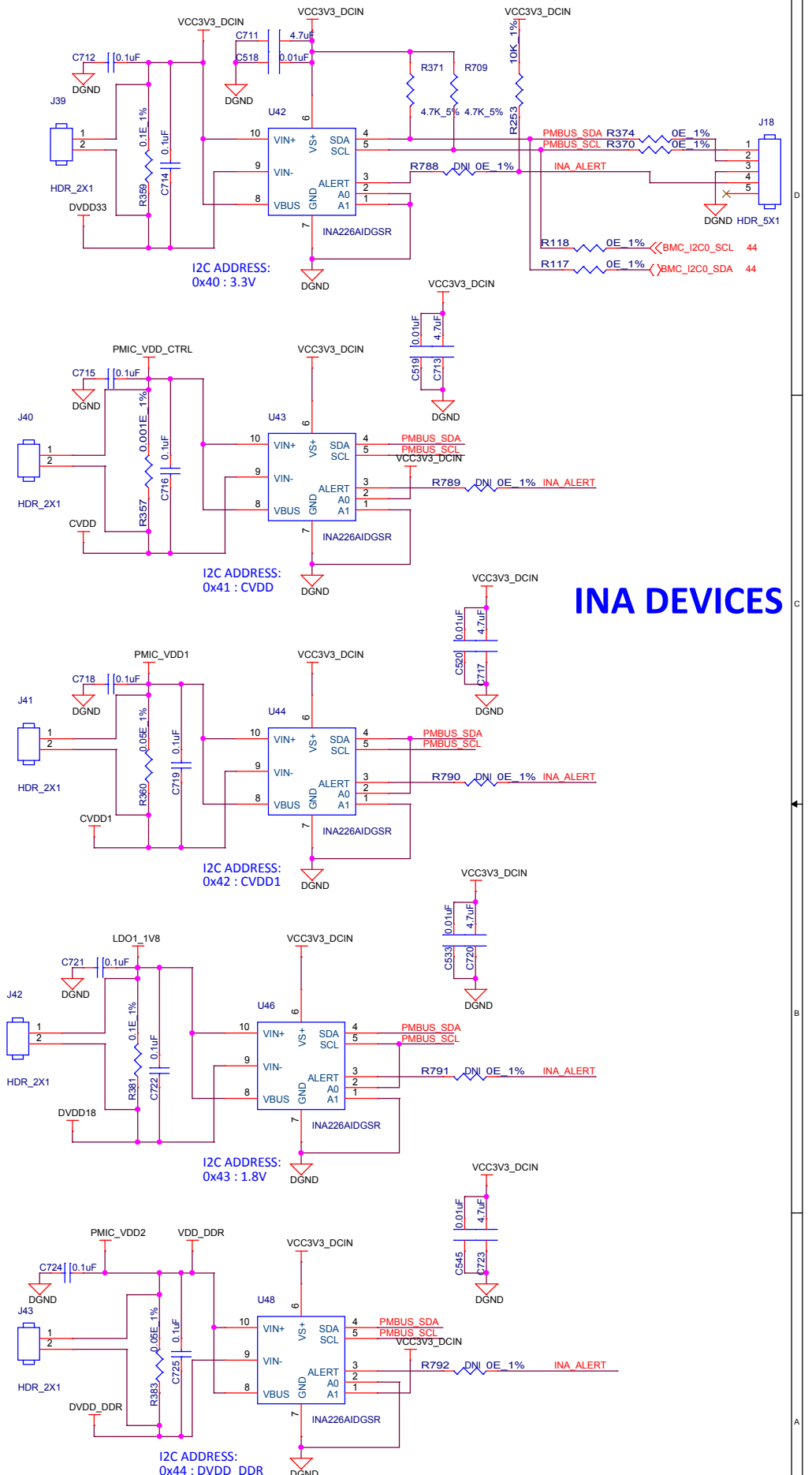
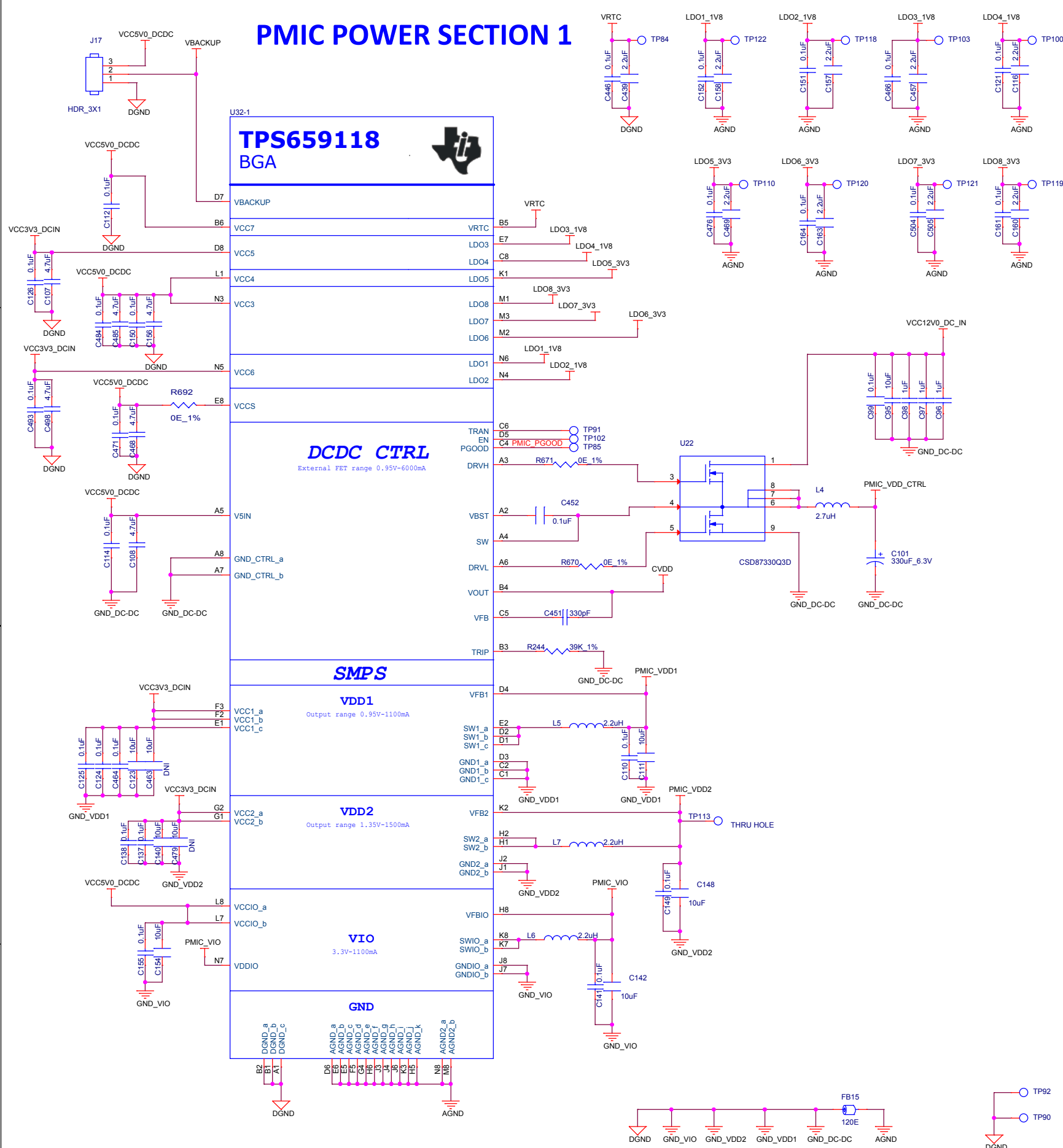


BMC ISOLATOR4



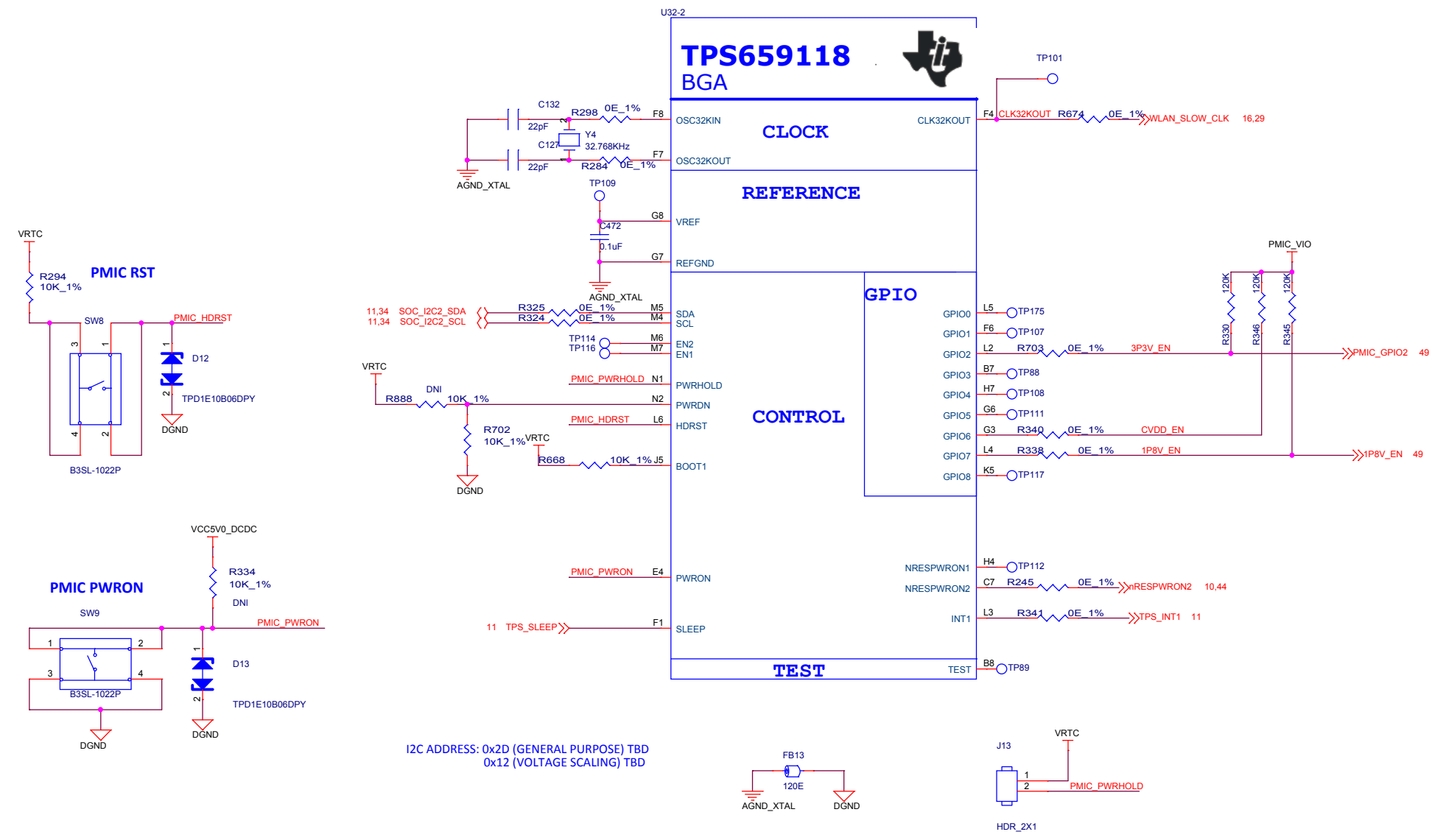
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K2G EVM		Size	Document Number	Rev
		C	MS_TI_K2GEVM_SCH_REVD	
Date:	Wednesday, April 13, 2016	Sheet	46	of 50

PMIC POWER SECTION 1

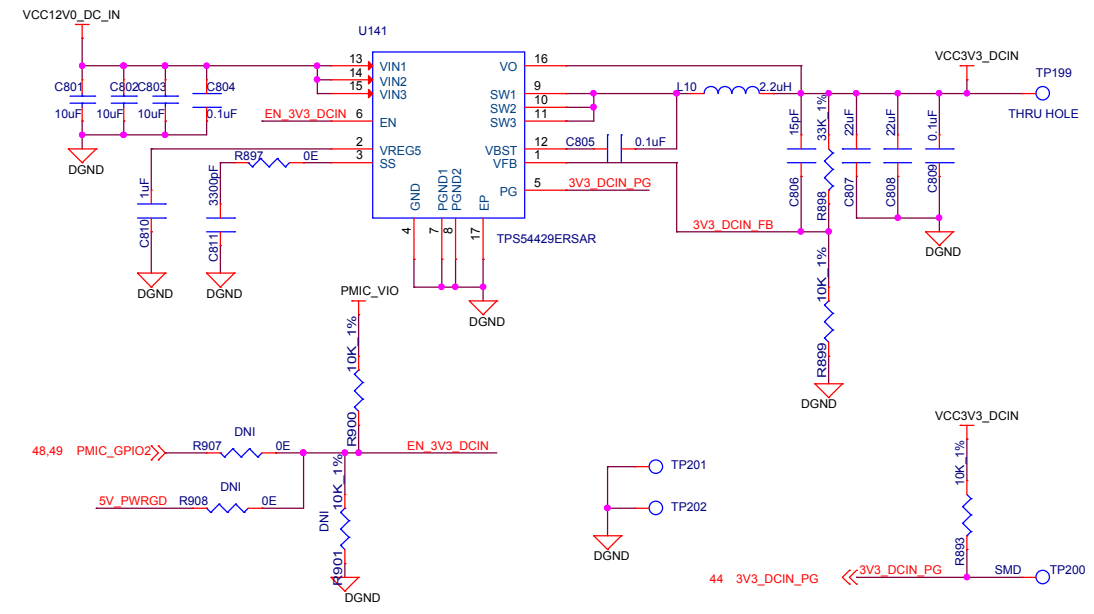


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title : PMIC POWER CIRCUIT 1	
K2G EVM		Size : Document Number	Rev
		C : MS_TI_K2GEVM_SCH_REV D	D
Date : Wednesday, April 13, 2016		Sheet 47 of 50	

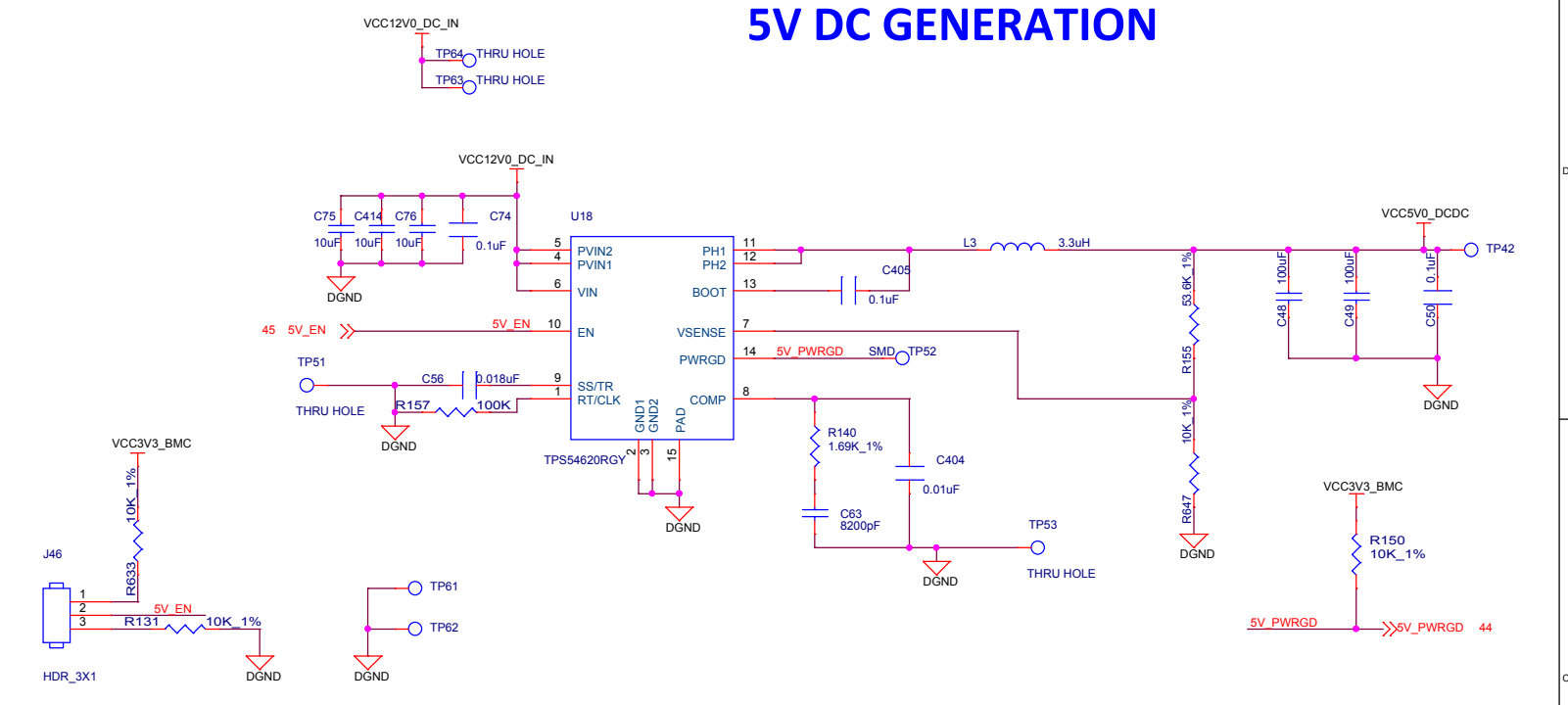
PMIC POWER SECTION 2



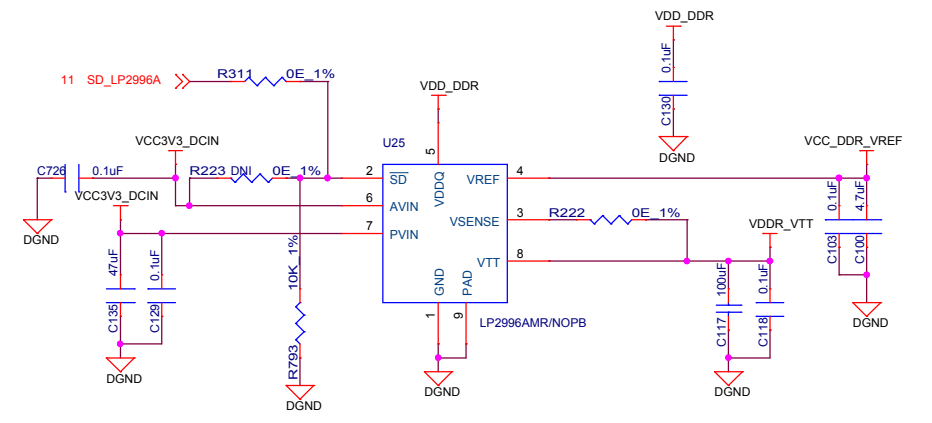
3.3V DC



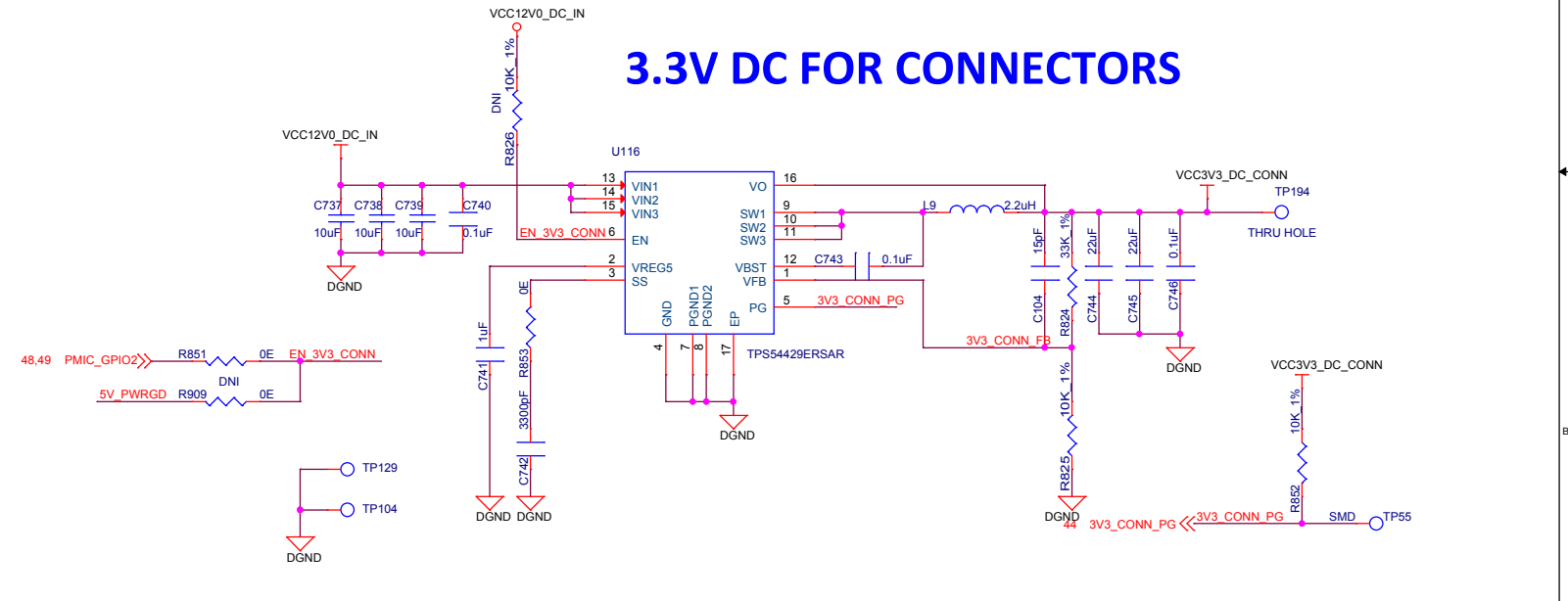
5V DC GENERATION



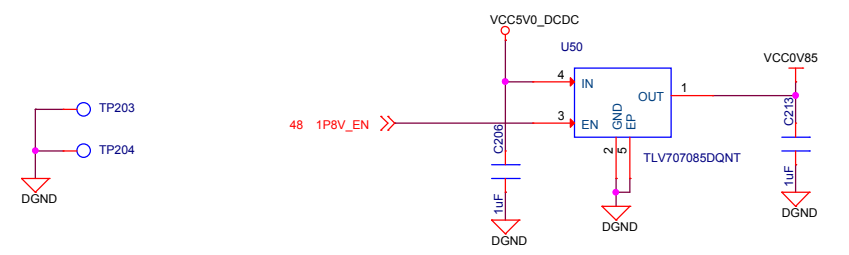
DDR VTT & VREF GENERATION



3.3V DC FOR CONNECTORS

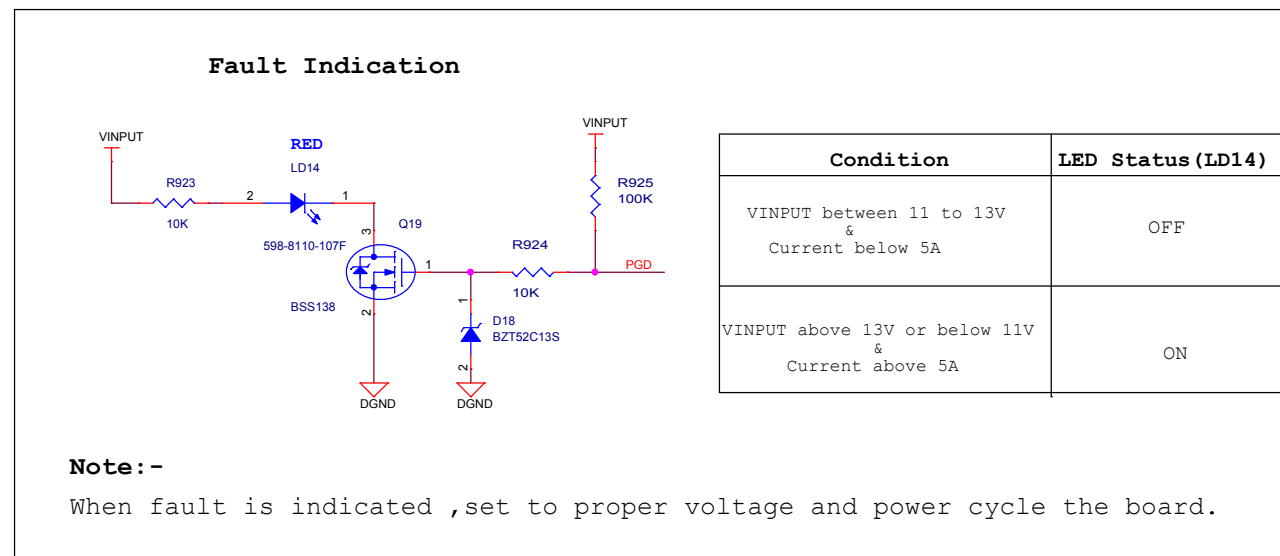
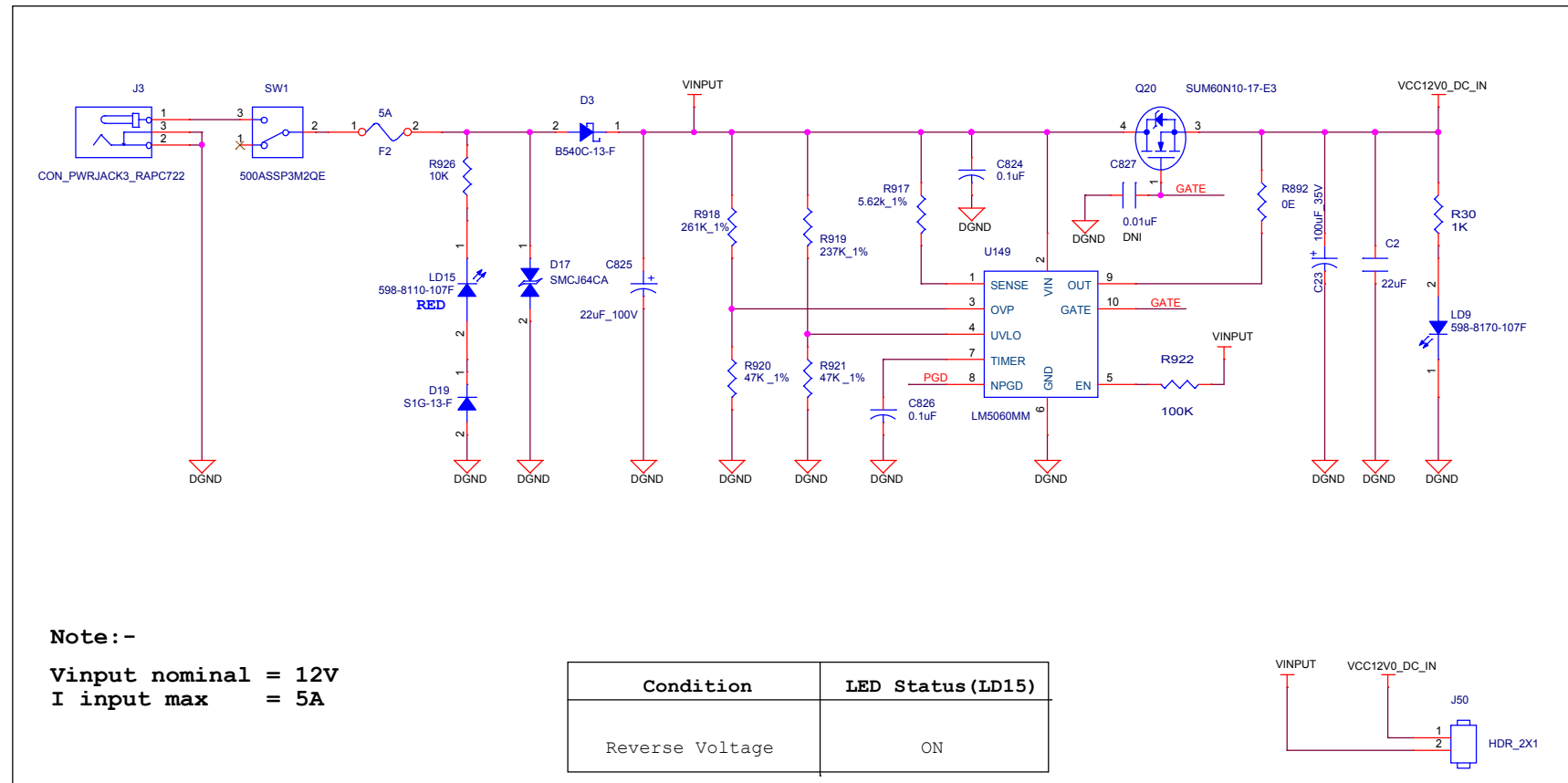


0.85V OPTIONAL LDO FOR PCIE & USB MODULES



Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title	DDR3L POWER
K2G EVM	 	Size	Document Number
		C	MS_TI_K2GEVM_SCH_REV D
		Date:	Wednesday, April 13, 2016
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OVER VOLTAGE PROTECTION CIRCUIT



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