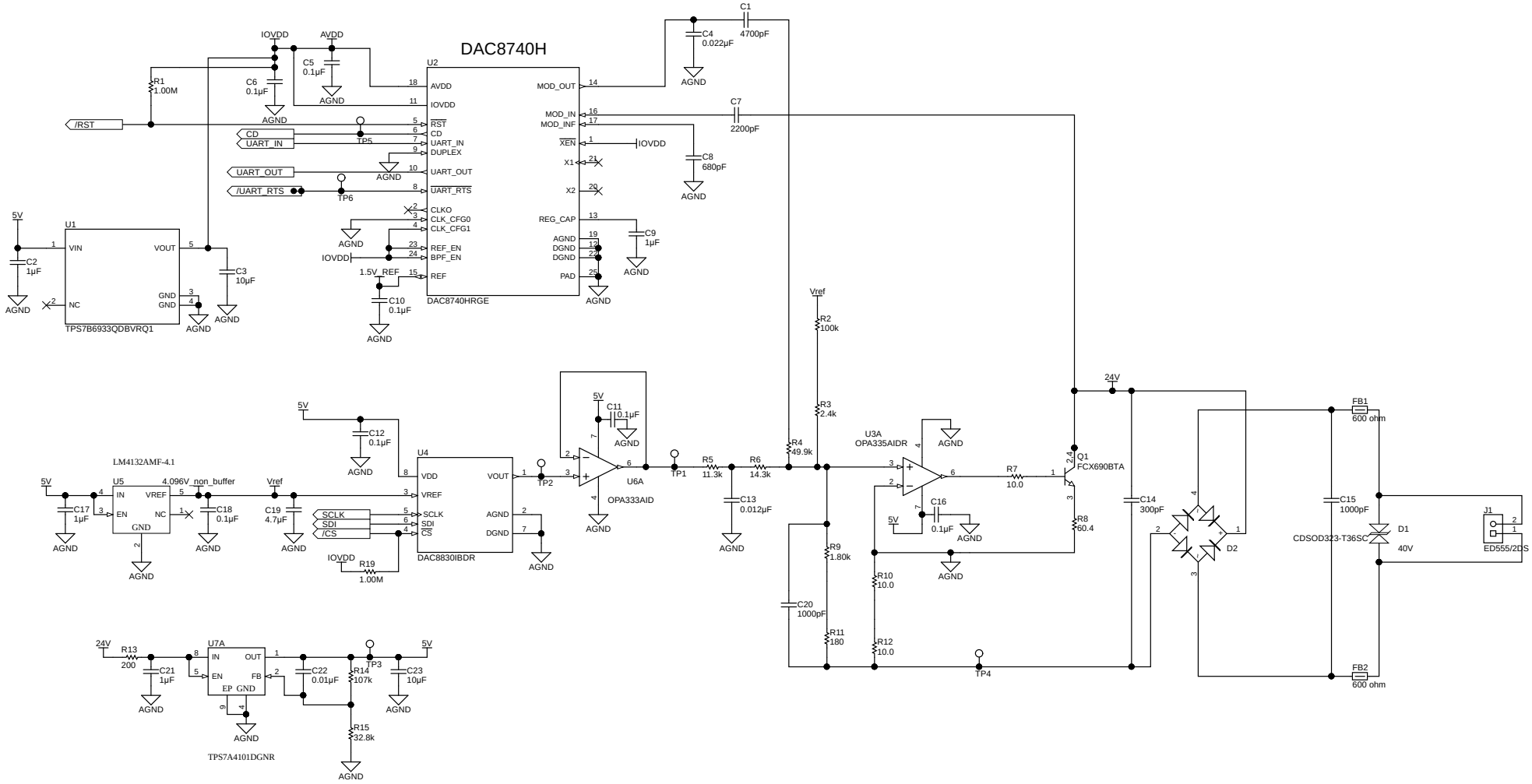
TIDA01504 - Highly Accurate, Loop-Powered 4-20mA Field Transmitter with DAC8740H HART Modem



Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 12/7/2017
TID #: N/A		Project Title: TIDA01504	
Number: TIDA01504	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 1 of 3
Drawn By:		File: DAC8740HTIPD_Sch1.SchDoc	Size: B
Engineer: Matthew Sauceda		Contact: http://www.ti.com/support	

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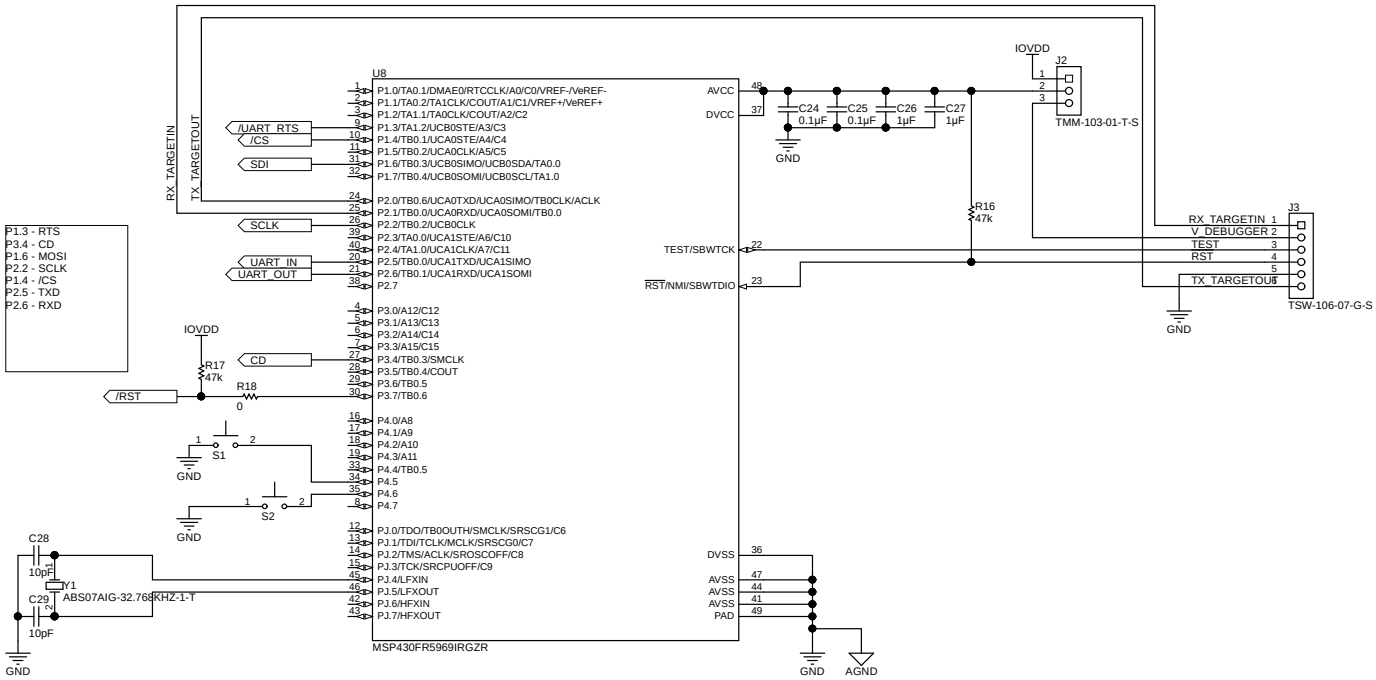

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 3/28/2017
TID #: N/A		Project Title: TIDA01504	
Number: TIDA01504	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 2 of 3
Drawn By:		File: DAC8740HTIPD_Sch2.SchDoc	Size: B
Engineer: Matthew Sauceda		Contact: http://www.ti.com/support	

H9
SJ-5303 (CLEAR)

H10
SJ-5303 (CLEAR)

H11
SJ-5303 (CLEAR)

H12
SJ-5303 (CLEAR)

FID1 FID2 FID3

PCB Number: TIDA01504
PCB Rev: E1

PCB
LOGO
Texas Instruments

PCB
LOGO
Pb-Free Symbol

PCB
LOGO
FCC disclaimer

You should delete the nylon screws/standoffs and/or the bumpons as needed for your design (or substitute other parts from Hardware.IntLib). Bumpons are cheaper, but provide less clearance.

Deleting anything else from this page may result in your EVM submission being rejected (until you add them back).

Update the Label Text in the Label Table as needed for each Assembly Variant.

You should delete this note too.

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 3/24/2017
TID #: N/A		Project Title: TIDA01504	
Number: TIDA01504	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 3 of 3
Drawn By:		File: PCB_Project_EVM_Hardware.SchDoc	Size: B
Engineer: Matthew Sauceda		Contact: http://www.ti.com/support	

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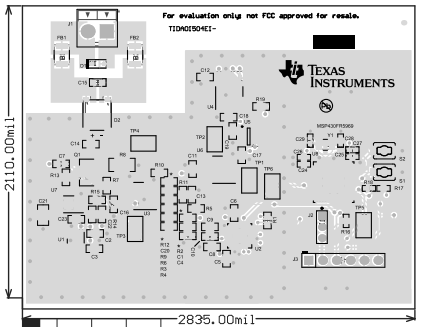
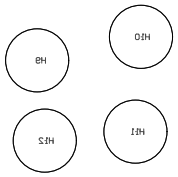
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4	59.20mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.





COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:	TIDA01504
DESIGNED FOR:	Public Release
FILE NAME:	DAC8740HTIPD_PCB.PcbDoc
ENGINEER:	Matthew Sauceda
LAYOUT BY:	Matthew Sauceda
SCALE:	1.00
ALTIUM DESIGNER VERSION:	17.1.5.472

ALL [illegible]		BOARD #: TIDA01504	REV: E1	[illegible]	
LAYER NAME = [illegible]		TID #: N/A	TID #:		
PLOT NAME: [illegible]	Composite Drill	GENERATED :: 12/27/2017	11:18:29 AM	Composite Layer	TEXAS INSTRUMENTS

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