Test Report: PMP20967

Adjustable Dual-Level Constant-Current Load Reference Design For Transient Testing

Description

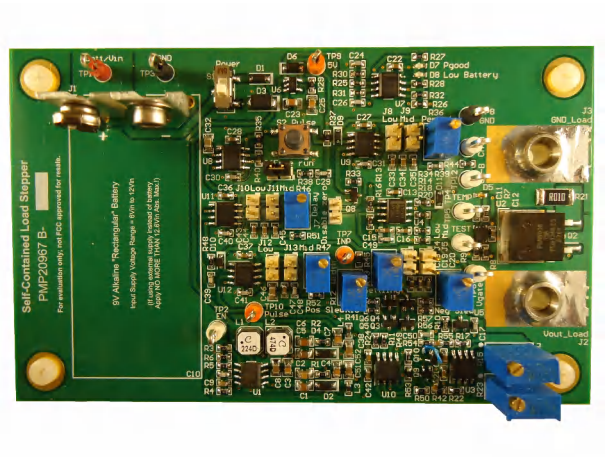
This adjustable dual-level constant-current load reference design helps engineers test a power supply output load transient response with special features and easy operation. The board provides load transient adjustments for low and high level, with slew rates as high as 100 A/µs. Timing adjustments such as period, delay, and pulse width are also designed into the board.

Features

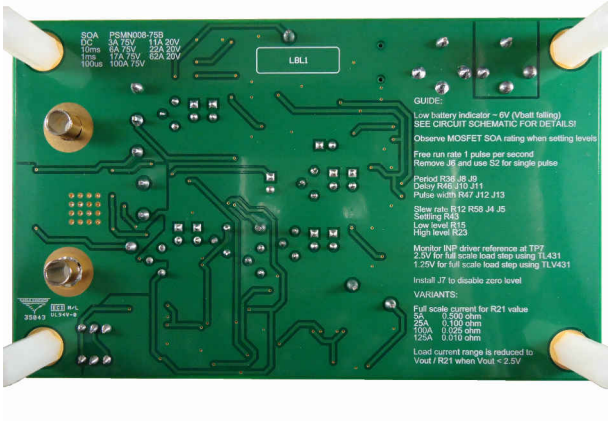
- Easily-adjustable load transient parameters
- Slew rates as high as 100 A/µs
- Settling time adjustment to minimize overshoot and oscillations
- Achieve a variety of power levels with a few easy component modifications
- Can be powered off of a regular 9-V battery
- Low battery charge monitoring
- Temperature monitoring and shutdown

Applications

- Programmable DC electronic load



Front of PMP20967



Back of PMP20967

1 Design Variants

The PMP20967 load step board can be changed into different models varying in output rated voltages and current. Table 1-1 shows the variants as well as the different components necessary for the specific model.

Table 1-1. PMP20967 Variant Specifications and Components

I_{OUT}	V_{OUT}	R21	R13	U5	Q2
5 A	100 V	0.500 Ω	32.4 kΩ	TL431	PSMN035-150B
25 A	100 V	0.100 Ω	16.2 kΩ	TL431	PSMN035-150B
100 A	100 V	0.025 Ω	8.06 kΩ	TL431	PSMN035-150B
125 A	50 V	0.010 Ω	4.02 kΩ	TLV431	PSMN008-75B
12.5 A	50 V	0.100 Ω	16.2 kΩ	TLV431	PSMN008-75B

2 Design Overview

This section provides an overview of each board function along with a description of the connectors and user interface for making load step adjustments.

2.1 Board Contents

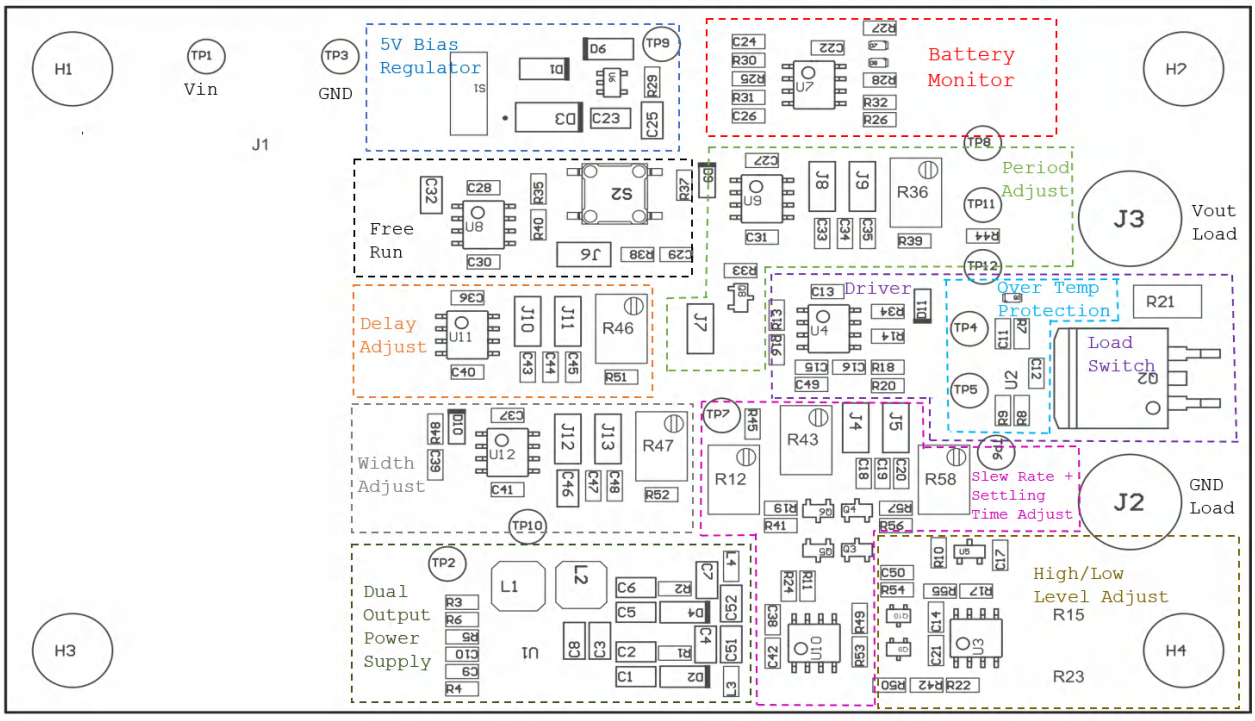


Figure 2-1. Board Subcircuits

The board consists of the following subcircuits:

- A dual output power supply to provide power for the pulse shaping and driver circuits
- A 5-V bias regulator to provide power for the timing circuits
- A battery monitor with status LEDs to indicate good or low battery
- An overtemperature protection circuit that provides thermal shutdown
- A driver and load switch circuit for the load transient
- A pulse shaping circuit that adjusts the low and high level of the load transient as well as the slew rate and settling time
- Timing circuits that set the period, delay, and pulse width adjustments

2.2 Connector Description

This section provides descriptions of the connectors:

- **J1** is the input power supply terminal that connects to a standard 9-V alkaline *rectangular* battery. Another option is to use a bench DC power supply that can be connected with hook test clips to **Vbatt_Vin (TP1)** and **GND (TP3)**.
- **Vout_Load (J2)** and **GND_Load (J3)** are the output load terminals that provide the load transient. Use standard banana jacks to connect to the load step board, or solder wires onto the pads for short connections and reduced inductance.

2.3 User Interface

2.3.1 Switches and Push-buttons

This section describes the switches and push-buttons:

- **Power (S1)** is a switch to enable or disable power to the load step board.
- **Pulse (S2)** is a push-button that triggers the timing circuits and sends an output pulse signal to create a load transient.

2.3.2 Jumpers

This section describes the jumpers:

- **Free run (J6)** enables a free running pulse signal of 1 Hz when installed. The pulse signal triggers circuits necessary for a load transient.
- **Disable zero (J7)** disables the zero-level step during a load transient when installed. The load stays at the adjusted low level until the next cycle.
- **Low (J4)** and **Mid (J5)** set ranges of the slew rate adjust. The default setting when both jumpers are open sets the fastest slew rate.
- **Low (J8)** and **Mid (J9)** set ranges of the period adjustments. The default setting when both jumpers are open sets the shortest period.
- **Low (J10)** and **Mid (J11)** set ranges of the delay adjustments. The default setting when both jumpers are open sets the shortest delay.
- **Low (J12)** and **Mid (J13)** set ranges of the pulse width adjustments. The default setting when both jumpers are open sets the shortest pulse width.

2.3.3 Potentiometers

This section describes the jumpers:

- **Low (R15)** is the low-level adjustment of the load transient. Turning the potentiometer clockwise raises the low level.
- **High (R23)** is the high-level adjustment of the load transient. Turning the potentiometer clockwise raises the high level.
- **Pos Slew (R12)** is the positive slew rate adjustment. Turning the potentiometer clockwise increases the rising transition time.
- **Neg Slew (R58)** is the negative slew rate adjustment. Turning the potentiometer clockwise increases the falling transition time.
- **Settling (R43)** is the settling time adjust. Turning the potentiometer clockwise dampens the oscillations by increasing the time required for the transition to settle to a steady state value.
- **Width (R47)** is the pulse width adjustment of the high level. Turning the potentiometer clockwise increases the pulse width.
- **Delay (R46)** is the delay adjustment of the high level relative to the period. Turning the potentiometer clockwise increases the delay time.
- **Period (R36)** is the period adjustment of the low level. Turning the potentiometer clockwise increases the period.

2.4 Functional Block Diagram

The images in this section provide various functional block diagrams.

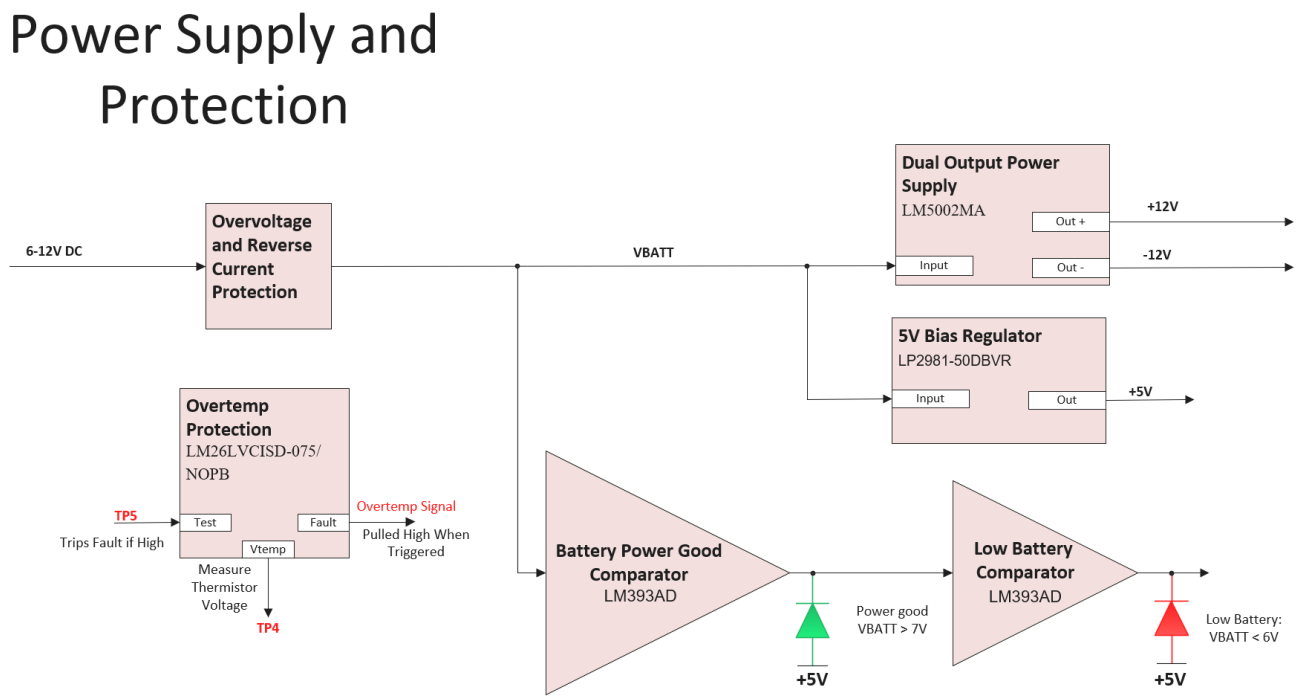


Figure 2-2. Power Supply and Protection

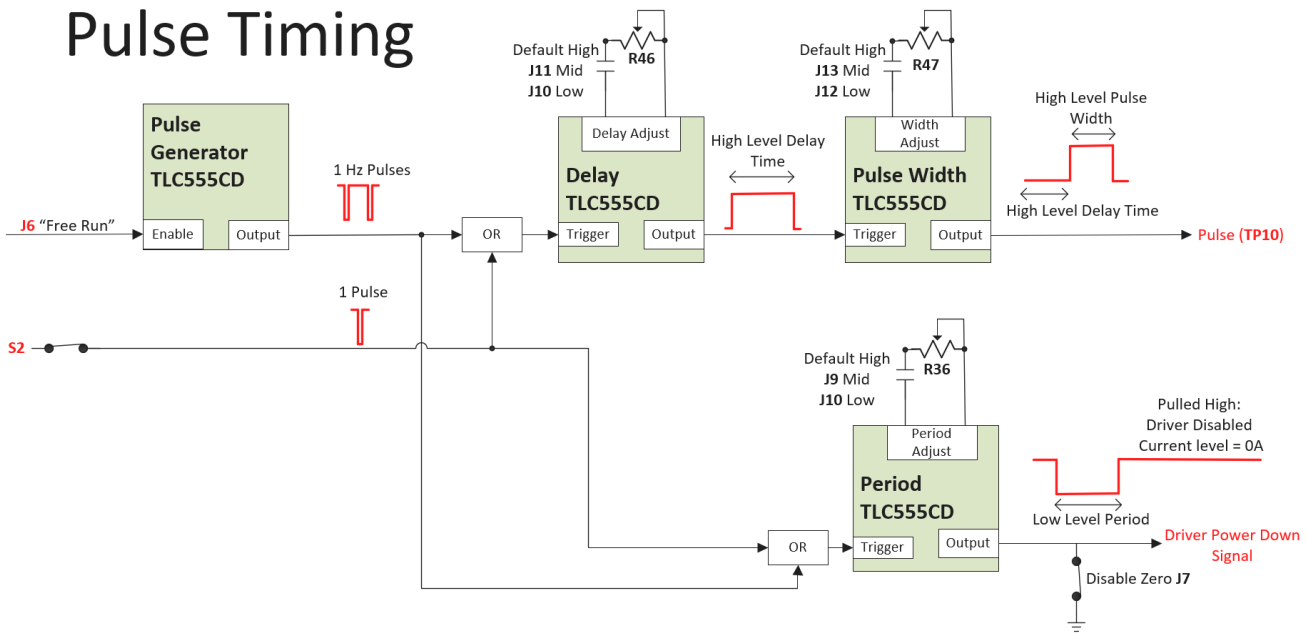


Figure 2-3. Pulse Timing

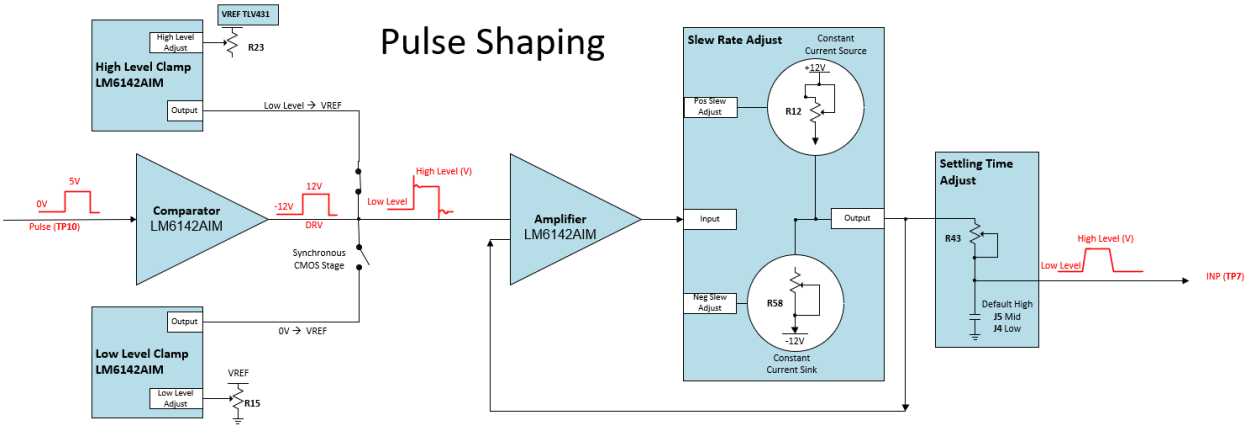


Figure 2-4. Pulse Shaping

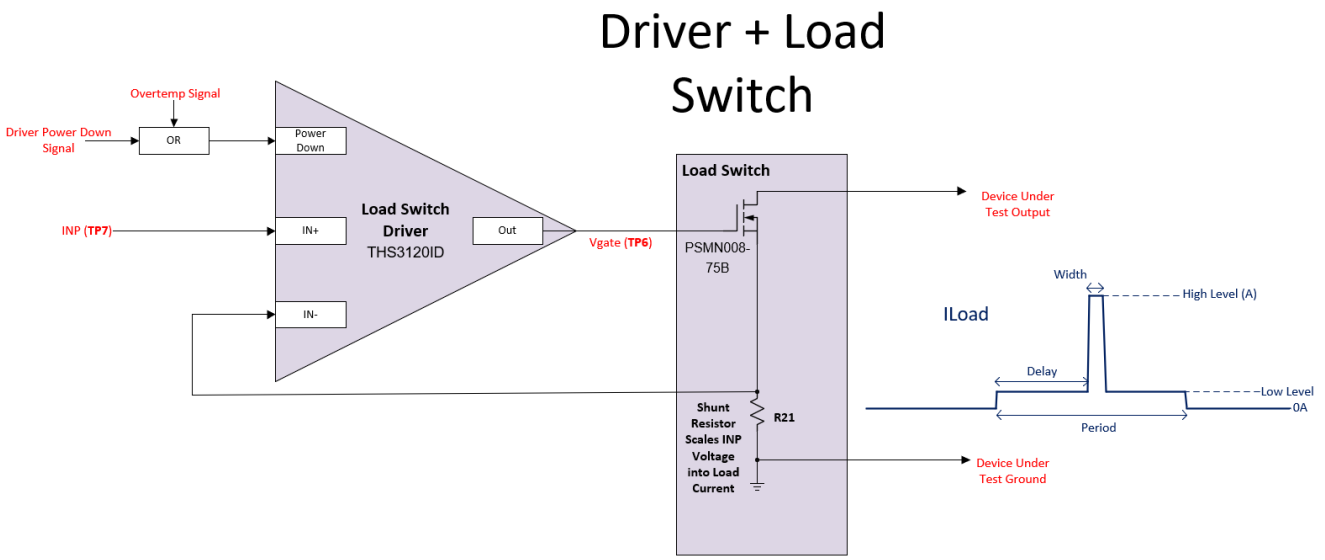


Figure 2-5. Driver and Load Switch

2.5 Functional Block Descriptions

This section describes the functional blocks in Figure 2-2 through Figure 2-5.

- **Power Supplies**

  Either a standard 9-V battery or a bench supply of 6 V to 12 V powers the board through switch S1. There is a reverse current and voltage clamping diode to protect the source. The input power feeds into a 5-V linear regulator for the pulse timing and protection features. There is also a switching regulator controlling SEPIC and Ćuk converters that share a coupled 1:1 inductor. This produces a dual output of +12 V and –12 V for pulse shaping and driving circuitry.

- **Overtemperature Protection**

  A factory preset temperature sensor with integrated comparator is used to deliver a shutdown signal to the load switch driver during an overtemperature event. There are test points for monitoring the thermistor voltage (TP4) and to simulate a fault (TP5). When the output is pulled high, the load switch driver is shut down.

- **Battery Monitoring**

  When the board is powered, an LED turns on to indicate battery voltage. Pgood (D7) is a green LED that indicates a good input supply. When Vbatt/Vin falls to 6 V, the Pgood LED turns off and the red LED, Low Battery (D8), turns on. When Vbatt/Vin rises to 7 V, the Low Battery LED turns off and the Pgood LED turns on.

- **Free Run Oscillator**

  This functions the same as pressing S2 every second to trigger the rest of the timing circuits. When J6 is connected, the output of U8 can now be pulled high or low depending on the voltage across capacitor C32. R35, R40, and C32 were chosen for short 1-Hz pulses pulled low to trigger the delay and period timers.

- **Period Adjust**

  This block enables or disables the driver to set the amount of time the load step current is non-zero for each 1-second interval. The free run or S2 pulse triggers the period 555 timer. When the period output is high, Q8 turns on and grounds the driver power-down signal which enables the driver to turn on. The amount of time the driver is enabled depends on the period RC time constant set by potentiometer R36 and caps C33–C35 (modified by jumpers J8, J9). When *Disable Zero* J7 is installed, the driver power down signal is always grounded and the driver is always enabled.

- **Delay Adjust**

  Delay is important to allow time for the low-level period to be set before the high-level pulse to correctly shape the load step reference. The free run or S2 pulse triggers the delay 555 timer to pull the delay output high. The amount of time the delay output is high depends on the delay RC time constant set by potentiometer R46 and caps C43–C45 (modified by jumpers J10, J11).

- **Pulse Width Adjust**

  This block determines the amount of time the load step board draws the high-level current. After the delay output falls low, the pulse width output gets pulled high. The amount of time the pulse output is high depends on the pulse width RC time constant set by potentiometer R47 and capacitors C46–C48 (modified by jumpers J12, J13). The Pulse (TP10) signal is then fed into the shaping portion of the board.

- **High- or Low-Level Current Adjust**

  A reference voltage U5 is connected between ground by two potentiometers where the center tap of each sets a voltage at the inputs of a dual op amp. The way the potentiometers are connected makes it such that the high-level minimum voltage is the same as the set low-level voltage, which ranges between 0 and Vref. The op-amp outputs are tied to complimentary NFET and PFET switches driven by an amplified and level-shifted version of the Pulse signal (TP10) called DRV. The end result is a scaled version of Pulse (TP10) ranging from the low-level to high-level voltages.

- **Slew Rate and Settling Time Adjust**

  To avoid overshoot and high-frequency ringing in the load step, this function slows down the slew rate of the reference voltage pulse and passes the pulse through a low-pass filter to get our INP reference for the driver (TP7). The settling time is controlled by modifying the RC time constant of the low-pass filter consisting of potentiometer R43 and capacitors C18–C20 (modified by jumpers J4, J5).

  To slow the slew rate, the available charging and discharging current of C18–C20 is decreased by using 2 independent current mirrors to control positive and negative slew rates separately.

  Q5 and Q6 form the positive slew control current mirror while Q3 and Q4 control the negative slew control current mirror. Increasing potentiometer R12 decreases the constant current source to charge C18–C20 on the rising edge of the pulse. Likewise, increasing potentiometer R58 decreases the constant current sink to discharge C18–C20 on the falling edge of the pulse.

- **Driver and Load Switch**

  Finally, the high bandwidth and low-noise load switch amplifier drives the gate of the load switch based on the INP (TP7) reference pulse. A current sense resistor R21 in the negative feedback trace scales the high- and low-level voltages of INP to high- and low-level currents for the load step. Additional filtering on the output of the amplifier determines the bandwidth limitation and R13 sets the amplifier gain for the gate drive. If the overtemperature or low-level period power down signals are pulled high, the driver shuts off the load switch and zero current is drawn.

3 Features and Performance Curves

This section highlights the features of the load step board. The scope plots show the performance of the features at their minimum and maximum end points.

3.1 Test Setup

Figure 3-1 shows the setup used to test each function of the board. A Chroma 62000P bench supply is used along with a capacitor bank consisting of six 470-µF aluminum capacitors to holdup the voltage. The capacitor bank is used to emulate a device under test (DUT). The capacitors represent the output filter of a typical power supply being tested.

The current probe used is the CP150 to avoid probe saturation for large load steps. Minimize the wiring inductive loop between the load step board and test device if high a slew rate (100 A/µs) is desired.

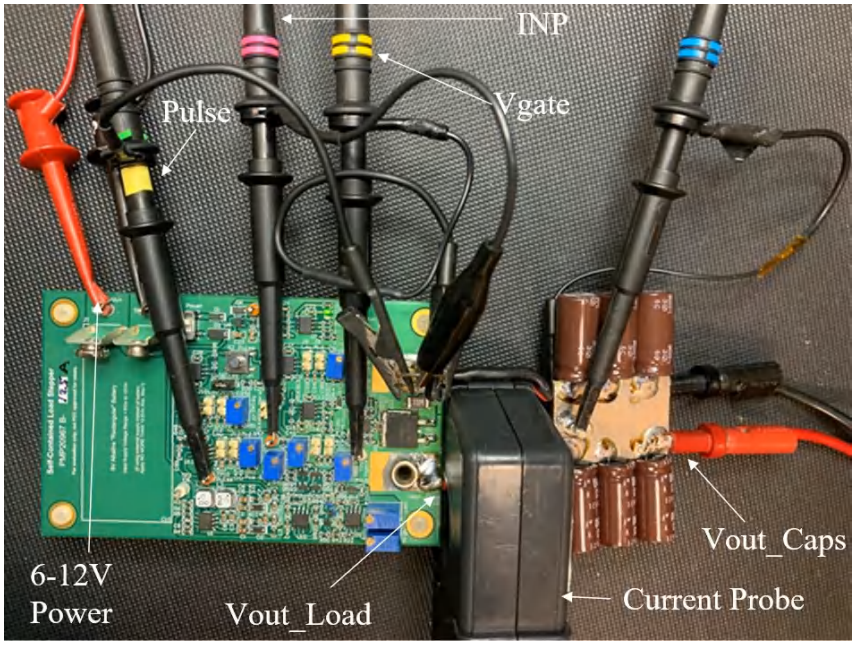


Figure 3-1. Setup for Testing the Load Step Board Using a Power Supply

Vout_Load is the drain-source voltage of Q2 which droops as the gate voltage increases and drain-source current rises. Minimize this voltage droop to keep Q2 out of saturation (see the limitations of wiring inductance and minimum voltage).

Measuring at the capacitor bank represents the response of the bench supply to the load step. The capture in Figure 3-2 shows the difference between the two output voltage measurements.

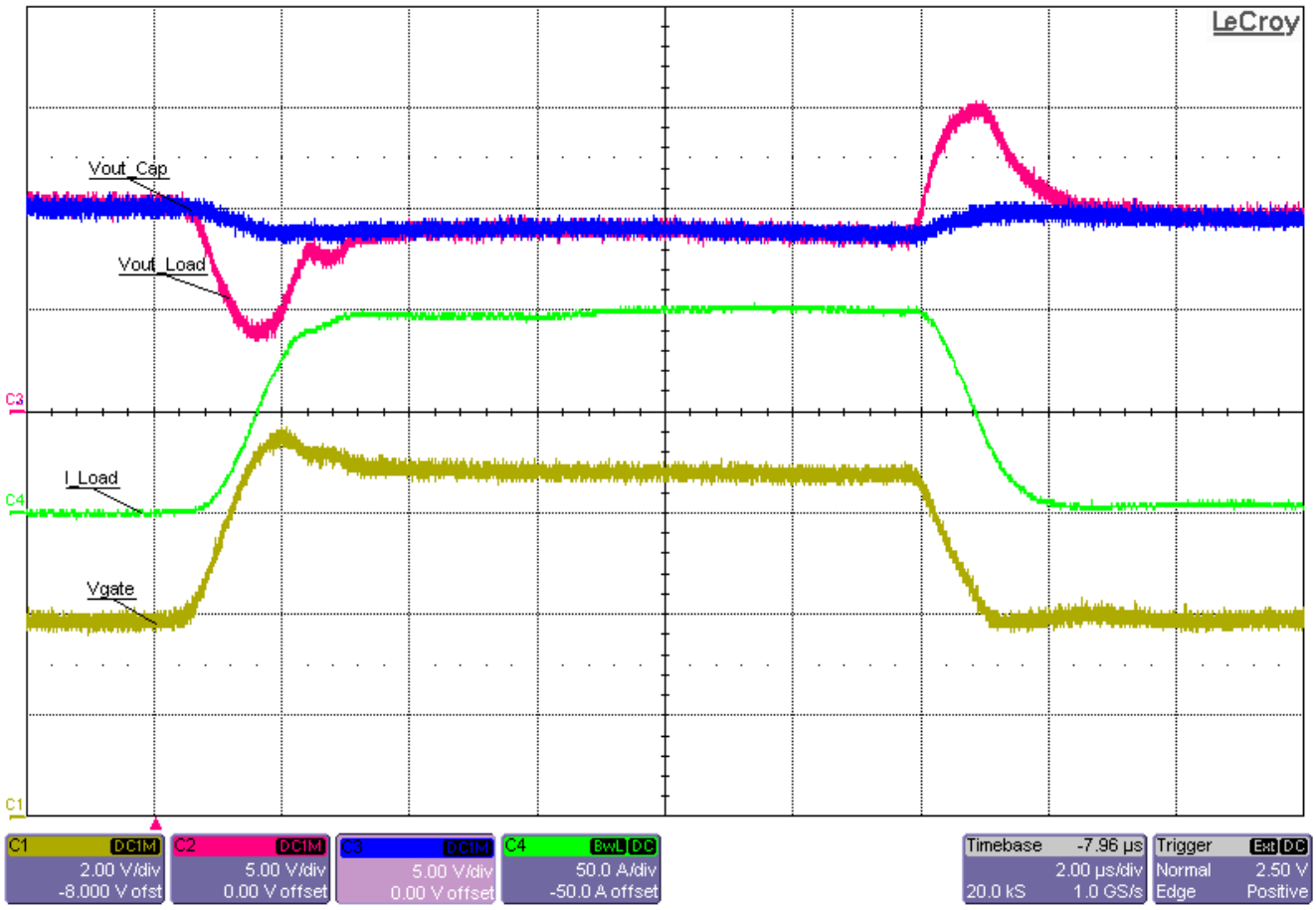


Figure 3-2. The Difference in Measuring Both Sides of the Capacitor Bank When Testing With the Chroma 62000p

When testing a converter, the Vout_Cap waveform depends on the control loop characteristics such as crossover frequency and phase margin. The load step requires a fast transition with respect to the converter bandwidth to fully exercise the control loop of the DUT.

Figure 3-3 shows the setup to test a converter using the PMP20967 load step board. A synchronous buck 12-V output reference design was used in this example. The output voltage response to the load step exhibits characteristics of a stable loop with a 15-kHz crossover frequency.

For best measurement accuracy of the output voltage response, a single voltage probe with ground at the DUT is used. A PCB coax probe connector with 50-Ω termination is used for this example.

Note

Avoid multiple ground connections between the load board and the device under test.

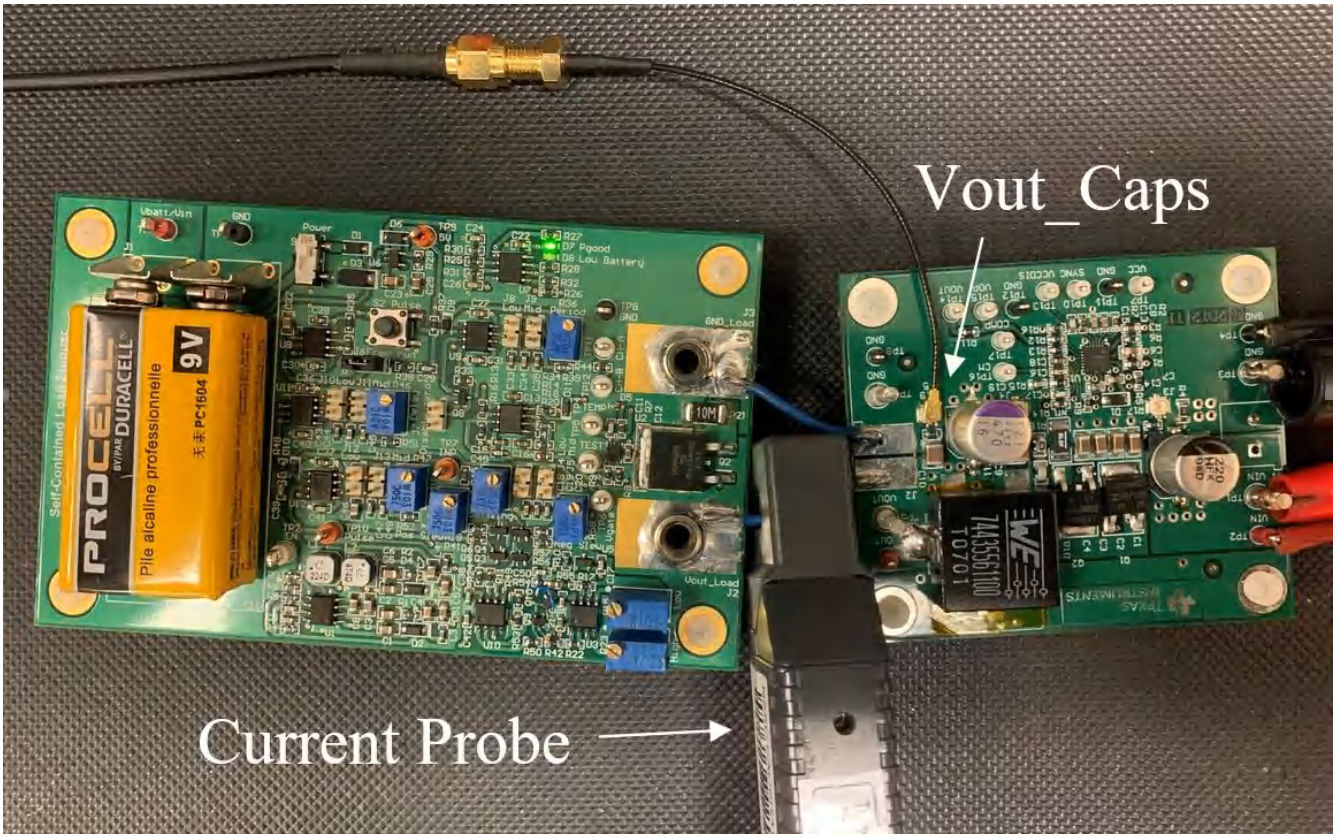


Figure 3-3. Setup for Using the Load Step Board With a Converter Under Test

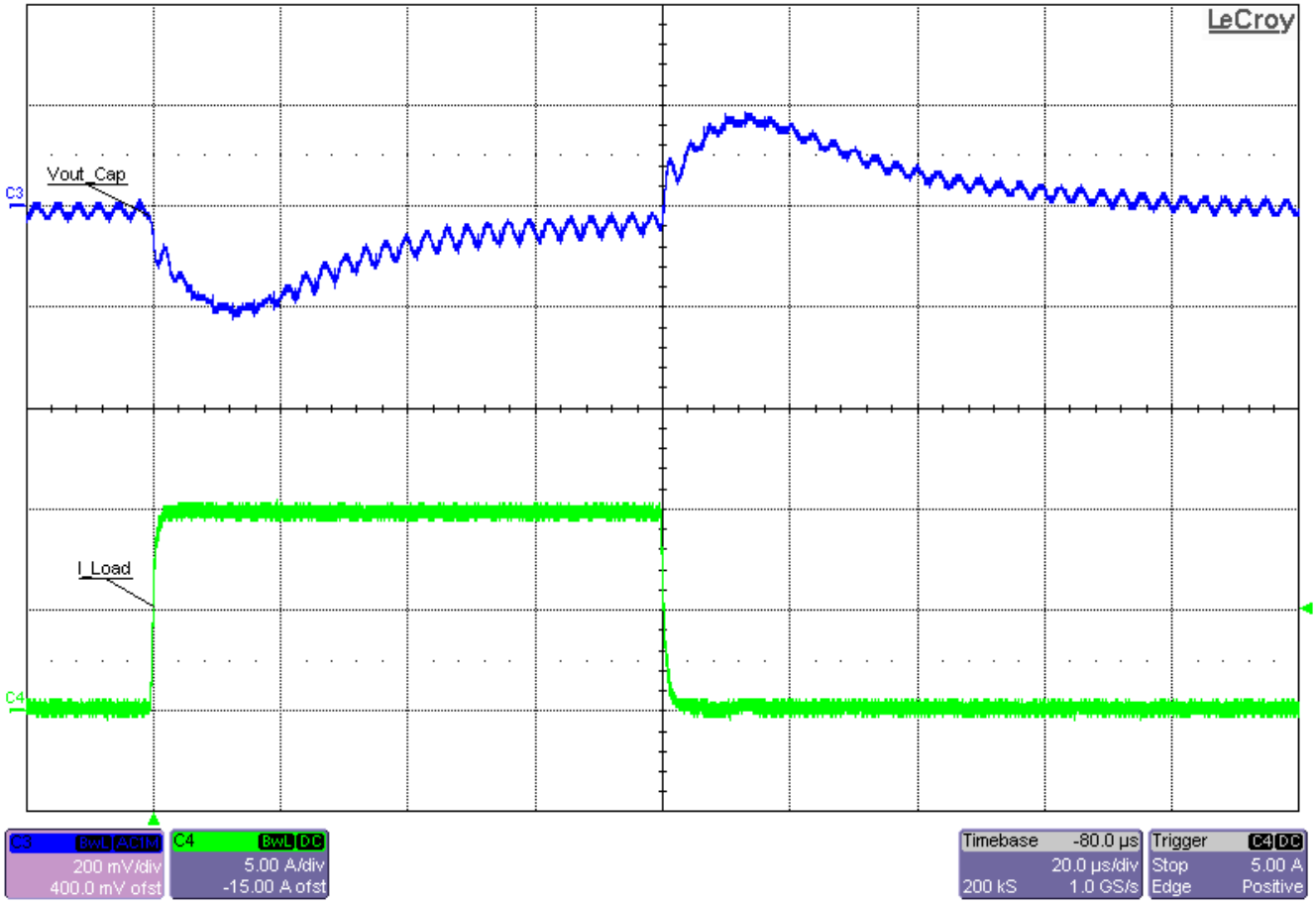


Figure 3-4. Load Transient Test on 12-V Output Synchronous Buck

3.2 Pulse

When the board is powered, a pulse signal is generated when **Pulse (S2)** is pushed, or **Free run (J6)** is installed. Monitor **Pulse (TP10)** to maintain normal operation. All further scope plots in this user's guide do trigger on the pulse signal, unless shown otherwise. The following scope plot shows the pulse signal.

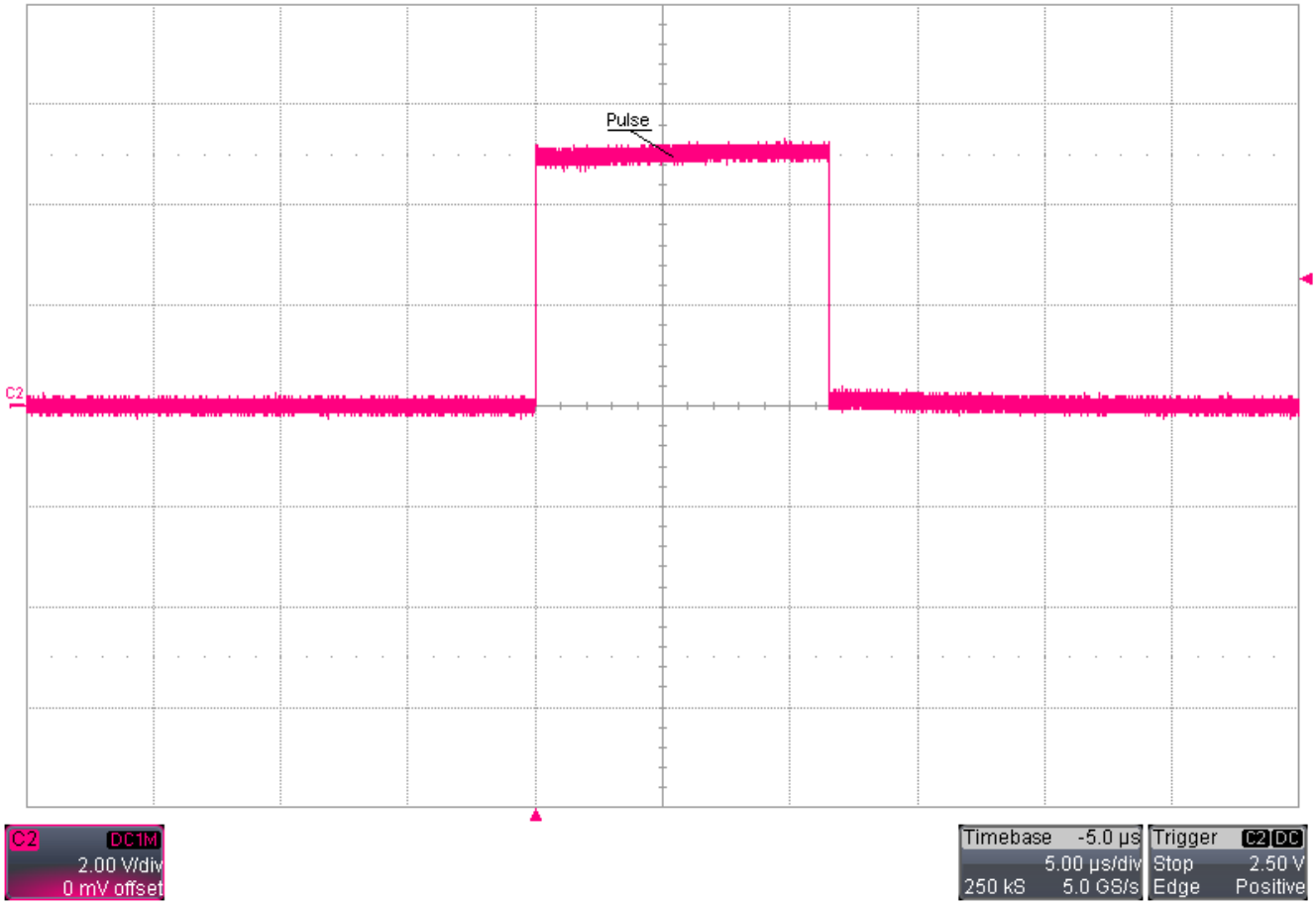


Figure 3-5. Measured Pulse Signal From TP10

3.3 Levels and Free Run

The load step board has three step levels: a low level, a high level, and a zero level. In one cycle, the board starts at the zero level, steps up to the low level, and then to the high level. Afterwards, the load steps down to the low level and then to the zero level, until the next cycle.

The following scope plot shows a load transient of 10 A to 25 A at a 10 V_{OUT} load. The low-level period is set for 14 ms, while the high-level pulse width is set for 4 ms. The results in the following waveform use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

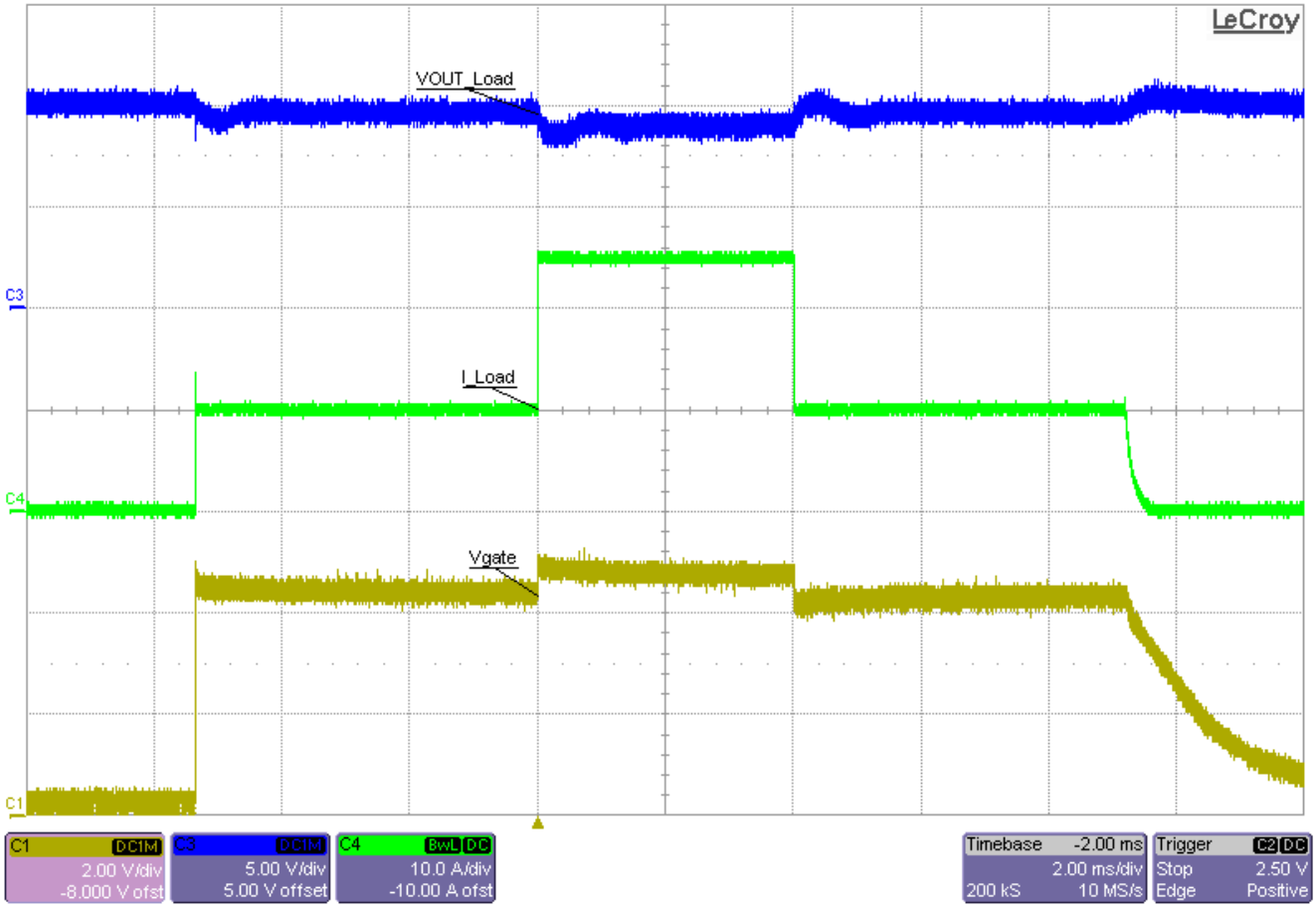


Figure 3-6. High-, Low-, Zero-Level Step, 10 A to 25 A, 10-V Output Load Transient

When the jumper, **Free Run (J6)**, is installed, a free running pulse signal of 1 Hz triggers the sub-circuits necessary for a load transient. The following scope plot shows two cycles generated by the free run. The transient is a 10-A to 25-A load step for a 10-V output load. The results in the following waveform use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

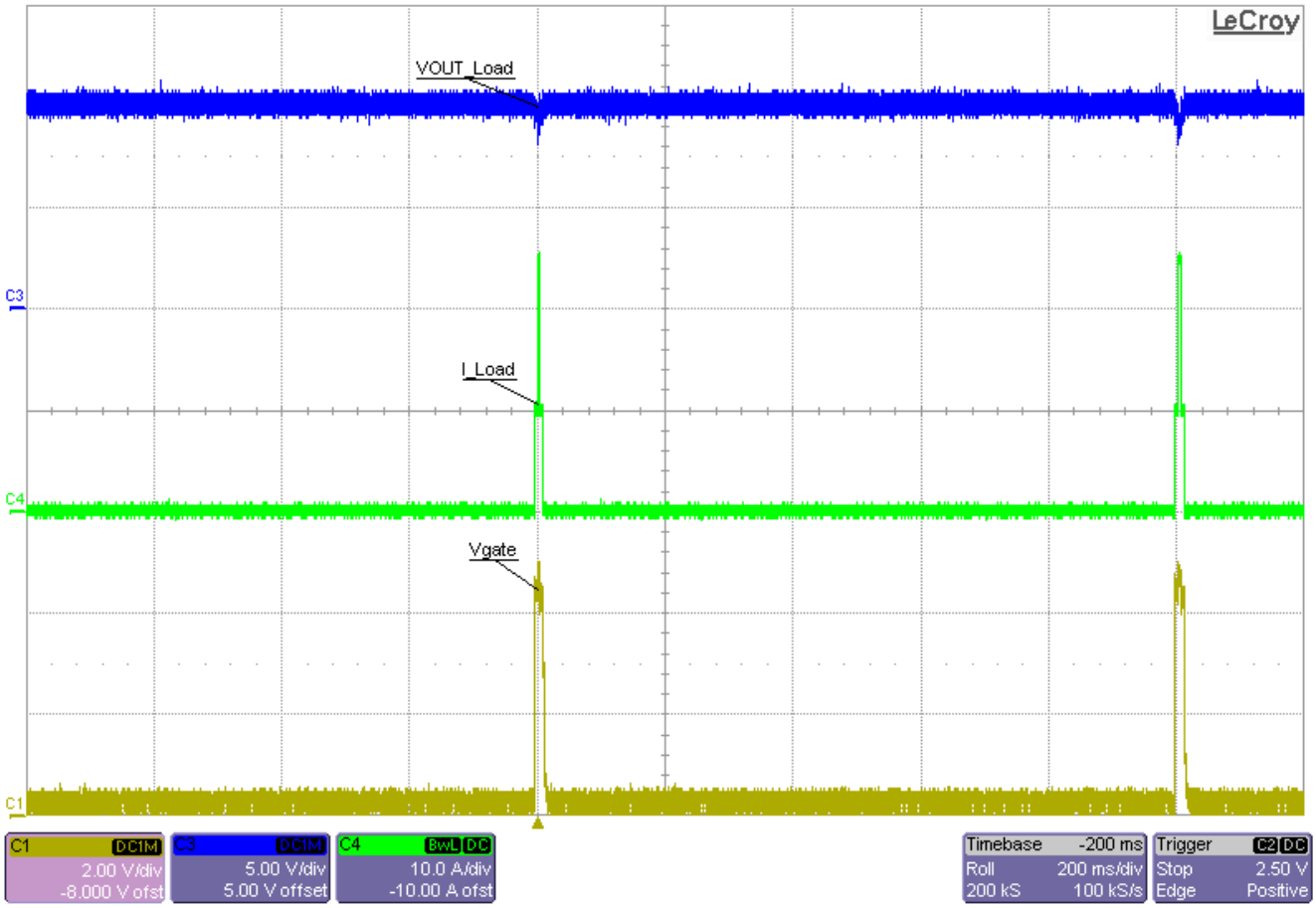


Figure 3-7. Free Run, 10 A to 25 A, 10-V_{OUT} Load Transient

When the jumper, **Disable Zero (J7),** is installed, the zero-level step is disabled during the load transient. The load stays at the adjusted low level until the next cycle. The following scope plot shows the load step board with the zero-level step disabled. The results in the following waveform use a PSMN008-75B MOSFET in the 125-A, 50-V variant. The zero-level is intended to keep the average power dissipation in Q2 within the safe operating area (SOA). Be sure to check the intended power through Q2 before installing J7.

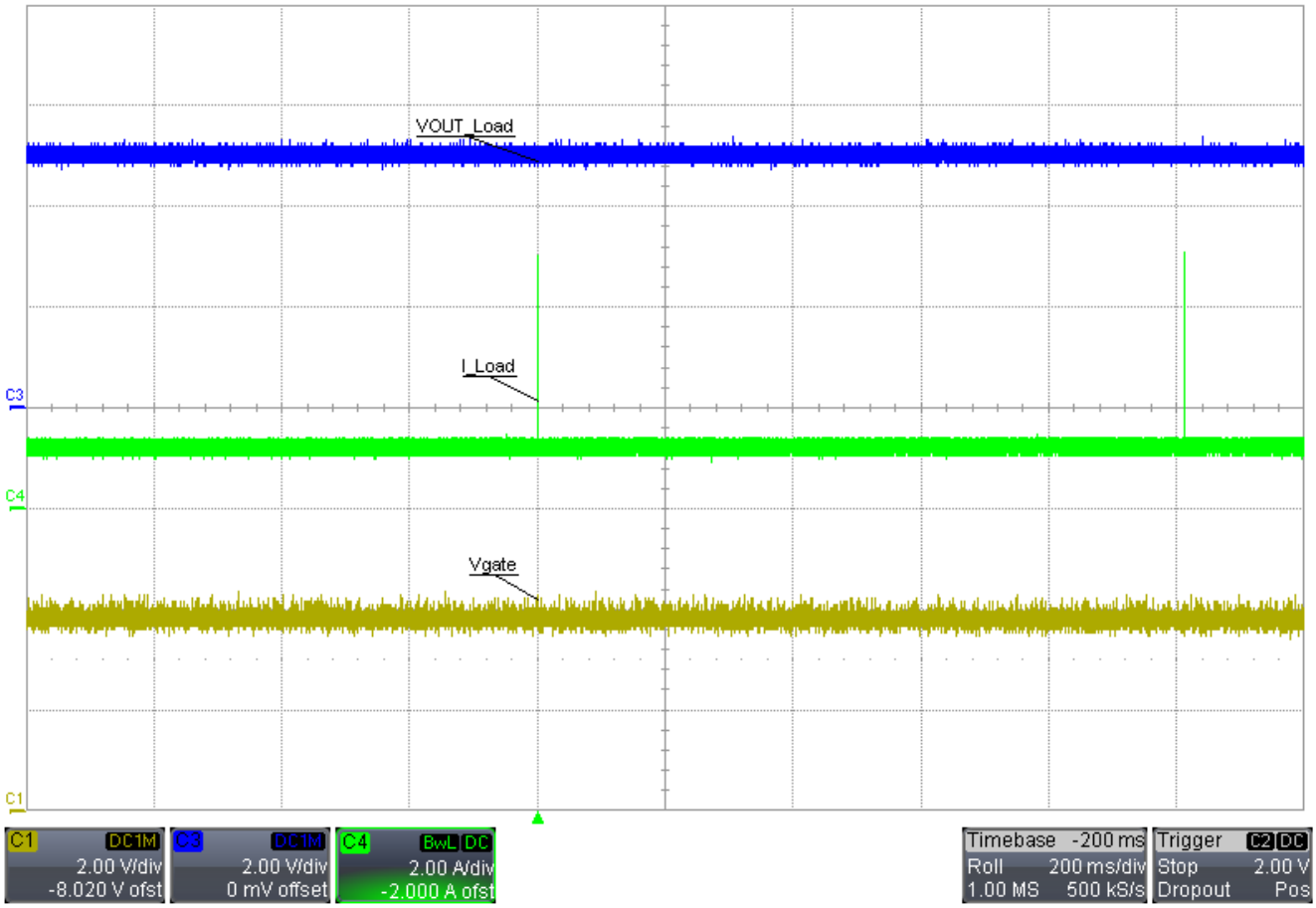


Figure 3-8. Disable Zero, 1 A to 5 A, 11 µs, 5-V Output Load Transient

3.4 INP

The INP is the driver reference signal for the high- and low-level transient as well as the slew rate. Monitor **INP (TP7)** to verify the signal is correct. Depending on **U5**, INP is at a 2.5-V or 1.25-V full scale load step.

The following scope plot is the INP signal relative to the load transient. For the 125-A variant, a 1-V INP signal produces a 100-A load step.

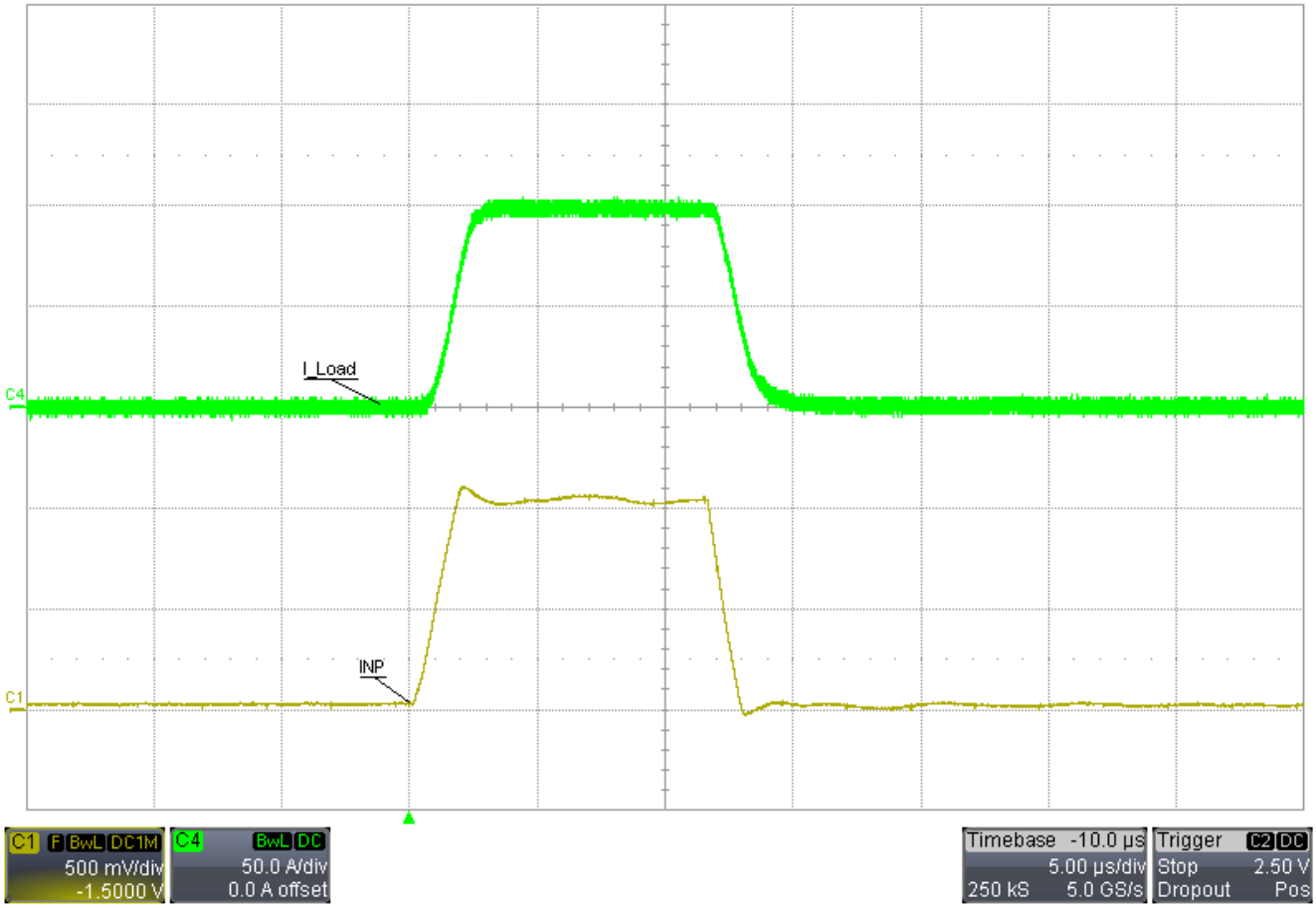


Figure 3-9. INP TLV431, 1 A to 100 A, 10-V Output Load Transient

3.5 Dual-Output Power Supply

The board has a dual-output power supply providing a +12-V and –12-V rail for the pulse shaping and driver circuits. This uses a combined SEPIC and Cuk configuration with a single inductor at the input and coupled inductor at the outputs.

The following scope plot is the power supply switch nodes for a 9-V input. **SW1** is probed at pin 1 of the LM5002 switch mode regulator. **SW2_Pos** is probed at the anode of **D2** and **SW2_Neg** is at the anode of **D4.**

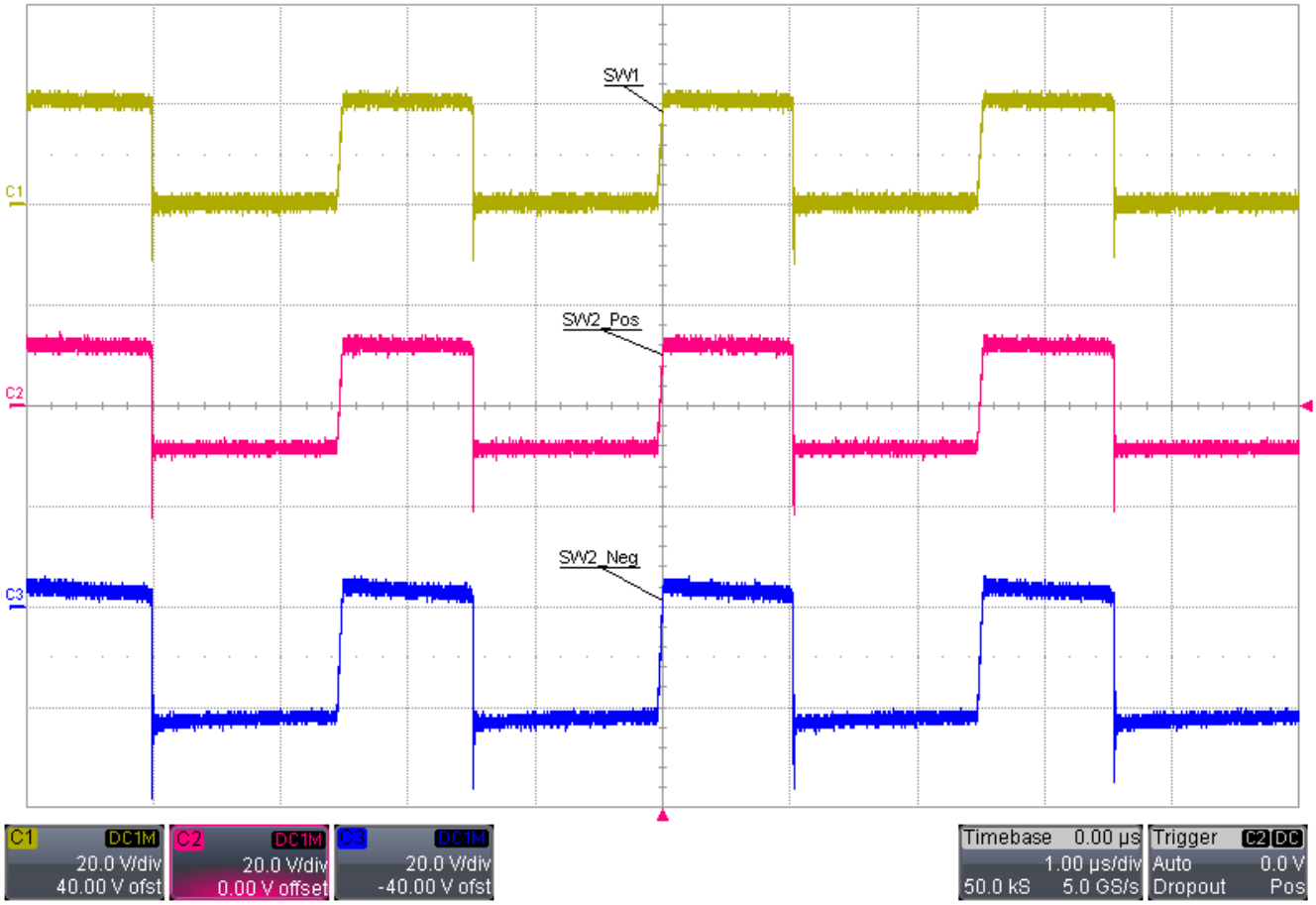


Figure 3-10. LM5002, 9-V Input, 12-V Positive and Negative Dual-Output Power Supply Switch Nodes

3.6 Overtemperature Protection

The overtemperature protection uses the LM26LVCISD-075, a 75ºC temperature sensor to shut down the driver and load switch. When thermal shutdown occurs, the sensor trips and turns off the driver and load switch circuit by pulling the power-down signal high. The overtemperature LED, **D5**, turns on to indicate that thermal shutdown has occurred. During thermal recovery, the LED turns off, and normal operation resumes.

For testing a 15-V, 5-A, 66-ms low-level pulse was used. The high-level pulse was set to 25 A at the minimum width of 11 µs. The average power dissipation was 5 W.

Thermal shutdown occurs when the sensor reaches a case temperature of about 67ºC. The thermal plot shows that the FET reaches around 114ºC. The results in the following image use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

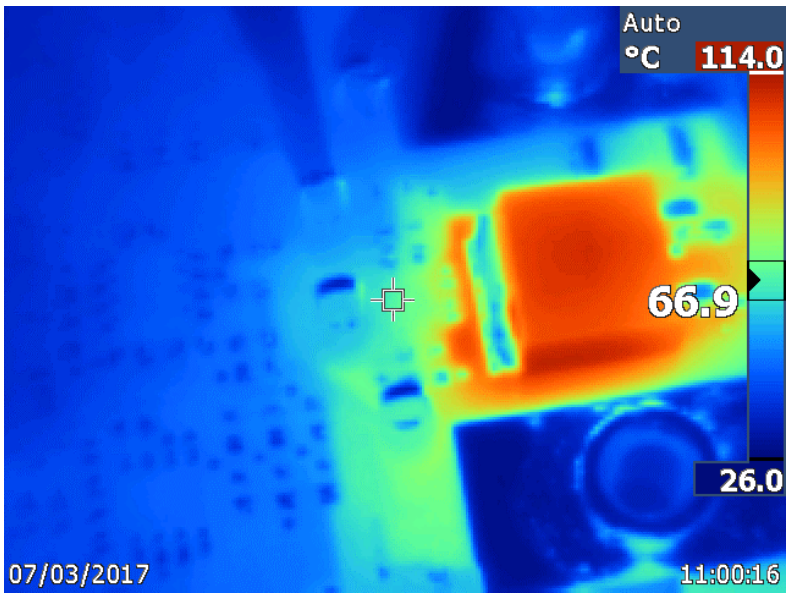


Figure 3-11. LM26LVCISD-075, PSMN008-75B Load Step Board Thermal Shutdown

Thermal recovery occurs at a lower temperature of about 63ºC. The thermal plot shows that the FET reaches around 94ºC. The results in the following image use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

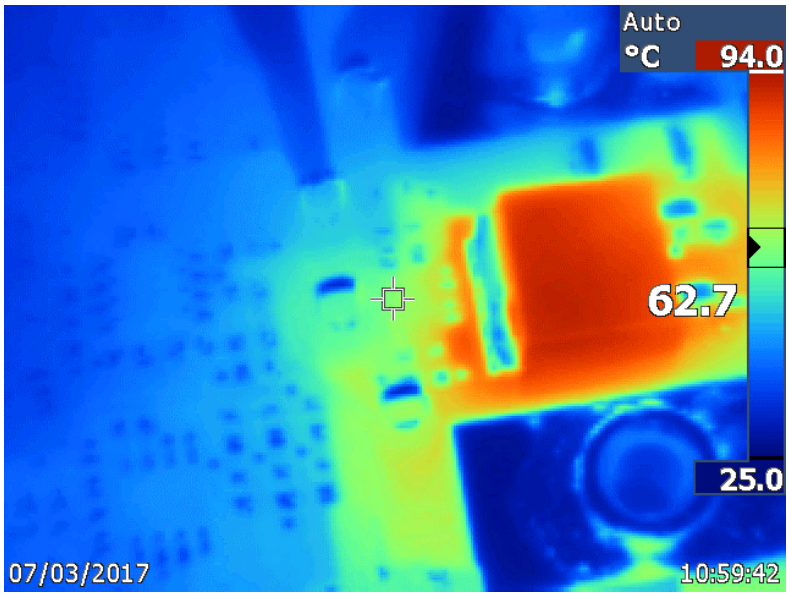


Figure 3-12. LM26LVCISD-075, PSMN008-75B Load Step Board Thermal Recovery

3.7 Slew Rate Adjust

The slew rate adjustment is made by turning the potentiometers **R12 and R58**. Jumpers **J4** and **J5** can be installed to set the range of slew rate adjustments. The measured slew rate can be as high as 100 A/µs. The results in the following waveform use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

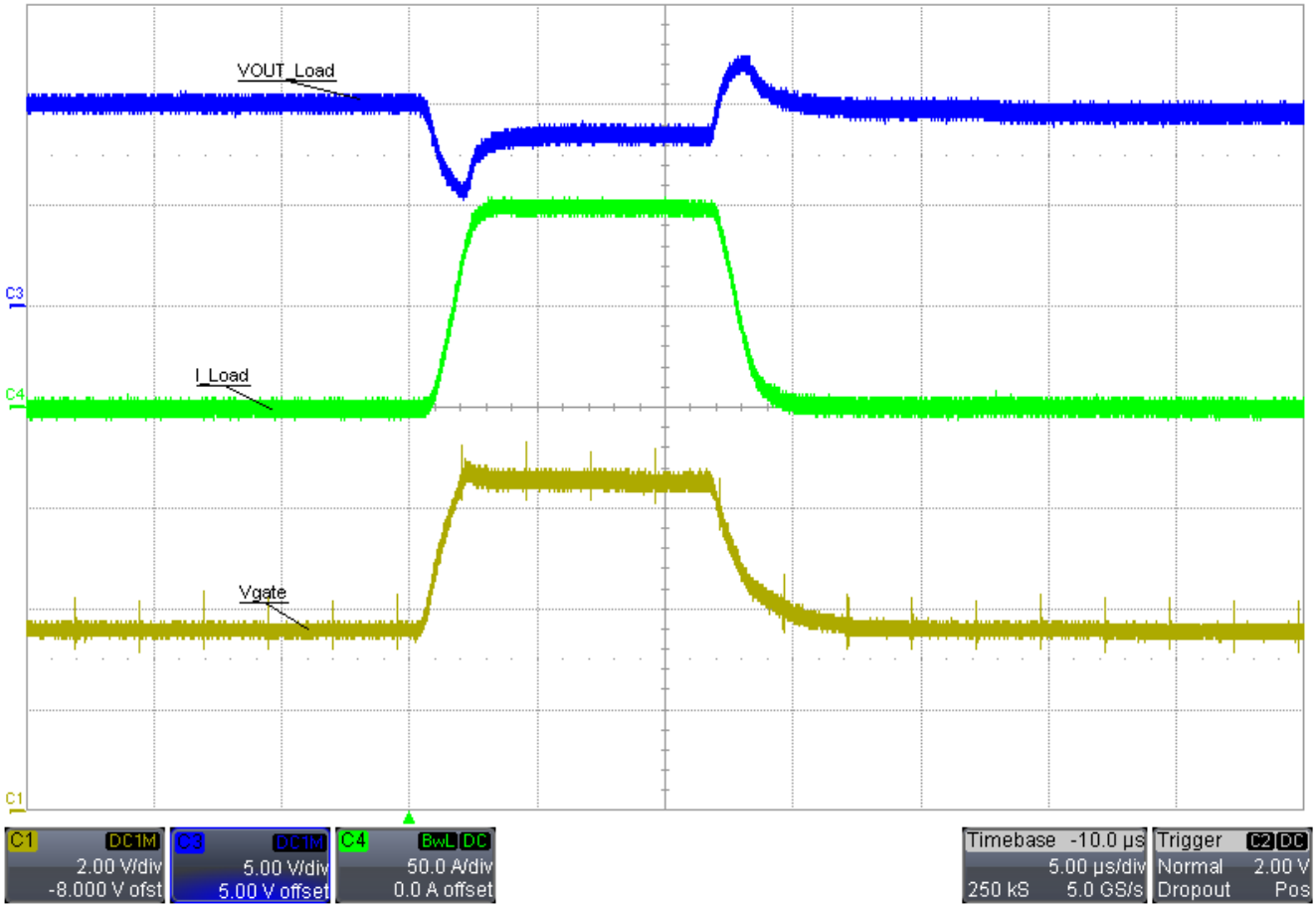


Figure 3-13. 10-V Output, 1-A to 100-A Load Transient, 1 µs Rise Time, Max Slew Rate

3.8 Settling Time Adjust

The settling time adjustment is made by turning potentiometer R43. There are no jumpers to set the range of this feature. Depending on the setup inductance and magnitude of the current step, a low R43 value can cause an unstable oscillatory state (see limitations of wiring inductance). The following data was taken on the 50-V, 125-A variant using the PSMN008-75B Q2 FET.

The following capture shows an underdamped load step by decreasing settling time potentiometer R43.

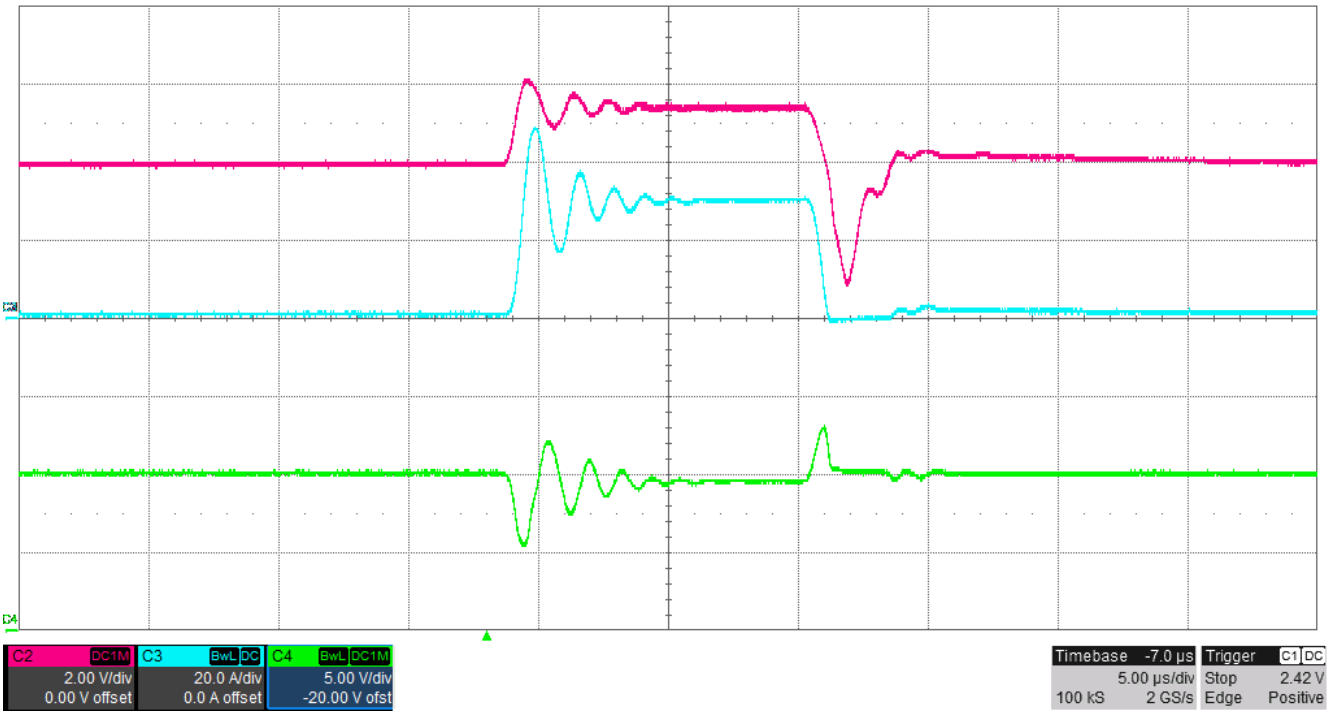


Figure 3-14. Maximum Slew Rate, 10-V Output, 1-A to 30-A Underdamped Load Transient

The following capture shows an overdamped load step by increasing the settling time potentiometer R43 to the maximum value.

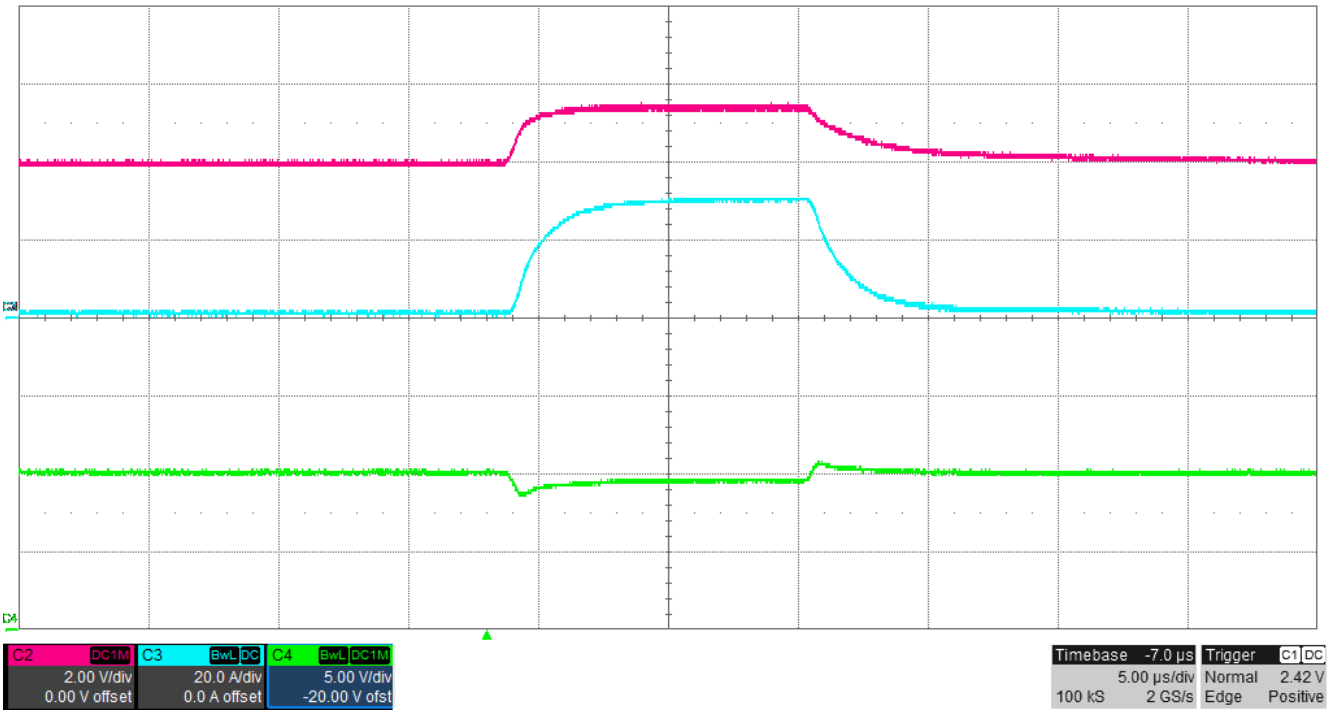


Figure 3-15. Maximum Slew Rate, 10-V Output, 1-A to 30-A Overdamped Load Transient

The following capture shows a critically damped load step. If minimizing overshoot is needed, increase the positive and negative slew rate.

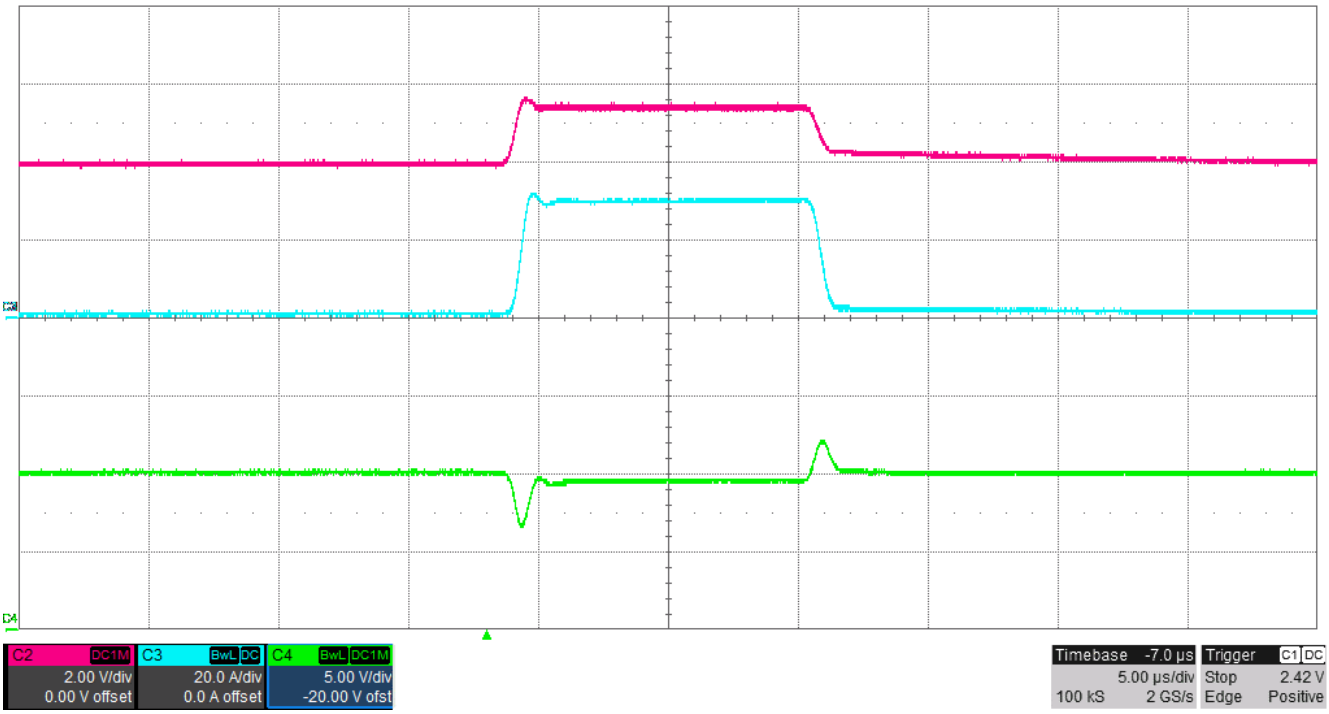


Figure 3-16. Maximum Slew Rate, 10-V Output, 1-A to 30-A Critically Damped Load Transient

3.9 Low- and High-Level Adjust

The low- and high-level adjustment is made by turning the potentiometers **R15** and **R23**, respectively. Make sure the levels along with the pulse width and period meet the SOA ratings of the FET **(Q2)**.

The following scope plot is a 1-A to 100-A load transient for a 100-V output. The results in the following image use a PSMN035-125B MOSFET in the 100-A, 100-V variant.

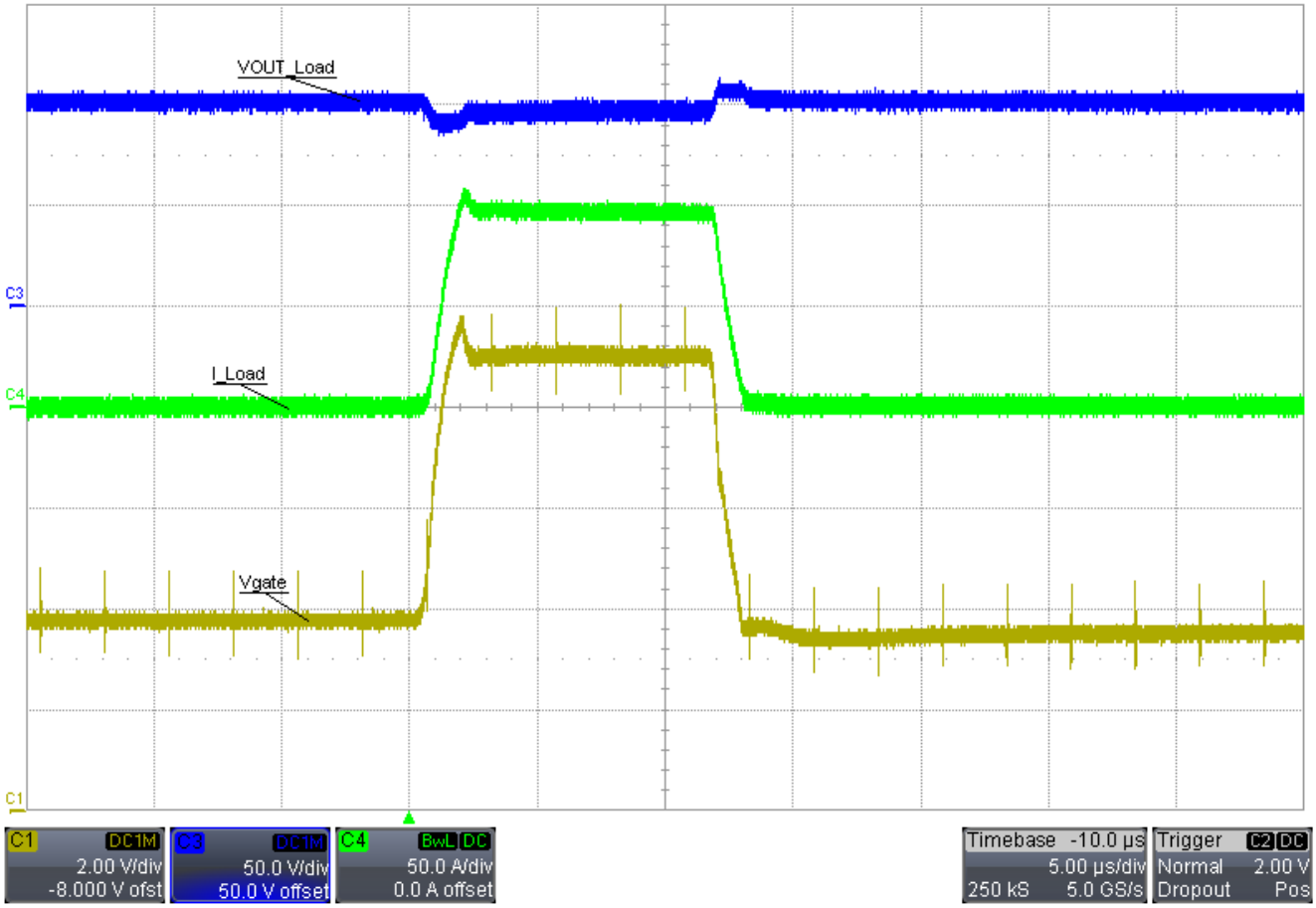


Figure 3-17. PSMN035-150B 100-V Output, 1-A to 100-A Load Transient

The following scope plot is a 10-A to 25-A load transient for a load of 10 V. The results in the following waveform use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

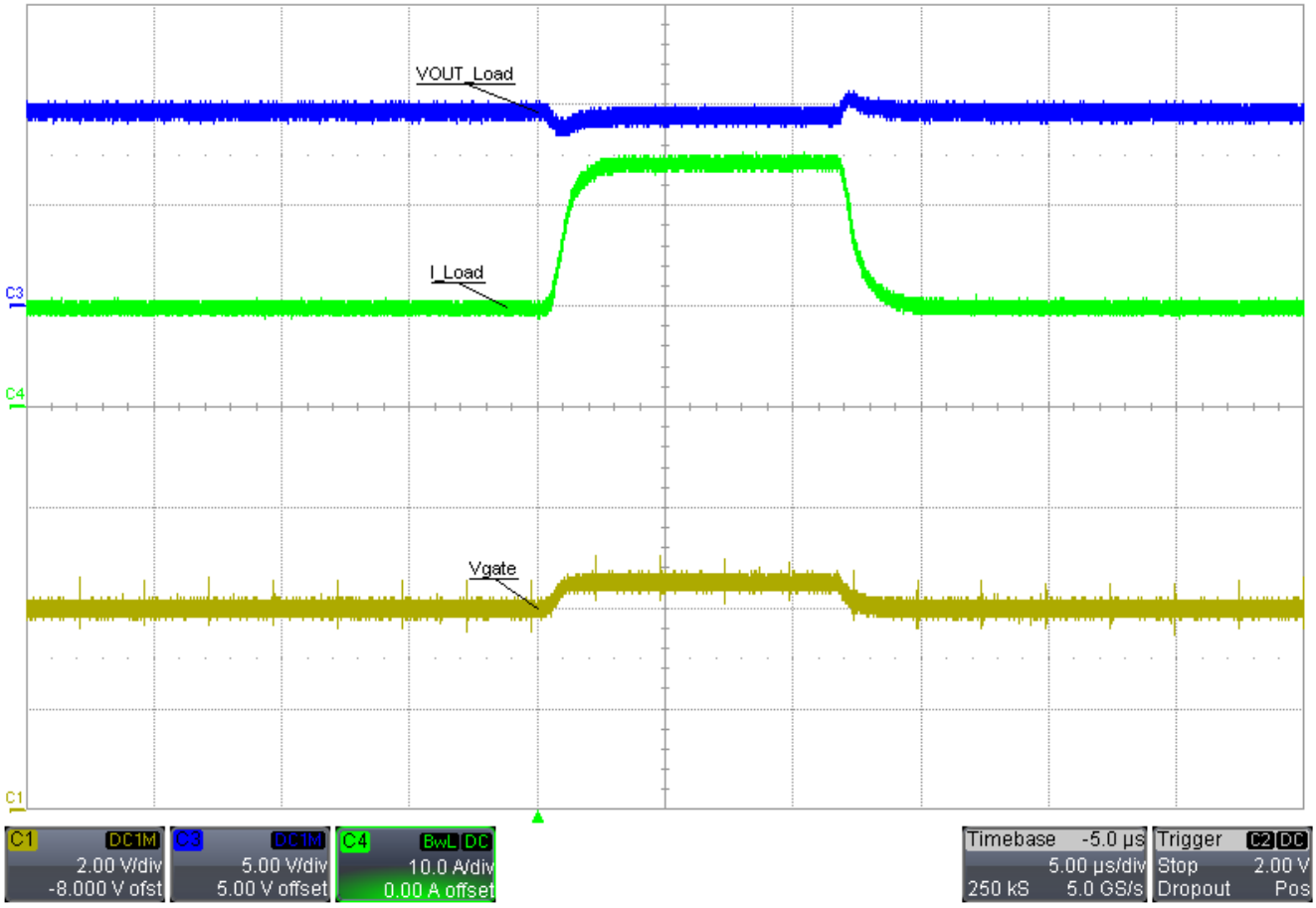


Figure 3-18. PSMN008-75B, 10-V Output, 10-A to 25-A Load Transient

3.10 Pulse-Width Adjust

The high-level pulse width adjustment is made by turning the potentiometer **R47**. Jumpers **J12** and **J13** can be installed to set the range of pulse-width adjustment. Pulse widths range from a minimum of 11 µs and maximum of 13 ms.

The following scope plot is the minimum pulse-width adjustment for the high-level step. The load step board is set up for a 1-A to 5-A load transient for a 5-V output. The results in the following waveform use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

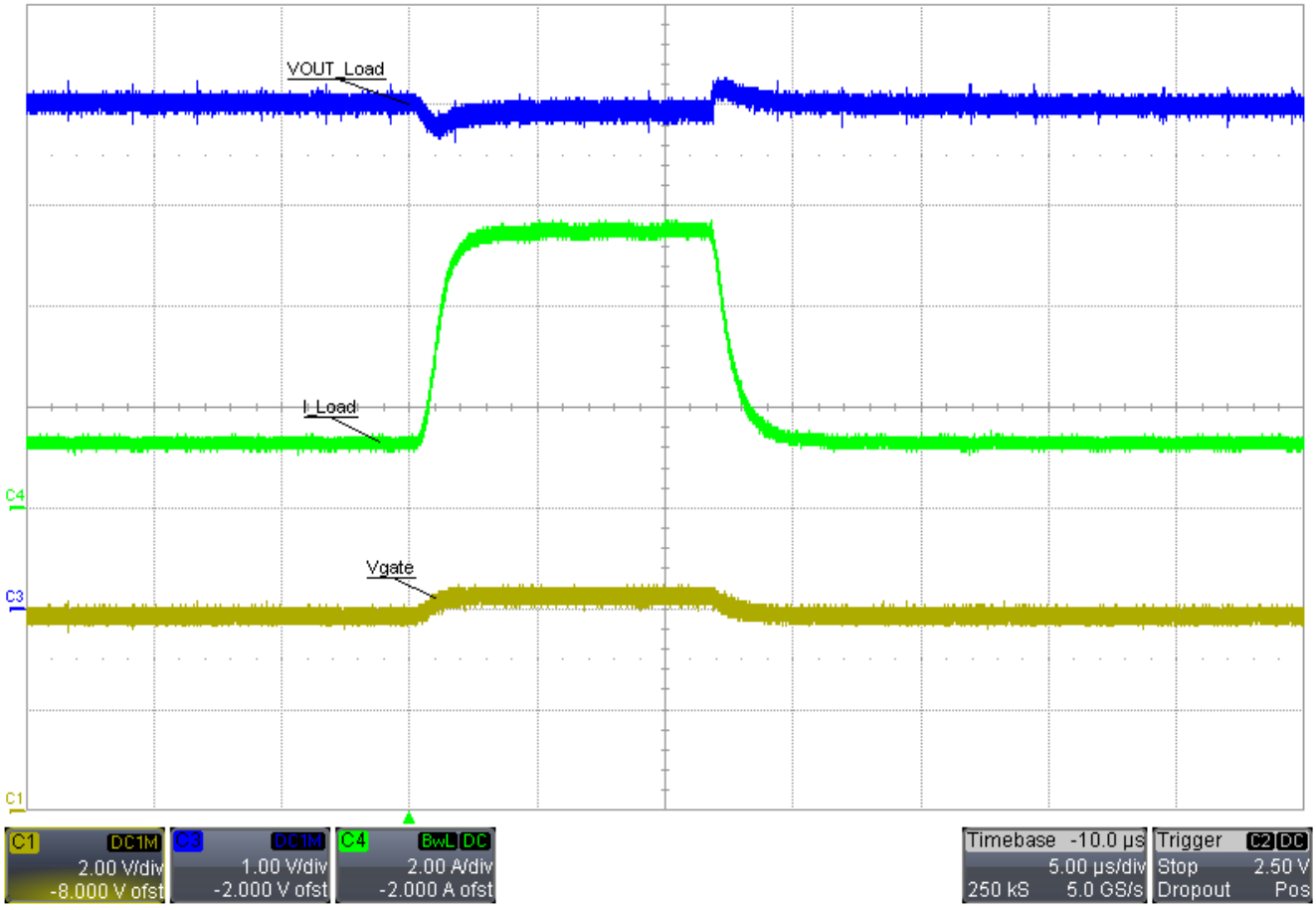


Figure 3-19. Minimum 11-µs High-Level Pulse Width

The following scope plot is the maximum pulse-width adjustments for the high-level step. The load step board is set up for a 1-A to 4-A load transient for a 5-V output. The results in the following image use a PSMN008-75B MOSFET in the 125-A, 50-V variant.

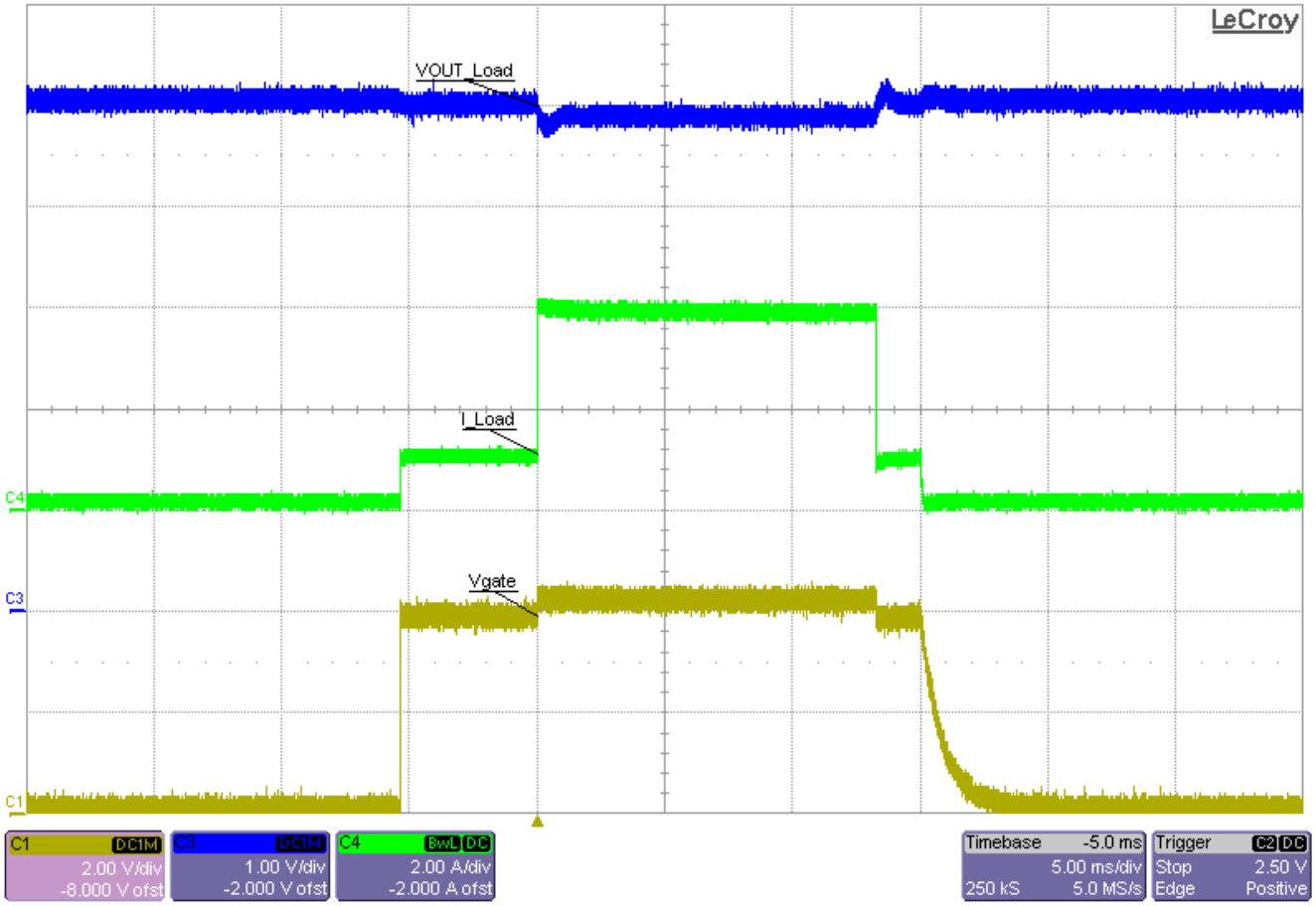


Figure 3-20. Maximum 13-ms High-Level Pulse Width

3.11 Period and Delay Adjust

The period adjustment is made by turning the potentiometer **R36**. Jumpers **J8** and **J9** can be installed to set the range of period adjustment. Periods range from a minimum of 11 ms and maximum of 160 ms.

The delay adjustment is made by turning the potentiometer **R46**. Jumpers **J10** and **J11** can be installed to set the range of delay adjustment. The delay ranges depend on the adjusted period.

The following scope plots are load transients of a 1-A to 5-A step at 5 V with a combination of minimum and maximum times for the period and delay.

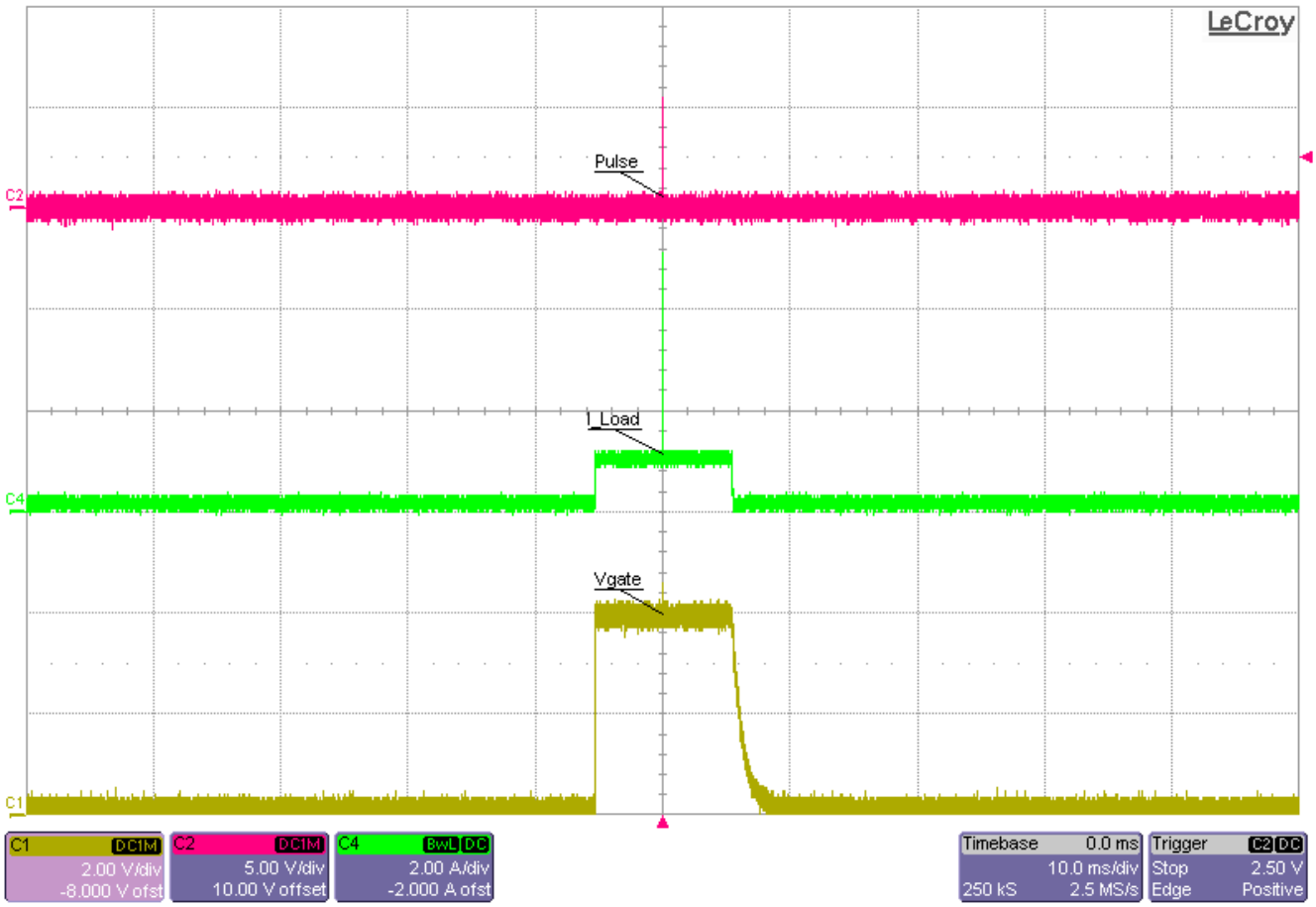


Figure 3-21. Minimum Delay and Minimum Period 11 ms

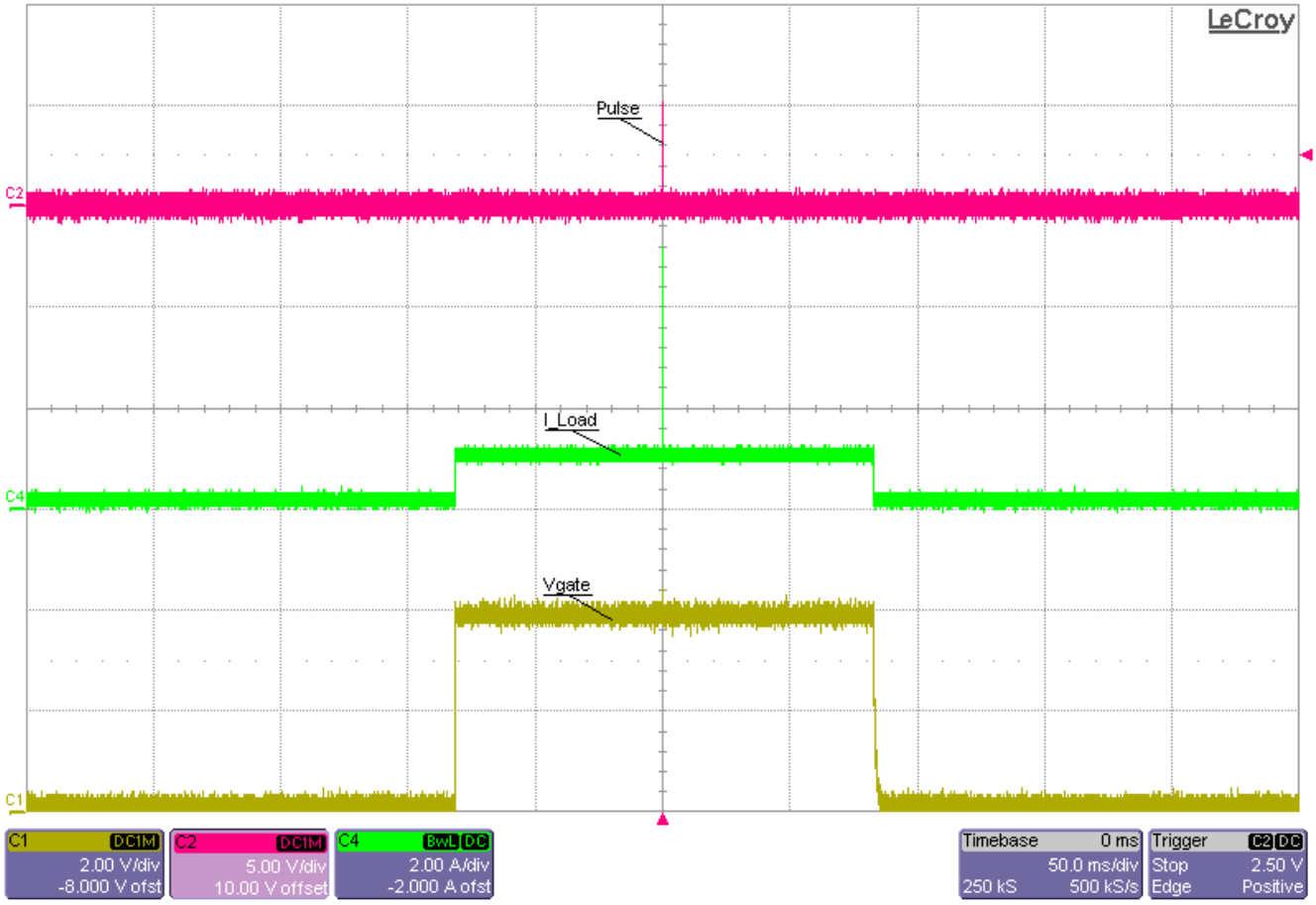


Figure 3-22. Maximum Delay and Maximum Period 160 ms

Having a large delay with a small a period causes a mistiming between the high-level step and the low-level step. The load transient does not occur because of this mistiming. Adjust the period and delay simultaneously to avoid this mistiming.

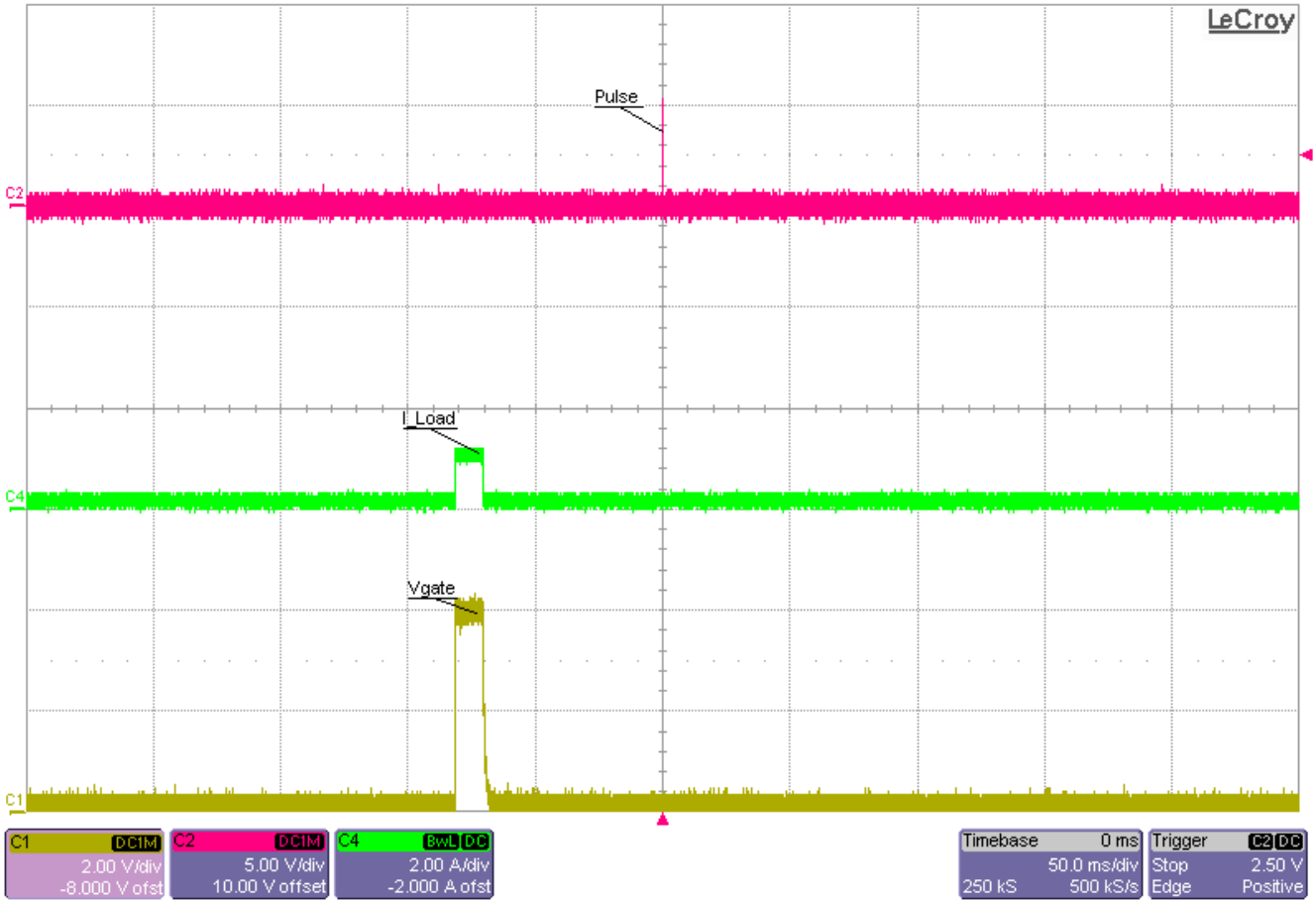


Figure 3-23. Maximum Delay and Minimum Period Mistiming

3.12 Frequency Response

The following bode plots measure the closed-loop feedback network of the driver and load switch. The load is at a constant low level with the free run and the zero-level disabled.

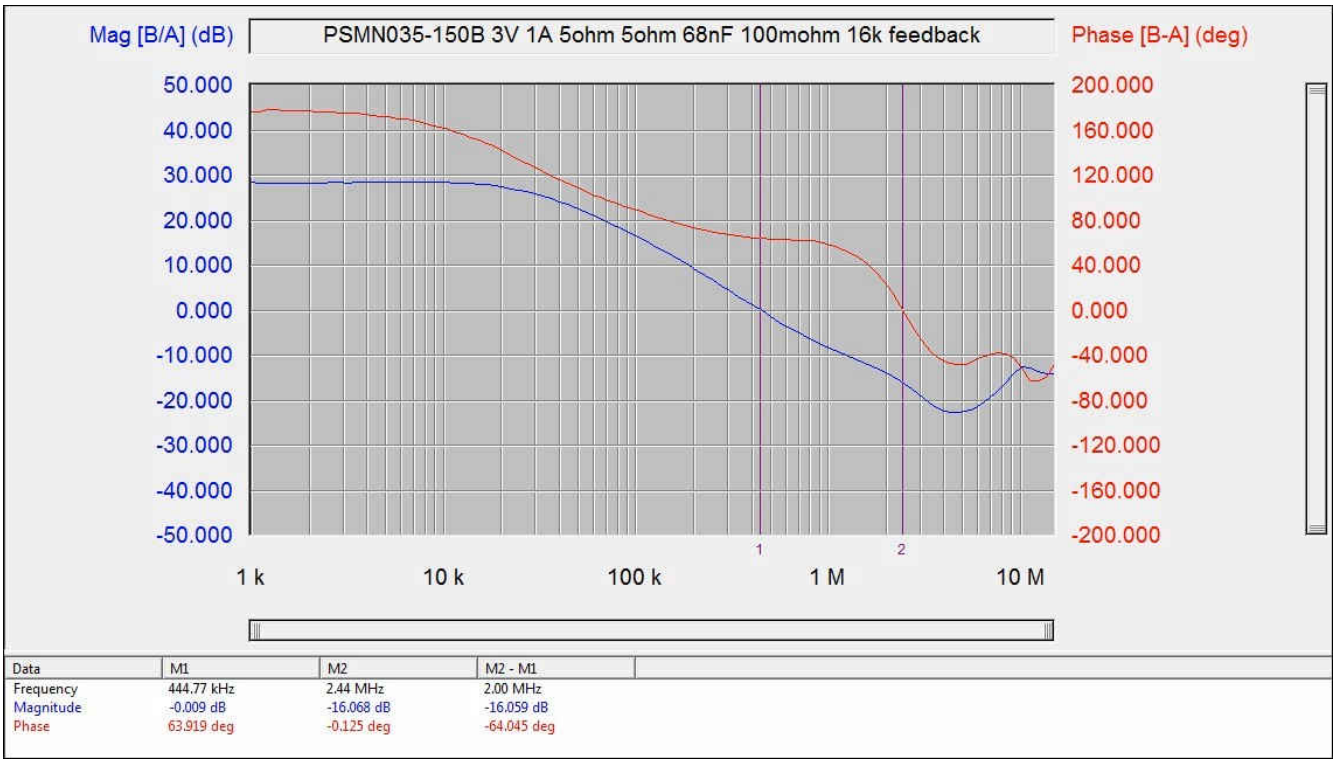


Figure 3-24. PSMN035-150B, 25-A Variant, 3-V, 1-A

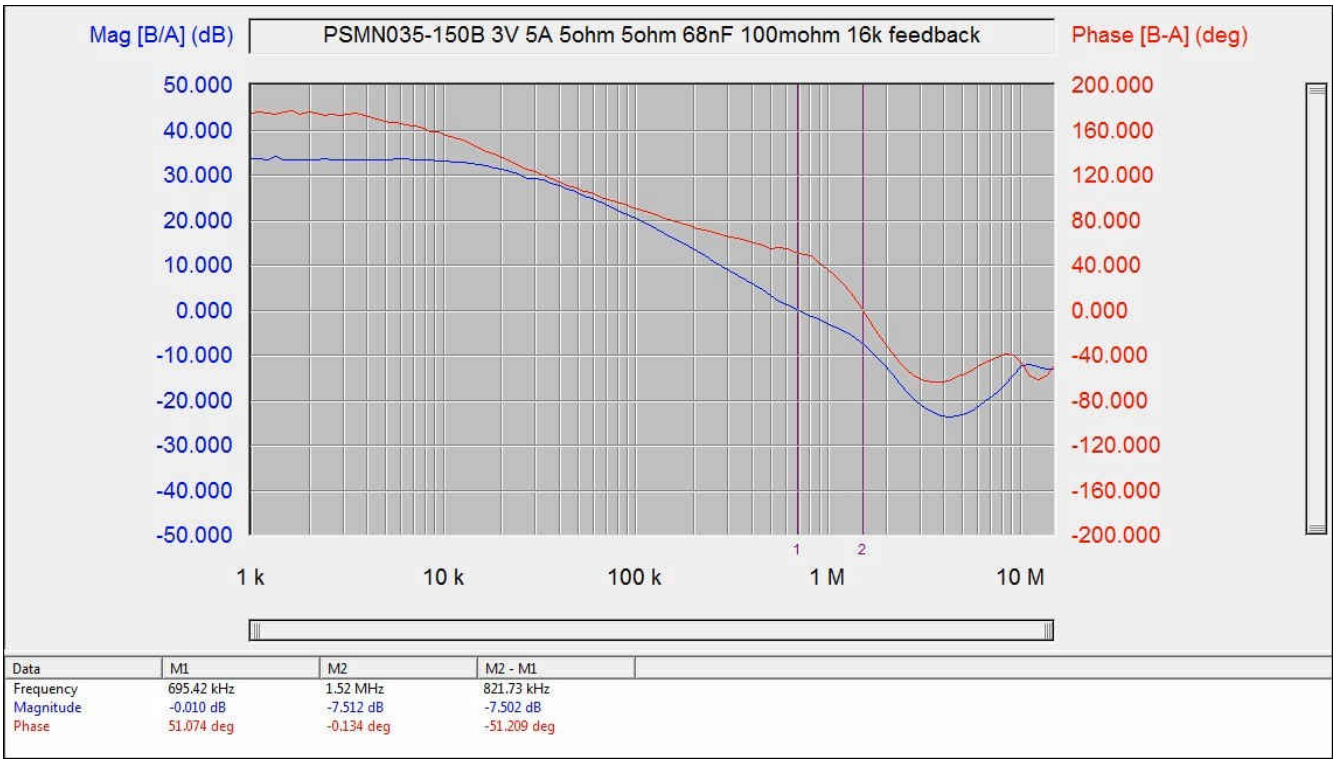


Figure 3-25. PSMN035-150B, 25-A Variant, 3-V, 5-A

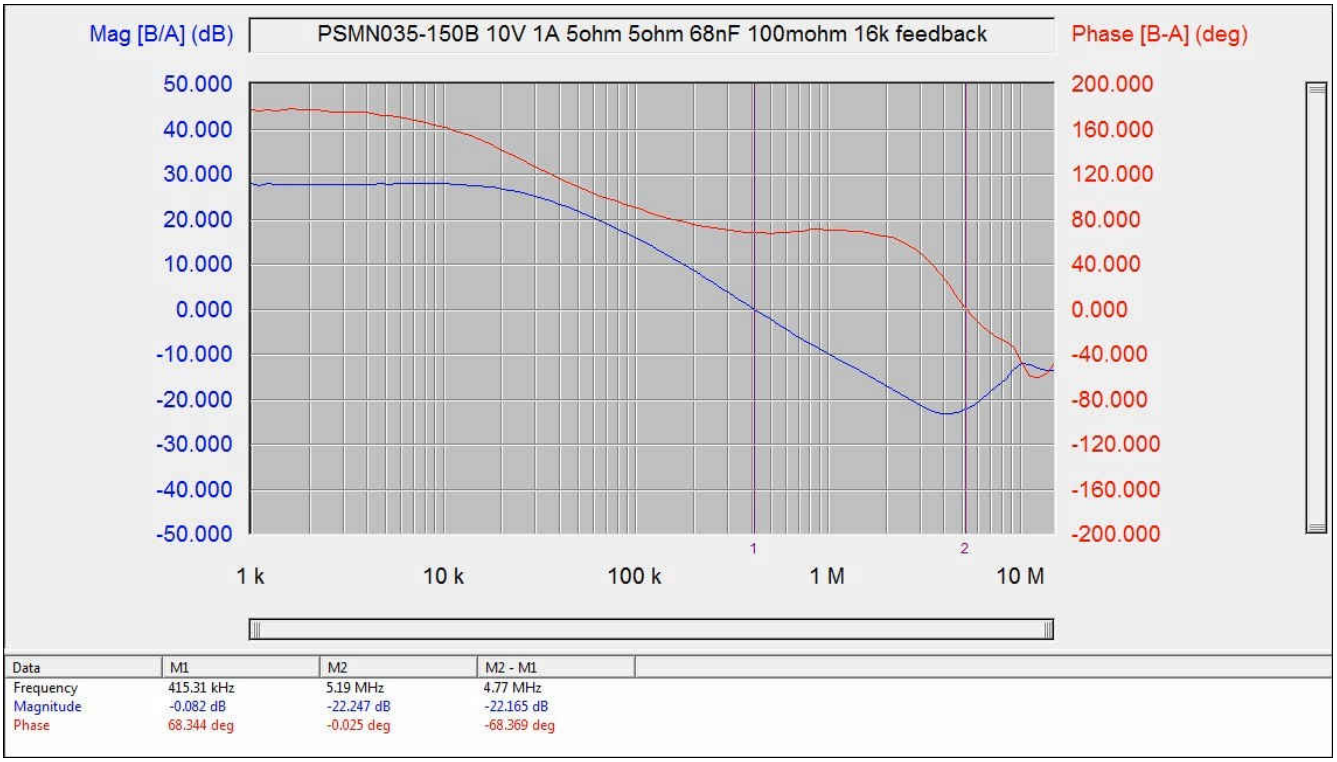


Figure 3-26. PSMN035-150B, 25-A Variant, 10-V, 1-A

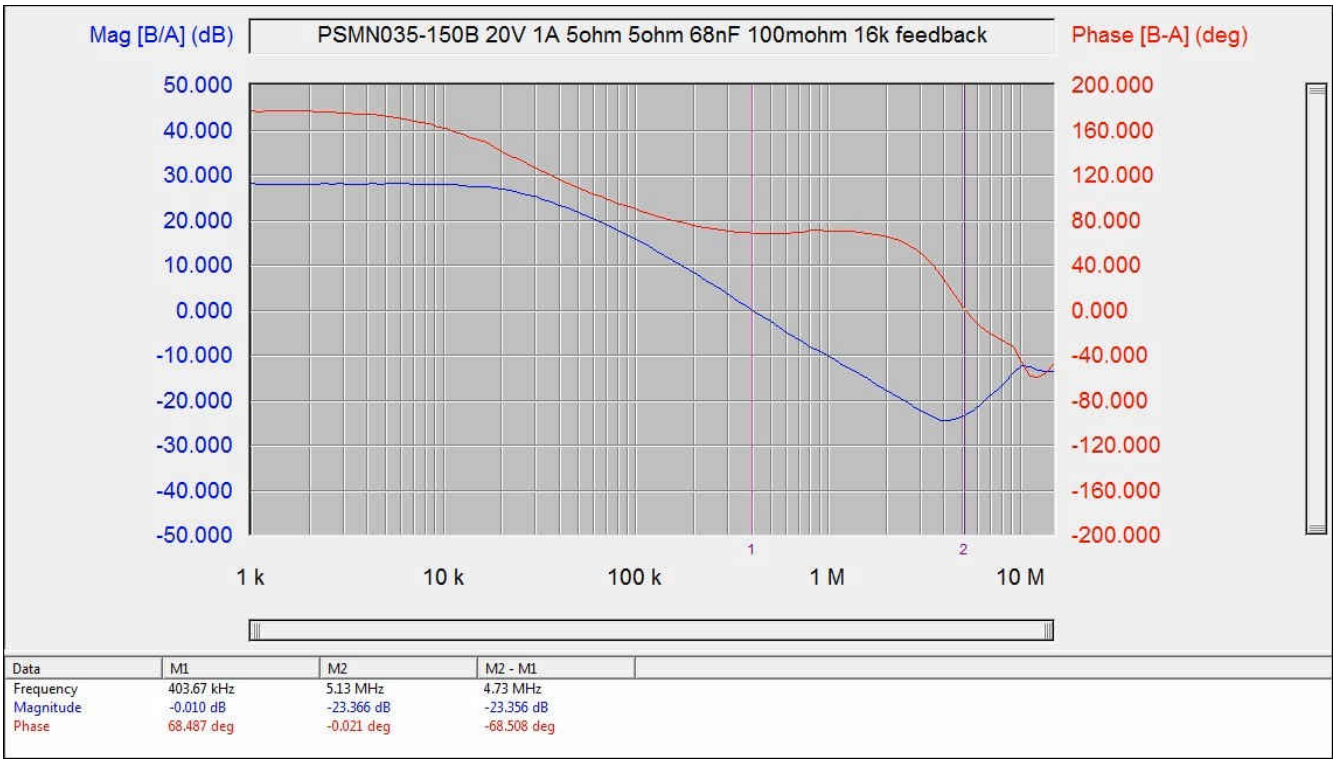


Figure 3-27. PSMN035-150B, 25-A Variant, 20-V, 1-A

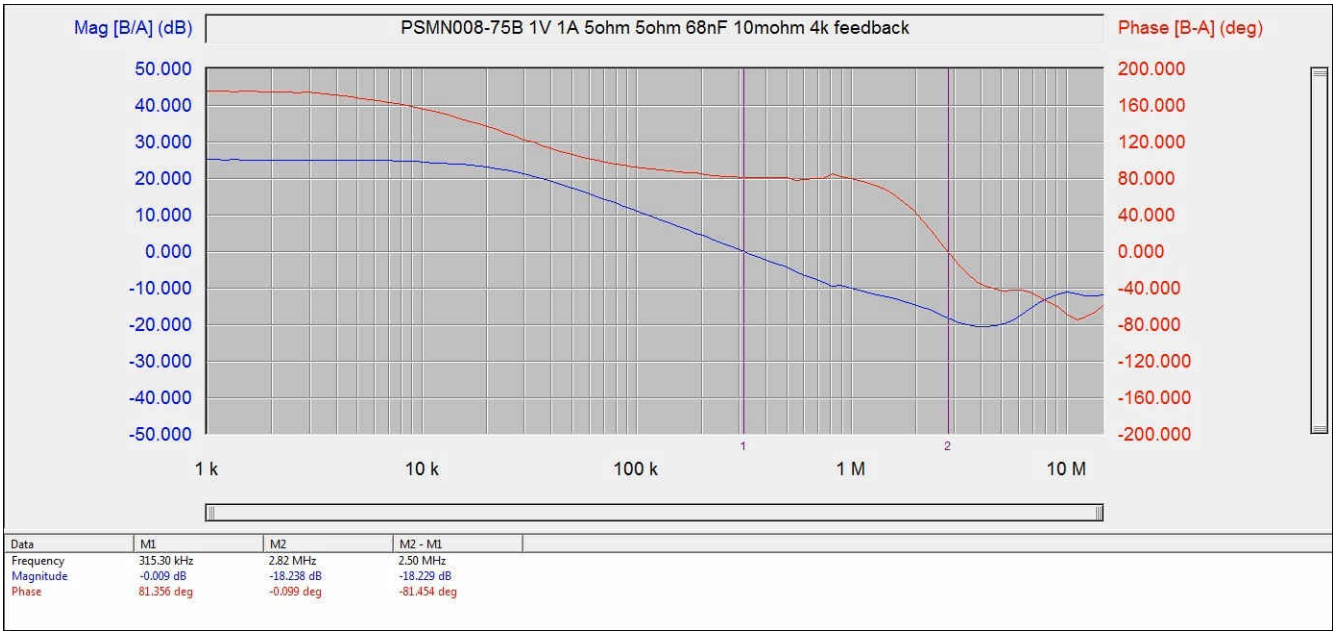


Figure 3-28. PSMN008-75B, 125-A Variant, 1-V, 1-A

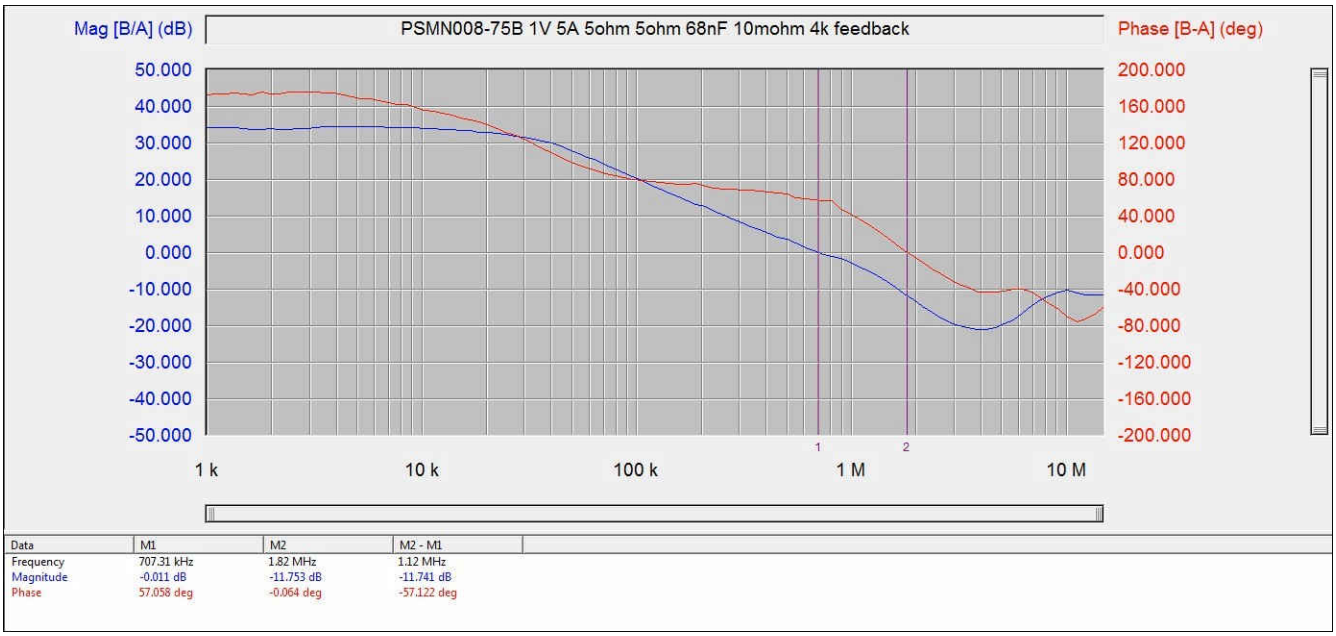


Figure 3-29. PSMN008-75B, 125-A Variant, 1-V, 5-A

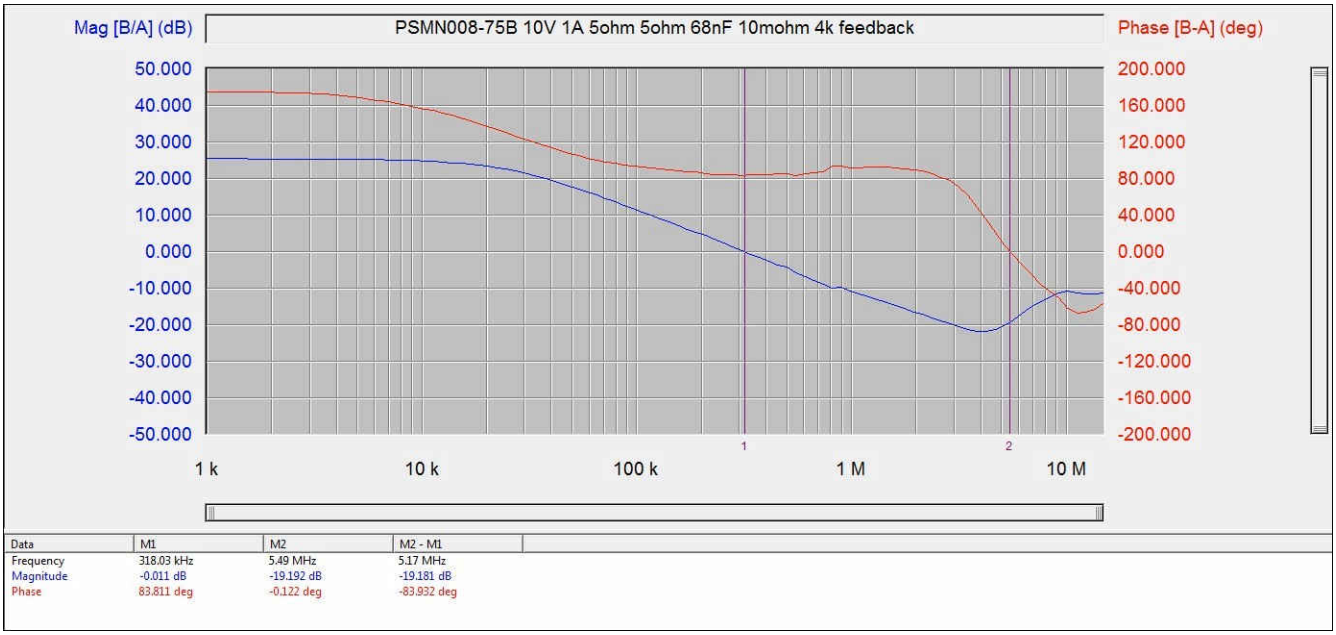


Figure 3-30. PSMN008-75B, 125-A Variant, 10-V, 1-A

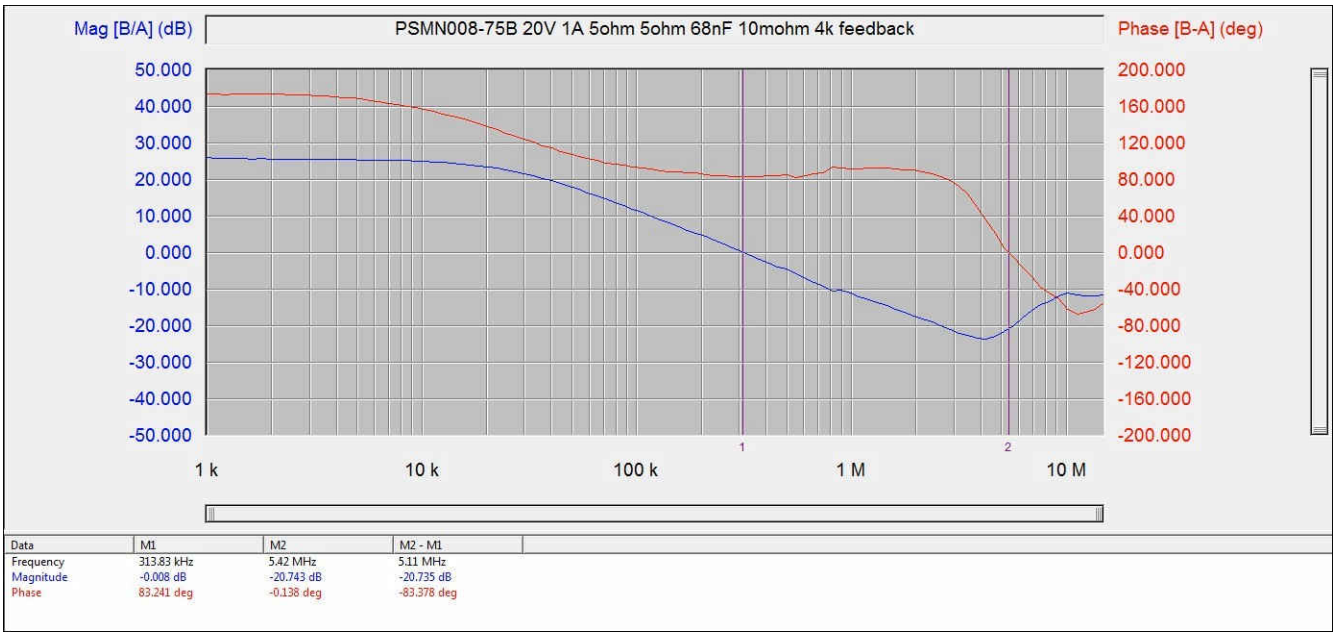


Figure 3-31. PSMN008-75B, 125-A Variant, 20-V, 1-A

4 Operation

This section shows the operation of the load step board. An initial setup is provided for safe and stable power up. The procedure provides step-by-step instructions for the initial power up of the board, as well as connecting the circuit under test for a load transient.

4.1 Initial Setup – Jumper Selection and Potentiometer Settings

Set the jumper selections and potentiometers for minimum on time and maximum slew rate. Install **Free Run (J6)** and have all other jumpers open. Have **Low (R15)**, **High (R23)**, **Period (R36)**, **Delay (R46)**, **Pos Slew (R12), Neg Slew (R58)**, and **Width (R47)** at the minimum by turning the potentiometers counterclockwise. Set the **Settling Time (R43) at midrange** to avoid oscillations if turned too low.

Keeping the slew rate potentiometers set to the minimum level in the high-range setting with **J4** and **J5** open is recommended. This delivers the fastest slew rate of 100 A/µs.

4.2 Procedure

4.2.1 Initial Power Up

1. Verify that **Vout_Load (J2)** is disconnected
2. Install a standard 9-V alkaline *rectangular* battery to **J1** or a bench DC power supply that can be connected with hook test clips to **Vbatt/Vin (TP1)** and **GND (TP3)**. The supply voltage range for the board is 6-V to 12-V DC. When using a 9-V power supply, the input current is 33 mA to 46 mA at slow and fast slew rates, respectively.
3. Turn on **Power (S1)**, verify the **Pgood (D7)** LED turns on
4. Probe **Pulse (TP10)**, and trigger the signal on an oscilloscope
5. Probe **INP (TP7)**, and monitor the signal
6. Adjust **Low (R15)** and **High (R23)** to the desired low and high levels, respectively
7. Adjust *Settling Time* **(R43)** for the cleanest INP signal. This can require additional tuning after connecting the device.

4.2.2 Connecting the Circuit Under Test

1. Turn off **Power (S1)**
2. Connect the circuit under test to the **Vout_Load (J2)** and **GND_Load (J3)** terminals
3. Turn on **Power (S1)**
4. Monitor current into **Vout_Load (J2)** and the voltage across the circuit under test
5. Adjust all levels and slew rates as desired observing MOSFET **(Q2)** SOA limitations

5 Limitations and Capabilities

This section provides information on the circuit capabilities and known limitations of the load step board as well as interactions between the slew rate and level adjustments.

5.1 Wiring Inductance

When adjusting to a lower voltage, the load-step current is limited by the wiring inductance and slew rate of the setup. The following scope plot is a 1-A to 10-A load transient for a 1-V output. There is about a 0.7 V voltage drop, leaving 0.3 V for the MOSFET and sense resistor. Use short wires soldered directly to the load step board to reduce wiring inductance. The results in the following waveform use a PSMN008-75B MOSFET in the 125-A variant.

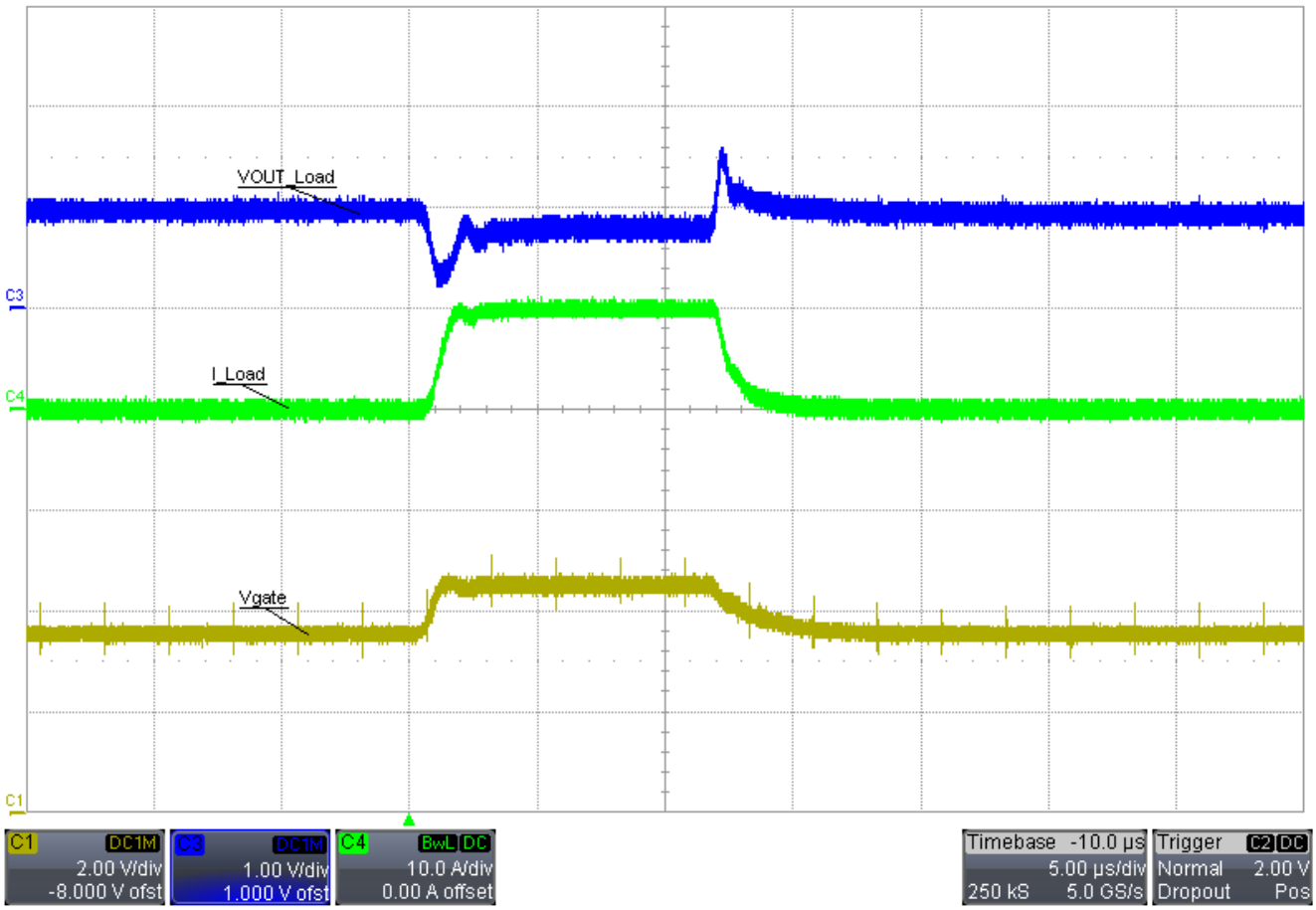


Figure 5-1. Wiring Inductance Voltage Drop 1 A to 10 A, 1-V Output Load Transient

A larger load step causes the MOSFET voltage to collapse, resulting in an abnormal load transient. The following scope plot is a 1-A to 15-A load transient for a 1-V output.

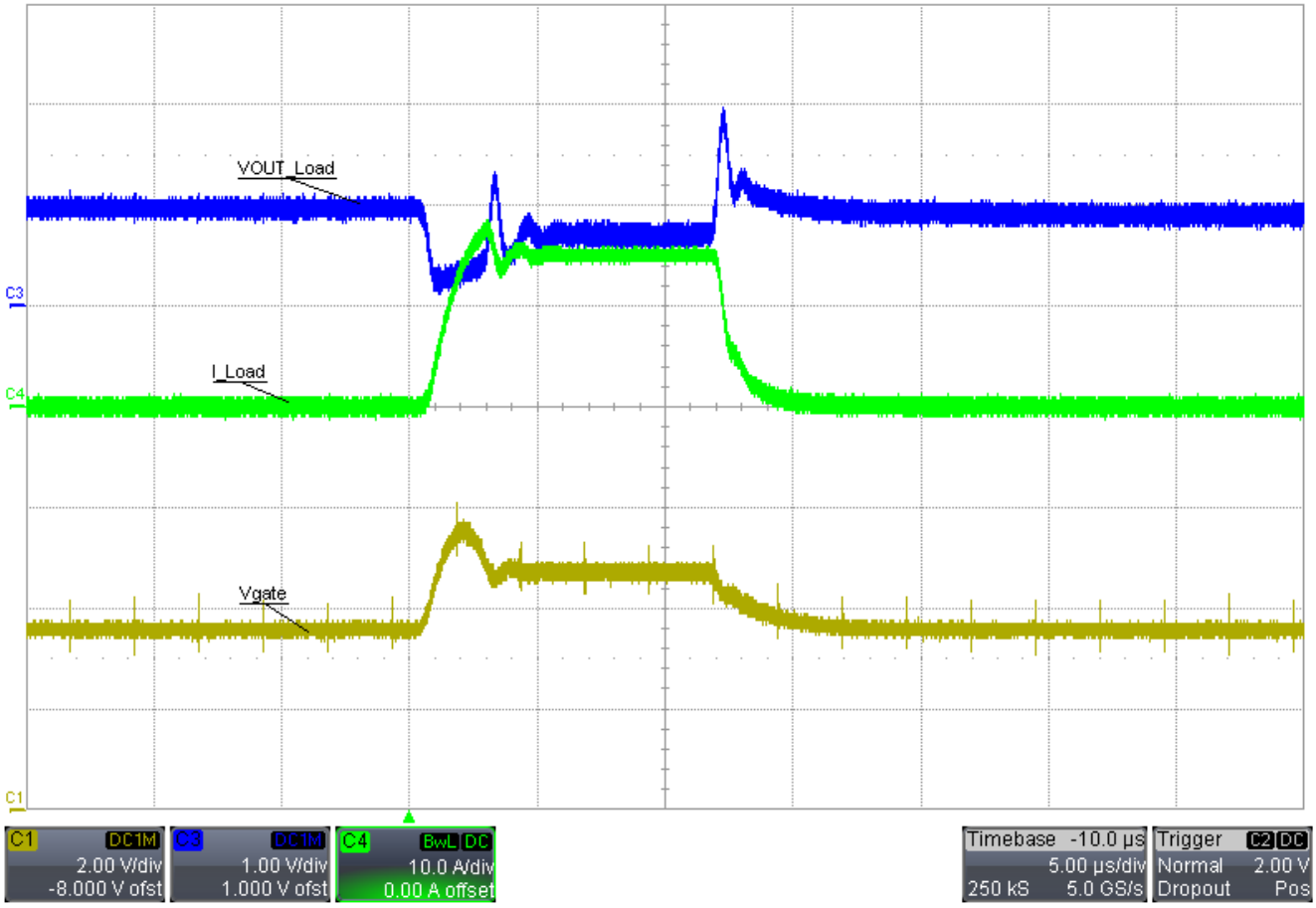


Figure 5-2. Wiring Inductance Voltage Drop 1 A to 15 A, 1-V Output Load Transient

5.2 Minimum Voltage

In higher voltage versions, the minimum voltage is limited for the circuit under test due to a higher reference voltage. Testing at a lower output voltage does not allow enough voltage on the FET during the droop. This is also a limitation of the wiring inductance in the setup. Use short wires soldered directly to the load-step board to reduce wiring inductance. The results shown in the following waveform use a PSMN008-75B MOSFET in the 125-A, 50-V variant. The following scope plot is a 1-A to 25-A load transient for a 5-V output exhibiting an abnormal result.

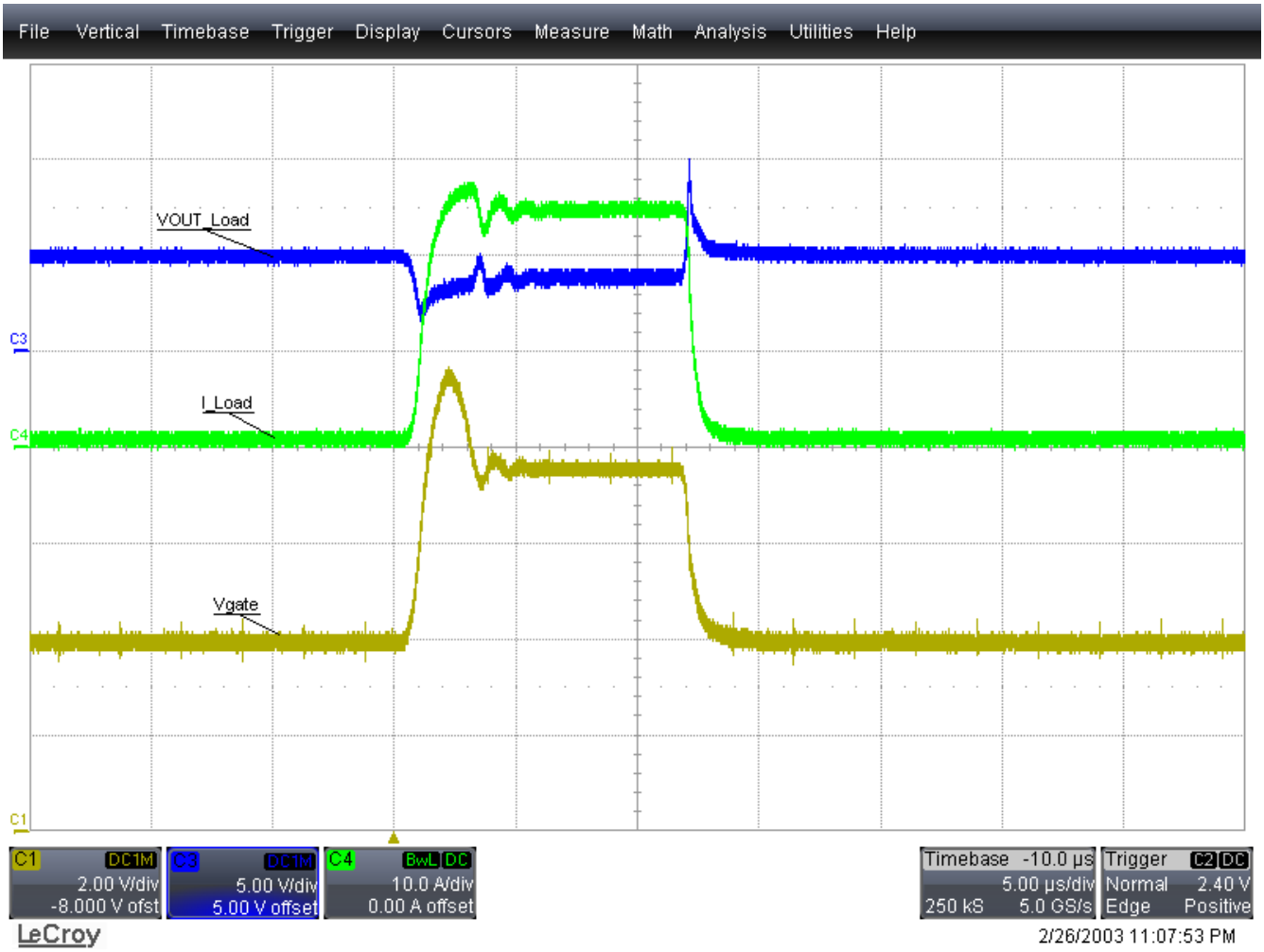


Figure 5-3. 1 A to 25 A, 5-V Output Load Transient

Applying a higher voltage does not collapse the FET voltage and creates a normal load transient. The following scope plot is a 1-A to 25-A load transient with a 10-V output.

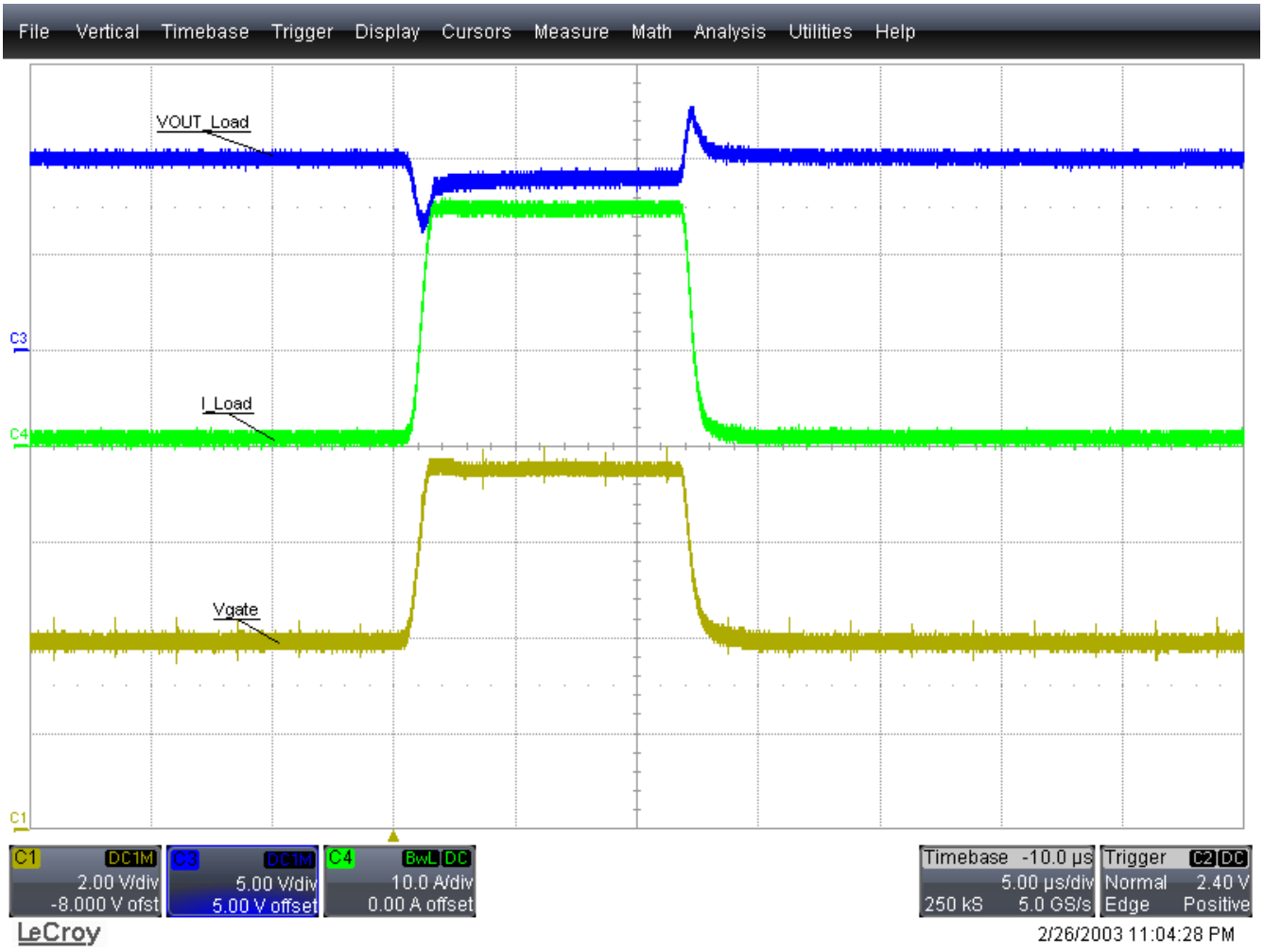


Figure 5-4. 1-A to 25-A, 10-V Output Load Transient

5.3 Battery Life

Based on the typical data for a 9-V alkaline battery, battery capacity is around 500 mAh. This limits the usable life around 10 to 15 hours.

6 Typical Failure Mechanism

This section provides information on what happens when the MOSFET **(Q2)** exceeds the power rating causing the circuit to fail. There are certain scenarios where the FET fails and the thermal protection circuit does not trip.

6.1 Fast Thermal Failure

Fast thermal failure occurs usually in high-voltage operation when the SOA rating of the MOSFET is exceeded. Generally, the FET **(Q2)** shorts, the sense resistor **(R21)** opens, the gate resistor **(R14)** is damaged, and the THS3120 op amp **(U4)** fails.

The following waveform shows a capture of a full-range step after damage to the load switch driver U4.

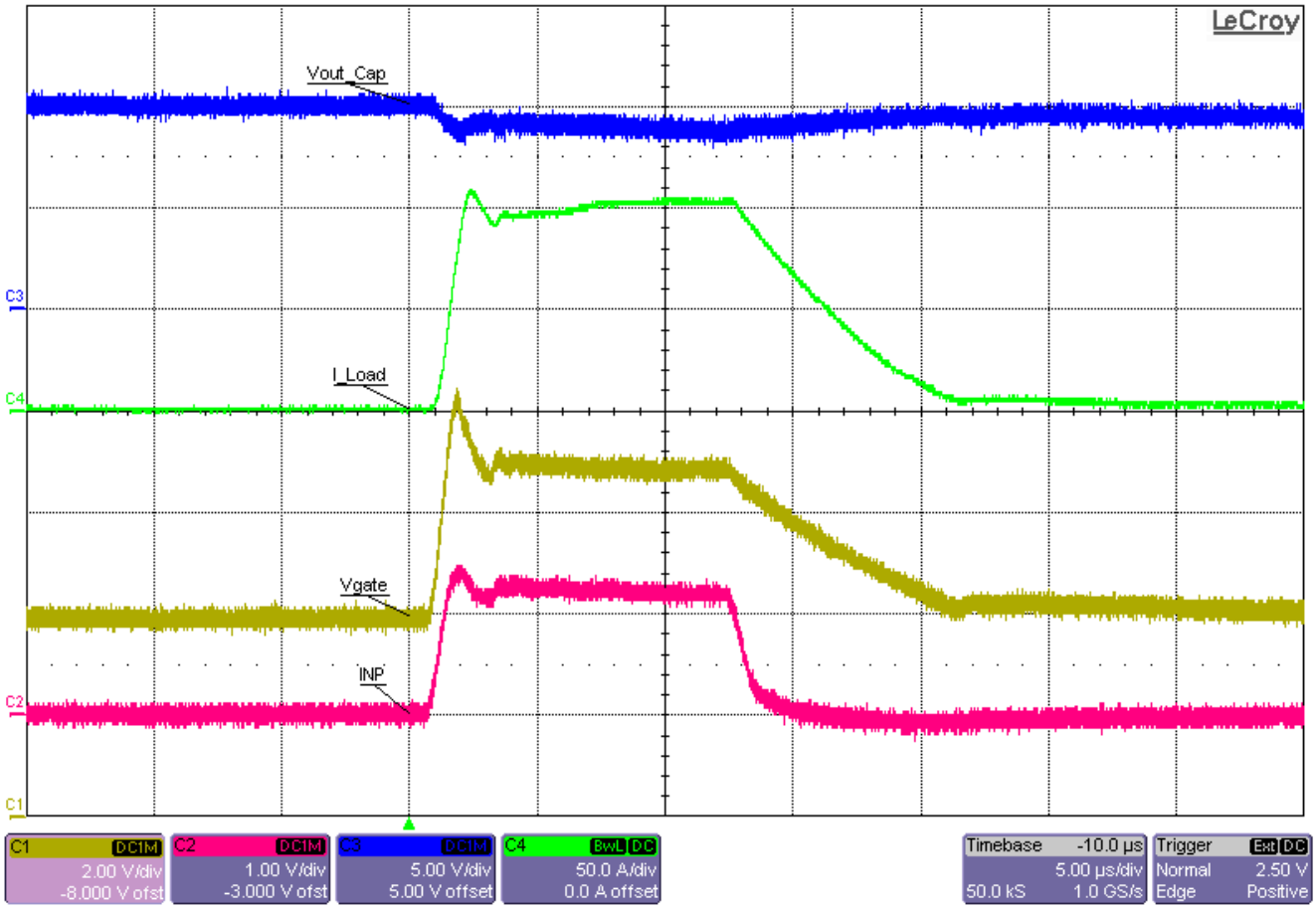


Figure 6-1. 1-A to 100-A Step, 10-V Output, Maximum Slew Rate, Damaged U4

The following image shows the same response after replacing U4.

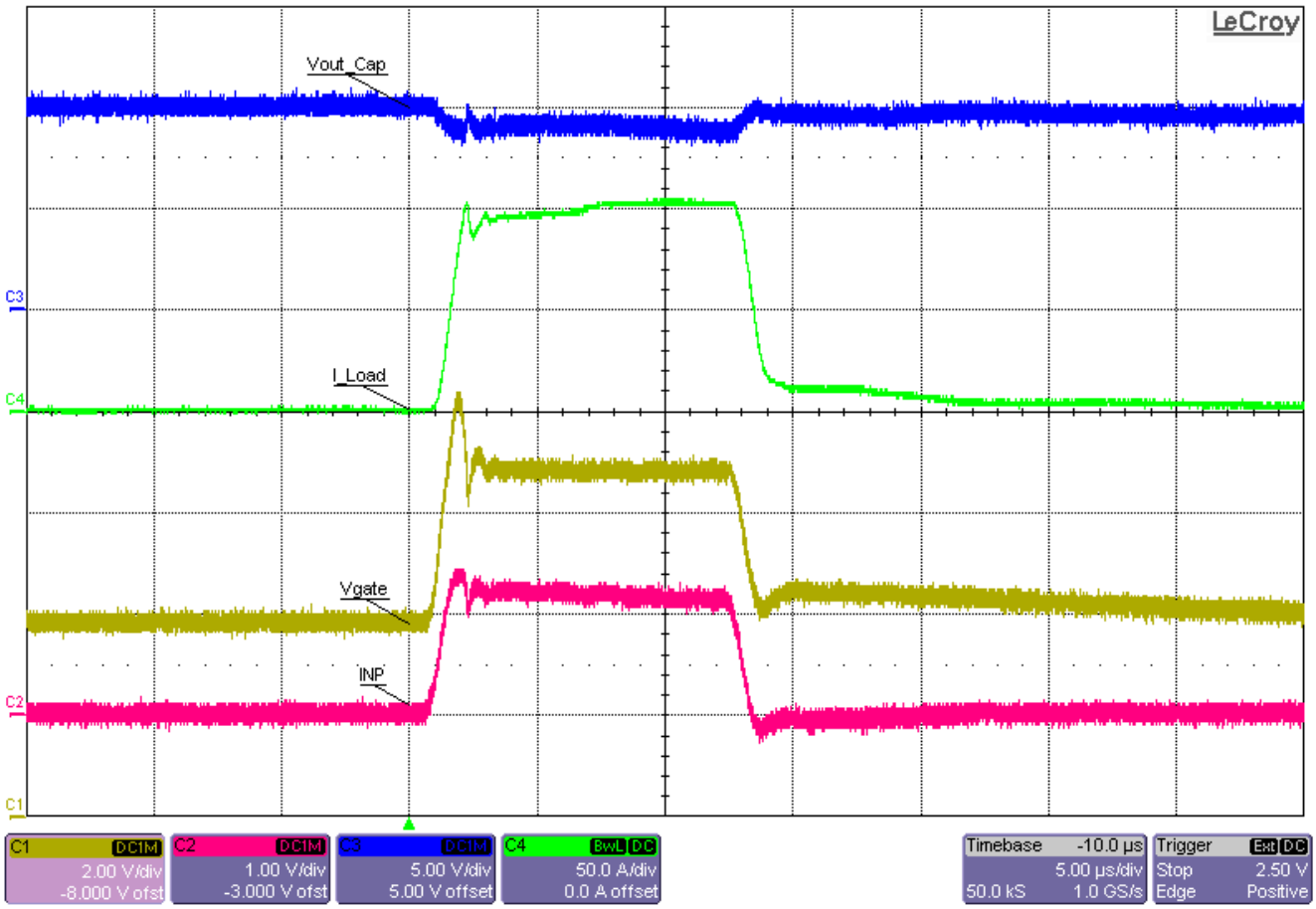


Figure 6-2. 1-A to 100-A Step, 10-V Output, Maximum Slew Rate, Replaced U4

6.2 Slow Thermal Failure

Slow thermal failure occurs when the FET internal junction exceeds the FET rating without tripping temperature protection. This can occur when using a fan to cool the board. In this case, the temperature sensor remained cooled, while the MOSFET still heats internally. Generally, the FET **(Q2)** shorts and the sense resistor **(R21)** opens. Cooling the load step board with a fan is not recommended.

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