Test Report: PMP40994

4-W Dual-Channel Isolated Gate Driver With 1500-V Isolation for IGBT Reference Design

Description

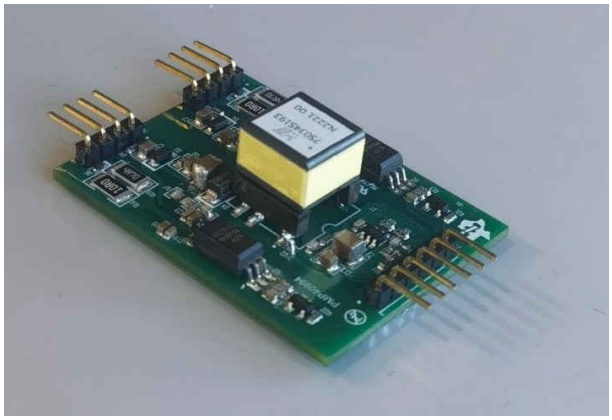
The reference design is a compact size, dual-channel output isolated gate driver board design for IGBT in solar inverter, PCS, as well as UPS and motor driver applications. The isolated bias power is implemented with fly-buck topology using the TPS54308 synchronous buck converter. This converter provides primary-side regulation without the need of optocoupler feedback and offers good output voltage regulation with certain input voltage variation versus the open-loop control method. The design takes 12-V input voltage and generates a non-isolated 5-V rail for primary-side MCU and two isolated outputs with 1500-V function isolation. Each output channel was split to 15-V and –8-V rail and biases each UCC23513 isolated gate driver. The total maximum power for each channel is 2 W. The design is a single-layer PCB board for easy manufacturing.

Features

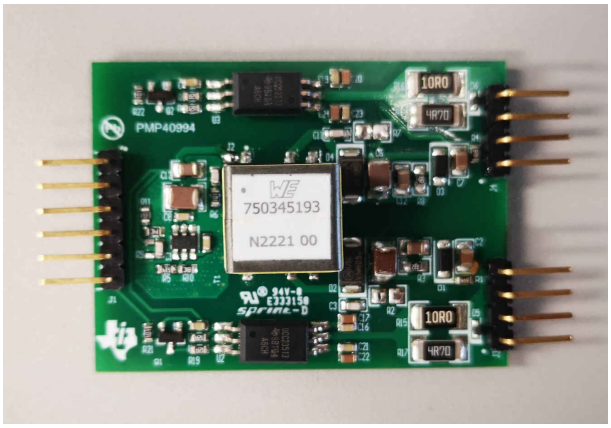
- Compact isolated bias power plus isolated gate driver design
- Provides 5% output voltage regulation with loose regulated 12-V power rail input
- Each channel can support a maximum of two watts per IGBT
- Each channel has split +15-V, –8-V power rails for the gate driver
- Provides 1500-V isolation between primary and secondary
- Single-layer PCB for easy manufacturing

Applications

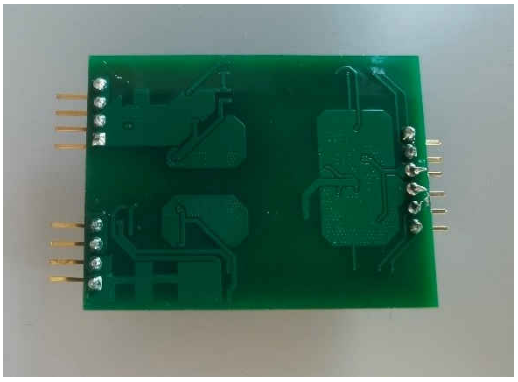
- Energy storage power conversion system (PCS)
- String inverter
- Three phase UPS
- AC drive power stage module



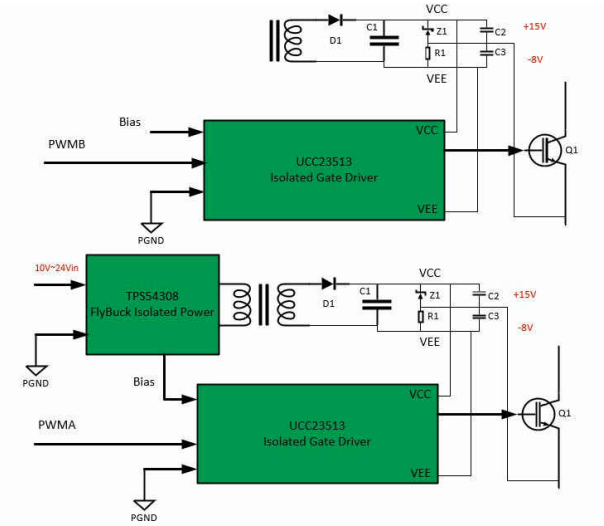
Top Angle View of Assembly



Top View



Bottom View of Assembly



System Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	10–20 VDC
Output voltage range	Dual channel, each one has +15 V, –8 V
Maximum output current	Each channel: 0.08 A
Maximum output power	4 W
Switching frequency (f_{SW})	350 kHz

1.2 Required Equipment

- DC source: GWinstek, GPS-4303C
- Electronic load: ITECH, IT8512+ and IT8510
- Oscilloscope: Tektronix, DPO MDO3024
- Infrared thermal camera: Fluke, Ti110

2 Testing and Results

2.1 Efficiency Graphs

The following image shows the efficiency across the line and load.

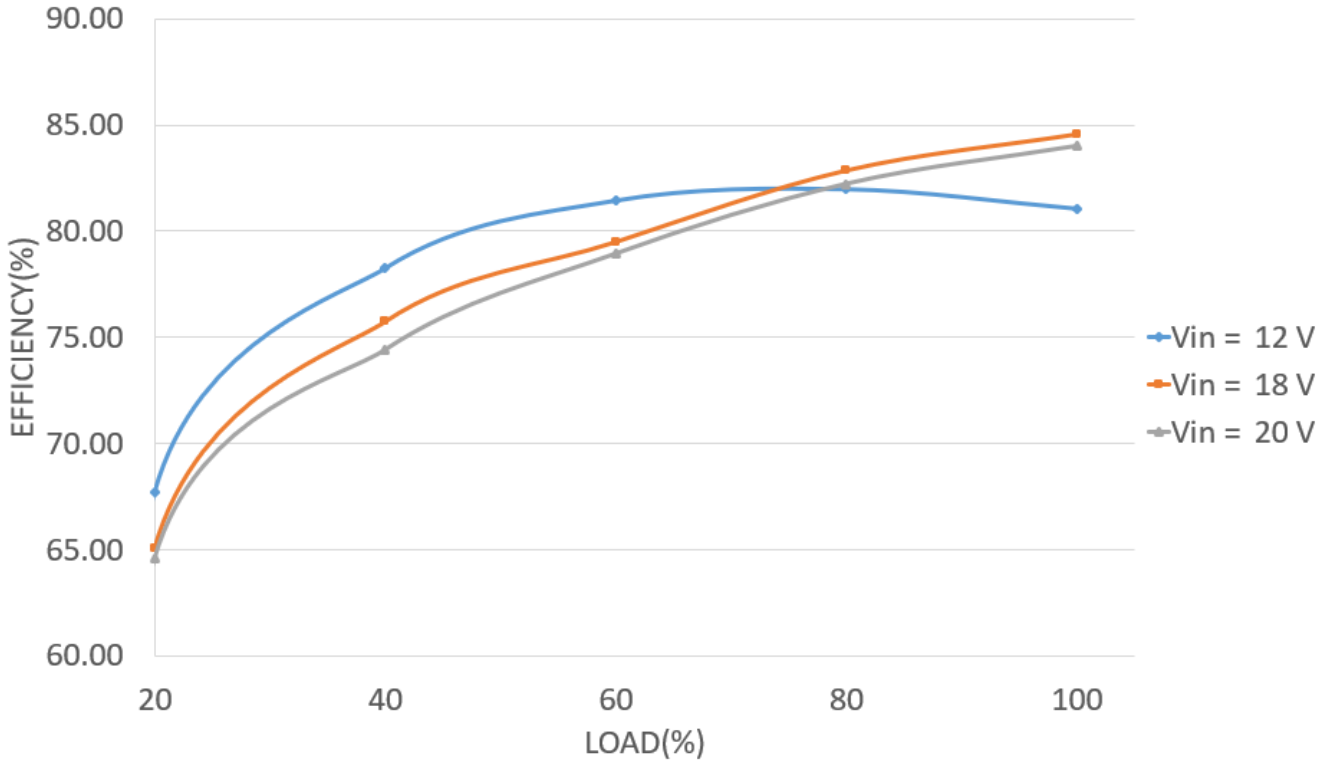


Figure 2-1. Average Efficiency for 10 V, 12 V, 18 V, 20 V

2.2 Cross Regulation

Figure 2-2 and Figure 2-3 illustrate the PMP40994 cross-regulation graphs.

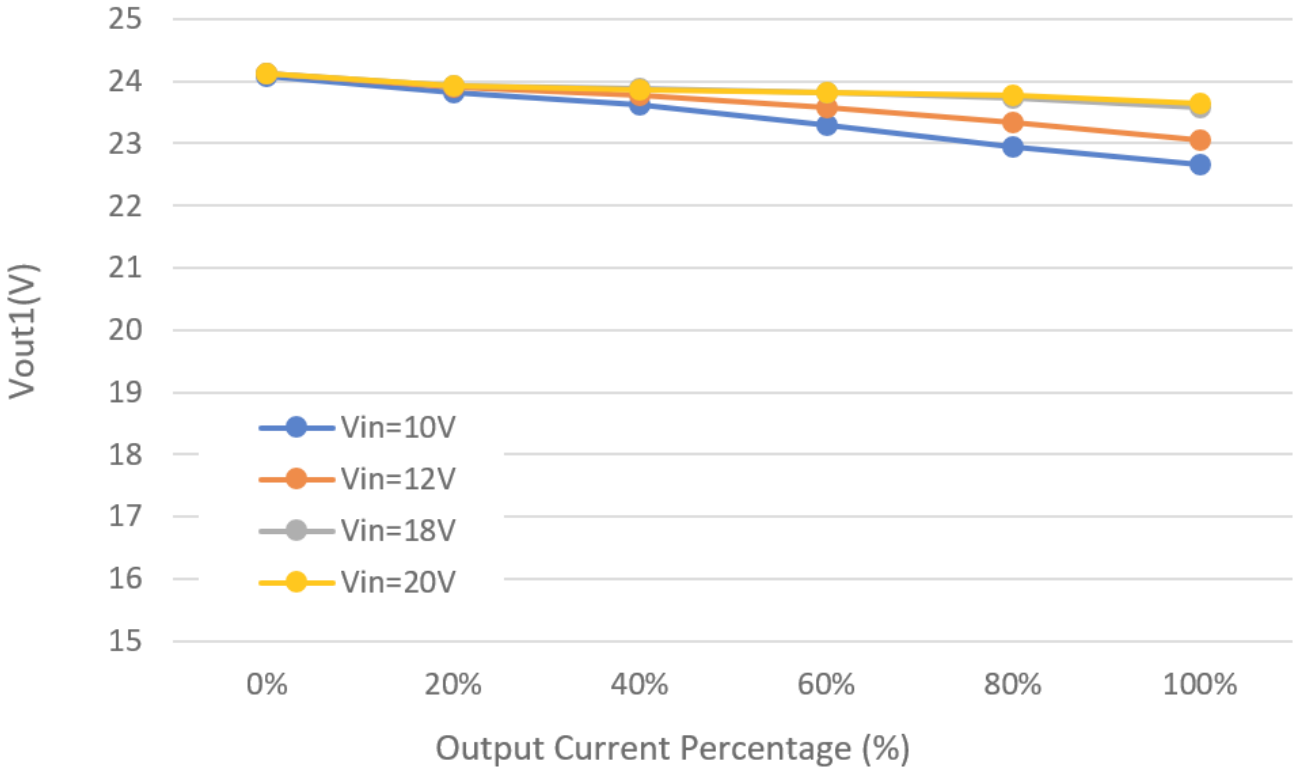


Figure 2-2. Isolated V_{OUT1} and V_{OUT2} Regulation With Same Percentage Current (Vout1)

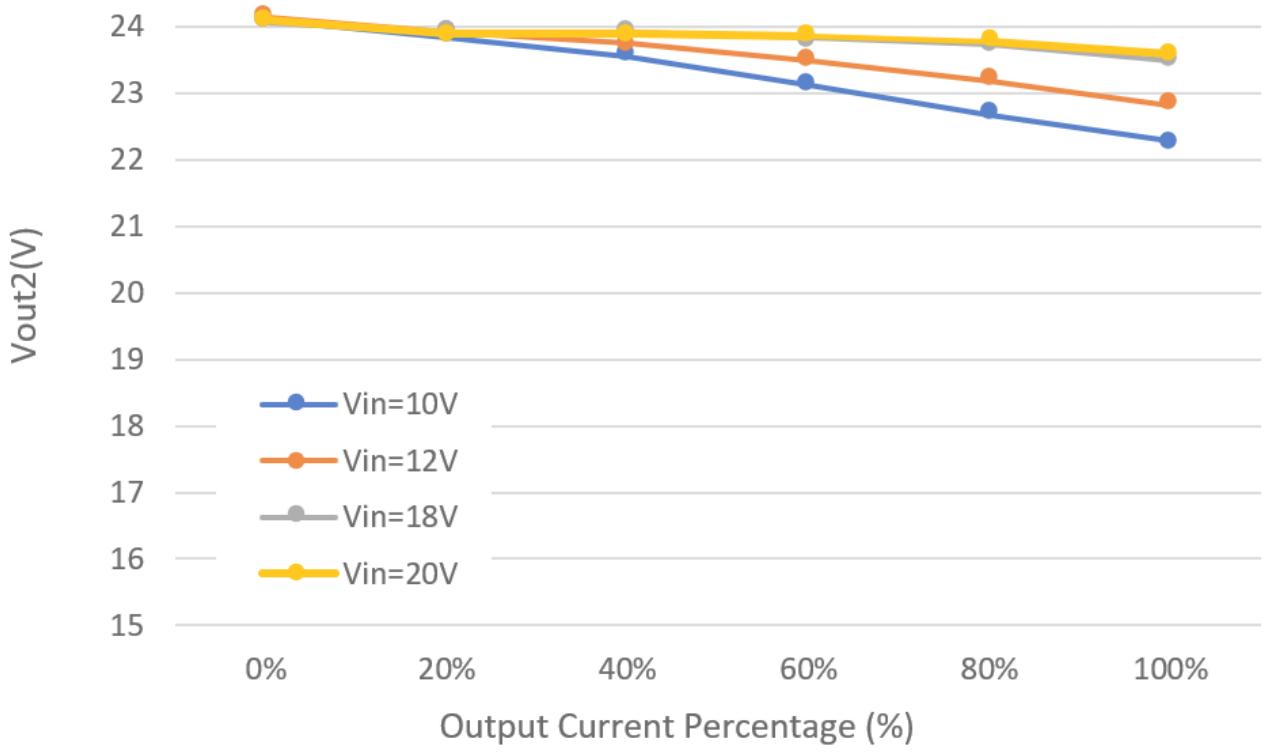


Figure 2-3. Isolated V_{OUT1} and V_{OUT2} Regulation With Same Percentage Current (Vout2)

2.3 Thermal Images

All thermal images were captured in 25ºC ambient, after a 30-minute warm up.

The following thermal images are at V_{IN} = 10 V, I_{OUT1} = 80 mA, and I_{OUT2} = 80 mA.

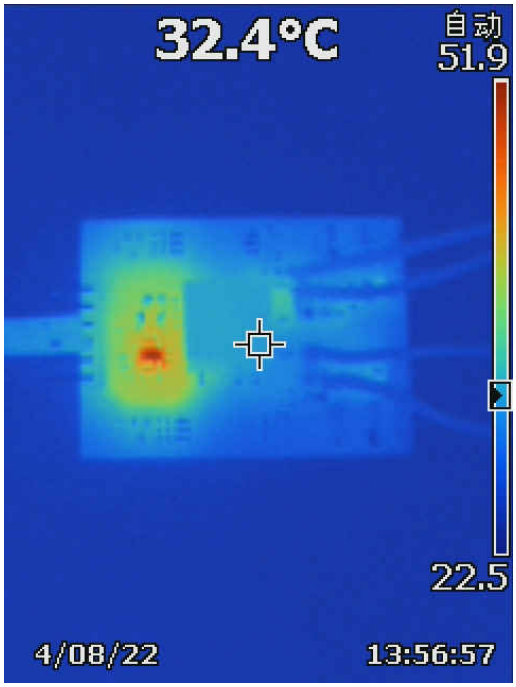


Figure 2-4. Top

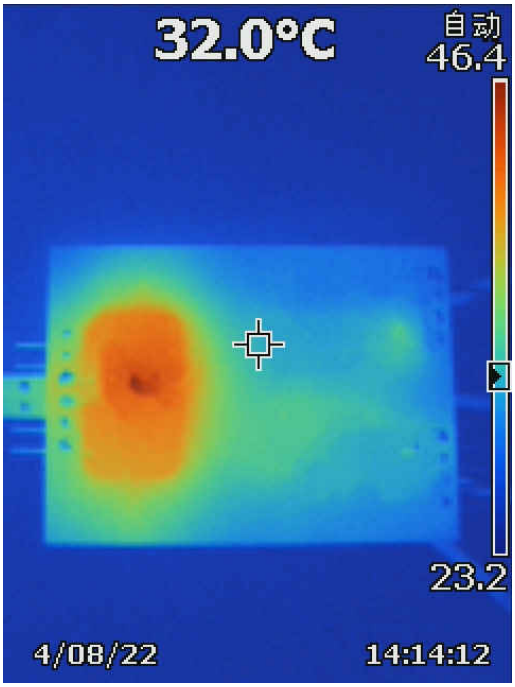


Figure 2-5. Bottom

The following thermal images are at V_{IN} = 12 V, I_{OUT1} = 80 mA, and I_{OUT2} = 80 mA.

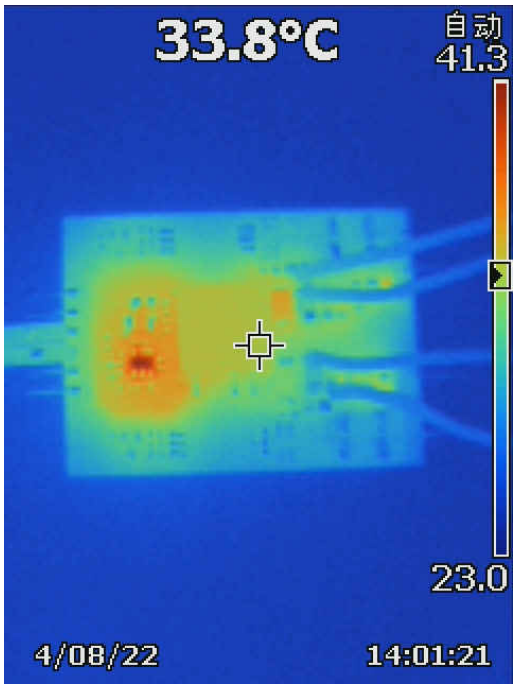


Figure 2-6. Top

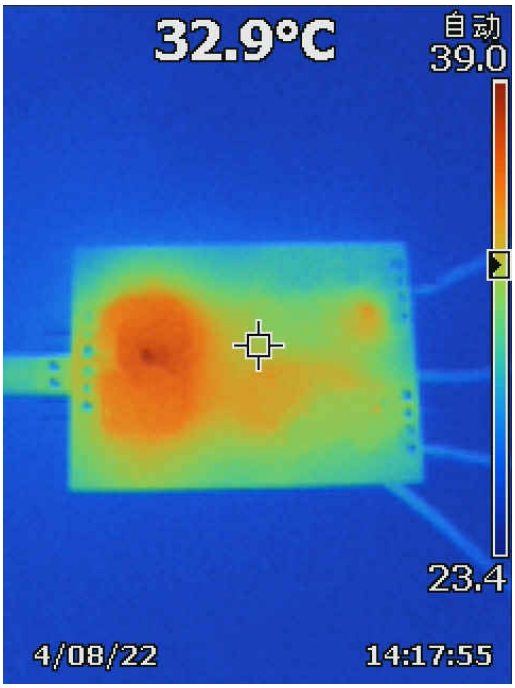


Figure 2-7. Bottom

The following thermal images are at V_{IN} = 20 V, I_{OUT1} = 80 mA, and I_{OUT2} = 80 mA.

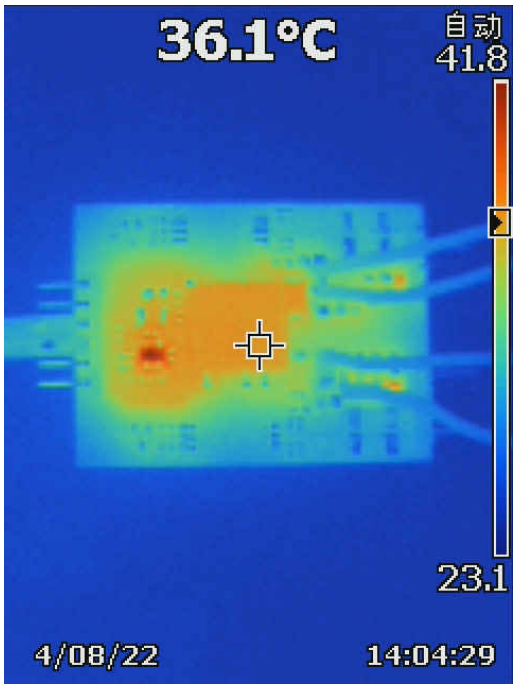


Figure 2-8. Top

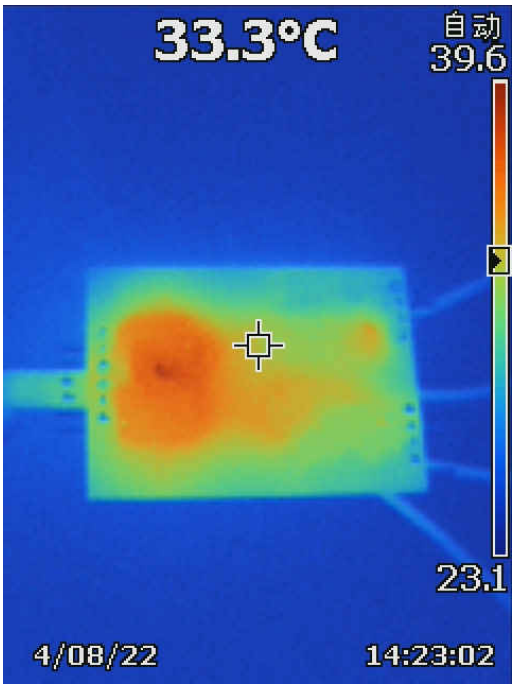


Figure 2-9. Bottom

3 Waveforms

3.1 Start-Up

The following images show the PMP40994 start-up waveforms.

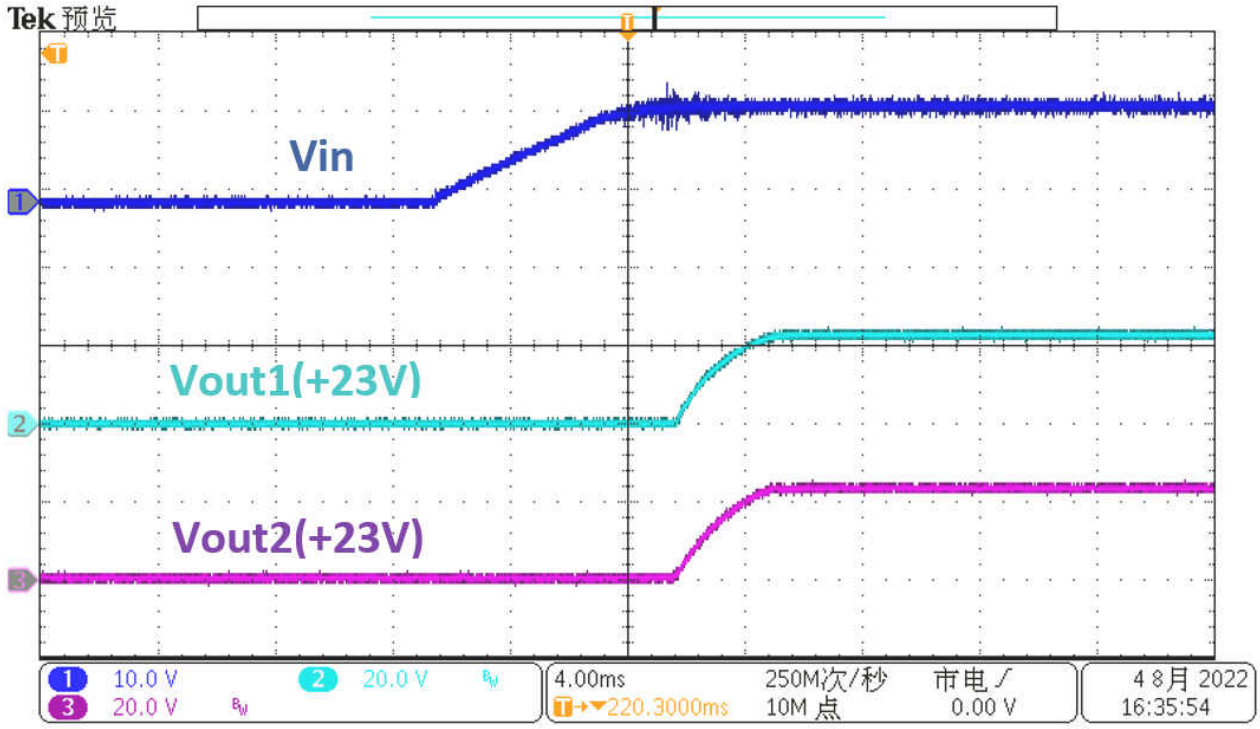


Figure 3-1. 12-V_{IN} Dual-Channel Output Start-Up Waveforms

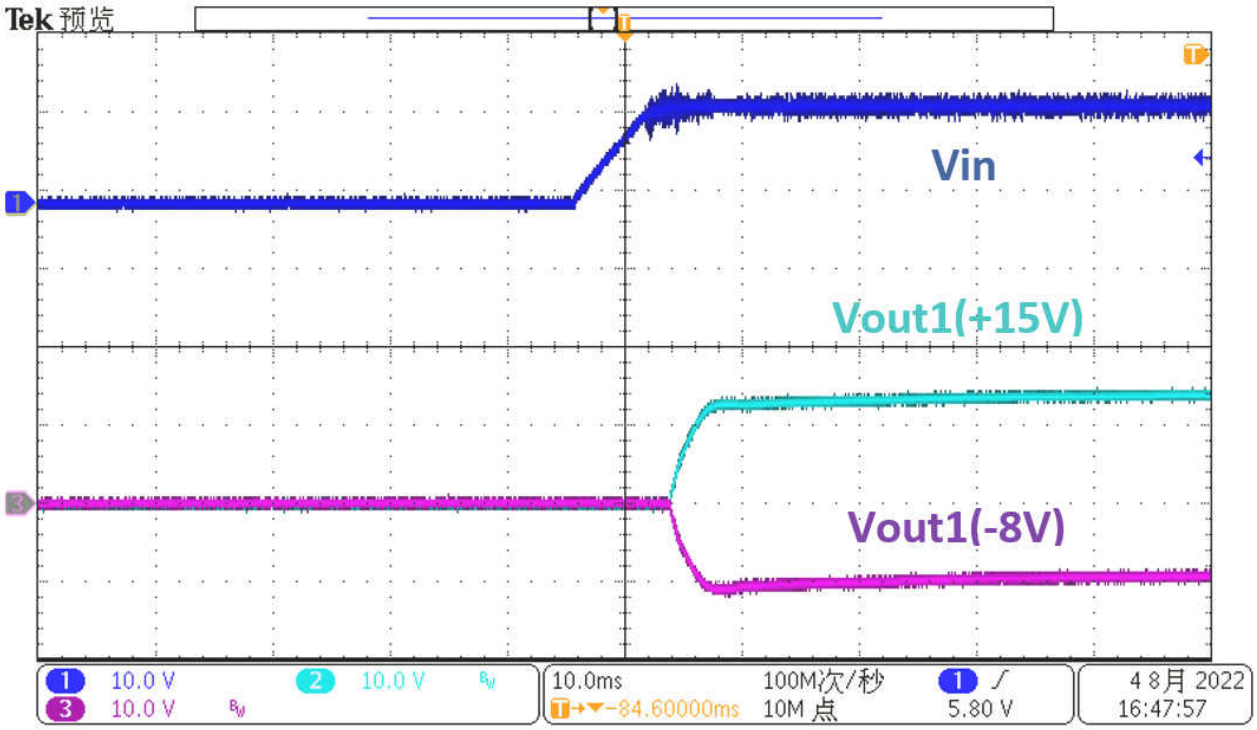


Figure 3-2. Channel A, +15 V, –8-V Output Start-Up Waveforms

3.2 Undervoltage Protection

The following images illustrate the PMP40994 power-off waveforms.

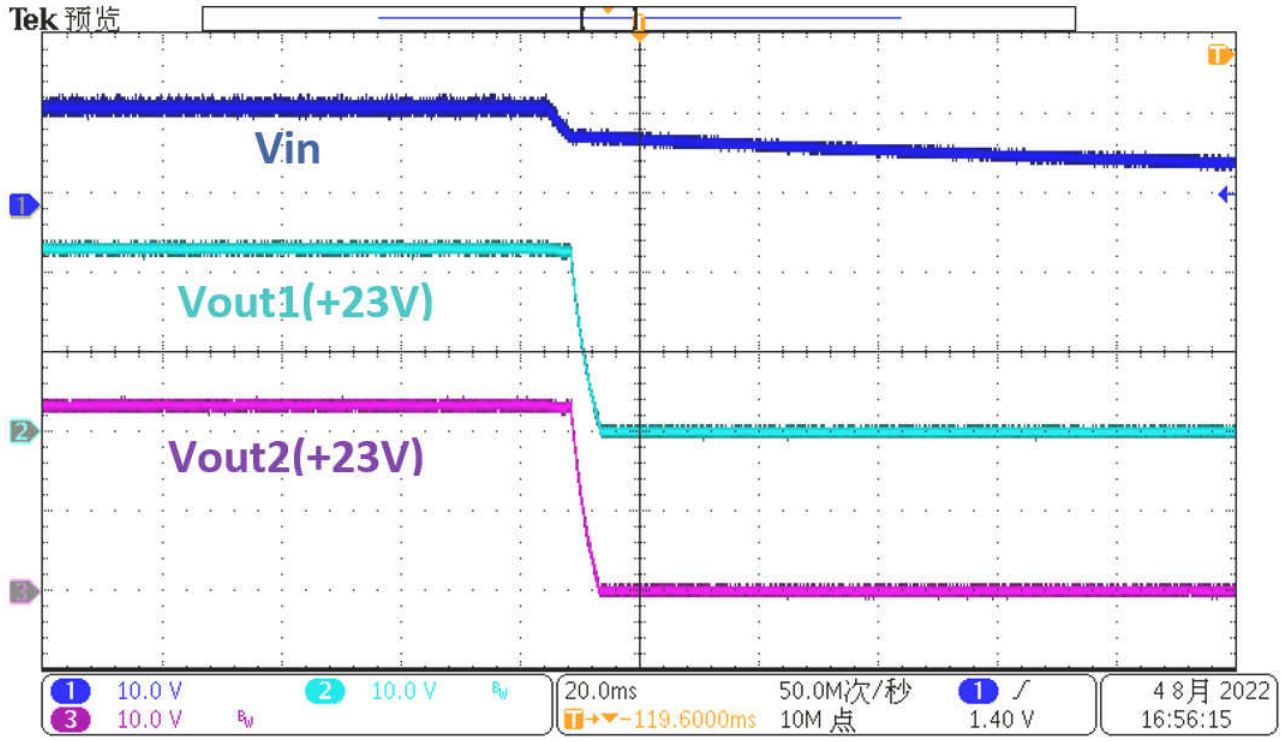


Figure 3-3. Two-Channel Power-Off Waveform of +23-V Output With V_{IN} = 12 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

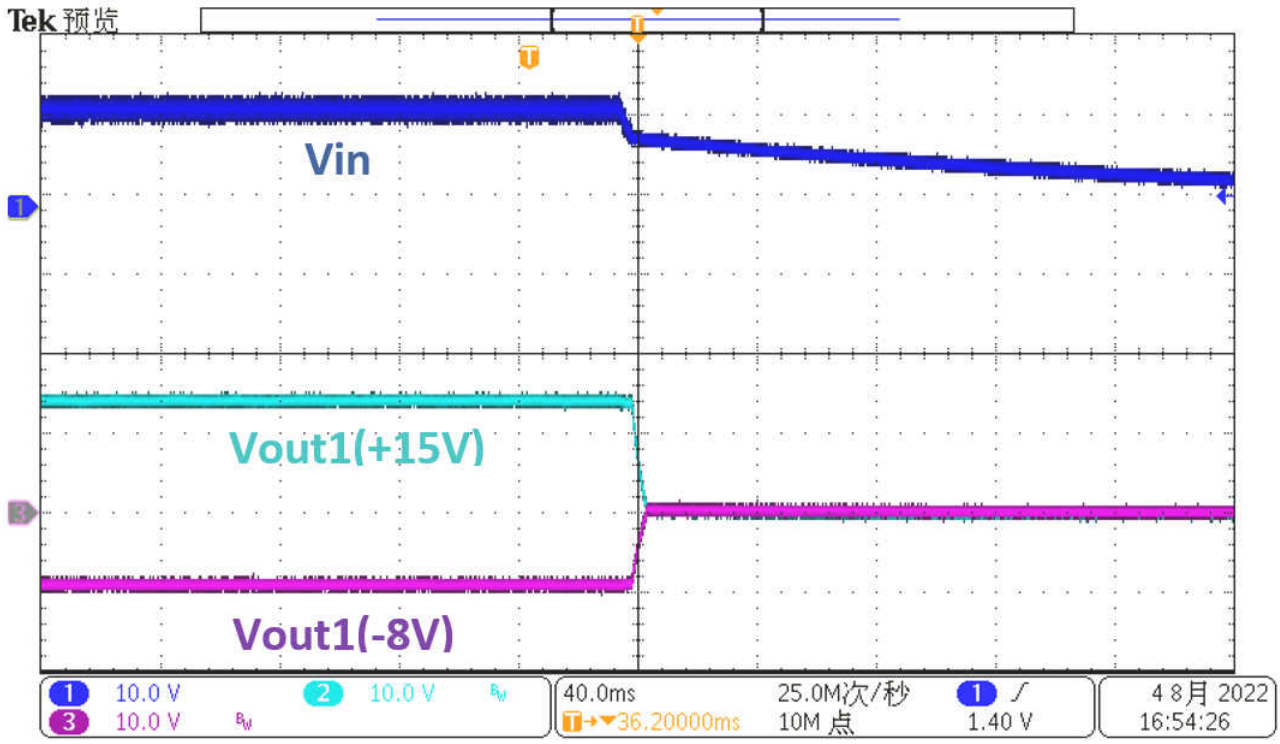


Figure 3-4. V_{OUT1} Channel Power-Off Waveform of +15-V, 8-V Output With V_{IN} = 12 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

3.3 Output Voltage Ripple

Figure 3-5 through Figure 3-7 show the output voltage ripple waveforms at the conditions indicated in the image title.

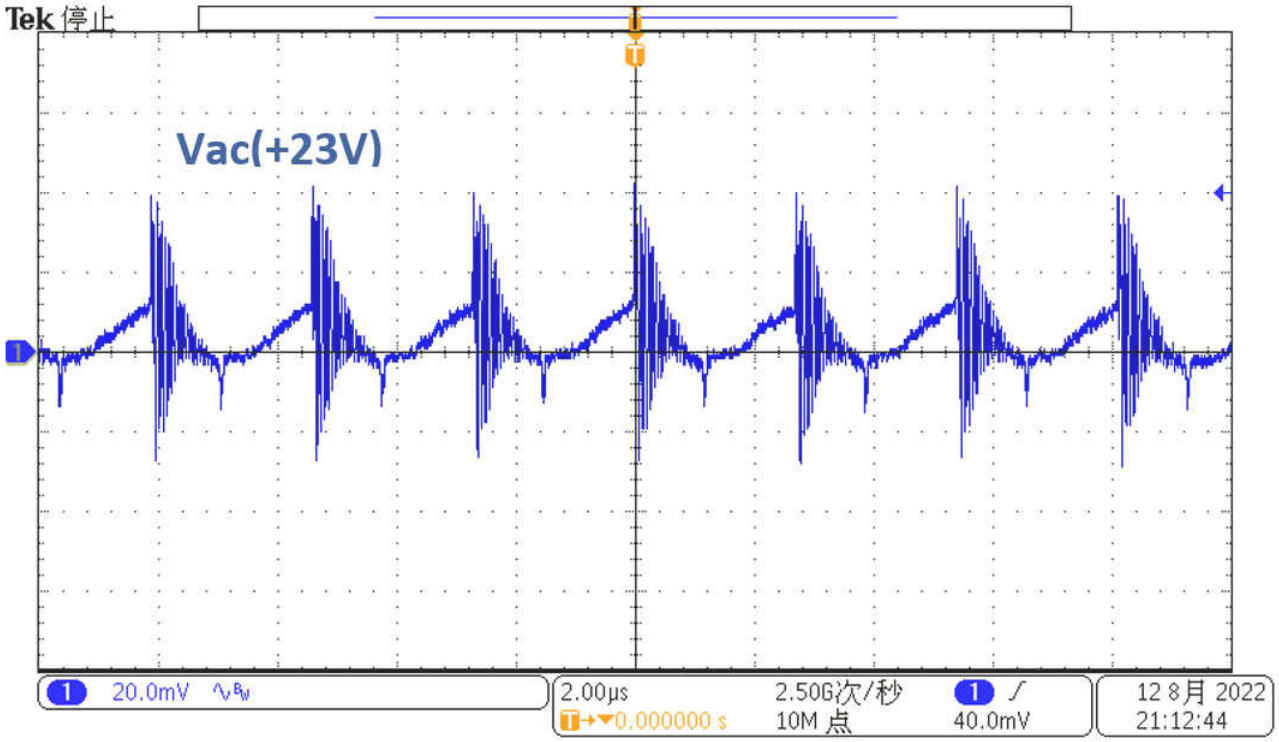


Figure 3-5. V_{OUT1} +23-V Output Ripple, V_{IN} = 12 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

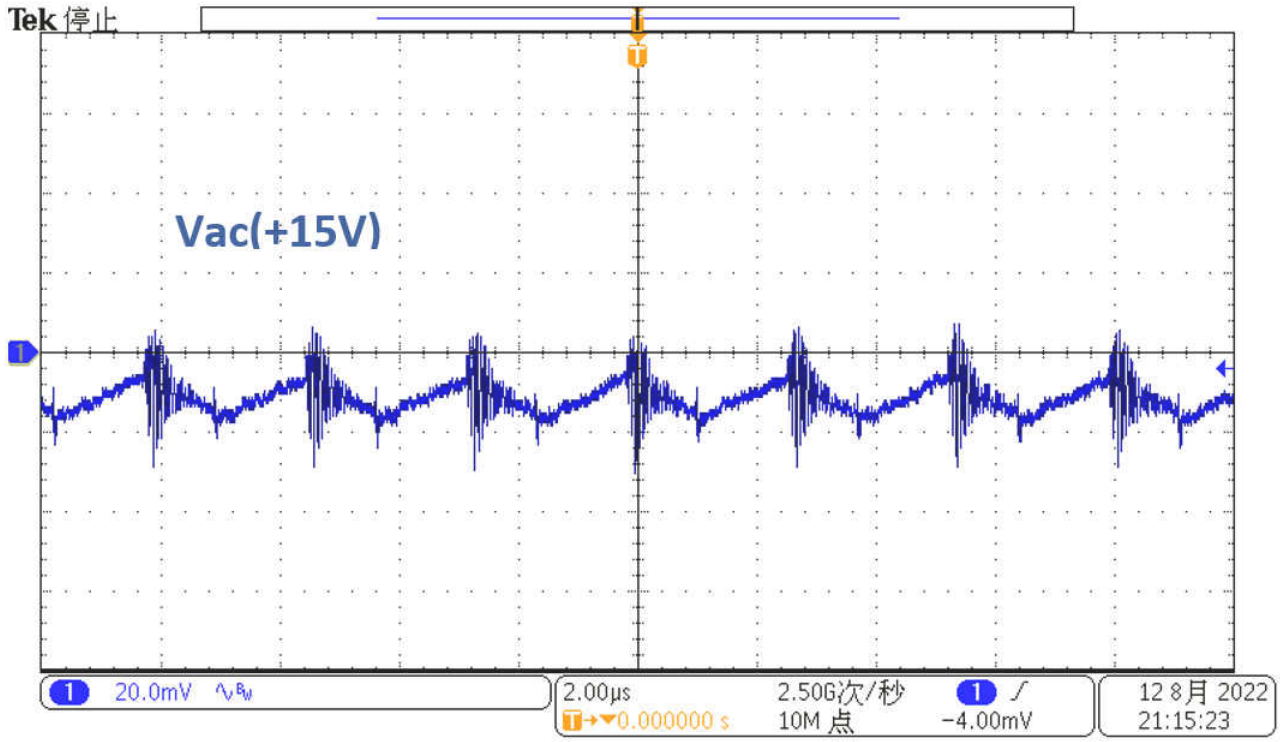


Figure 3-6. V_{OUT1} +15-V Output Ripple, V_{IN} = 12 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

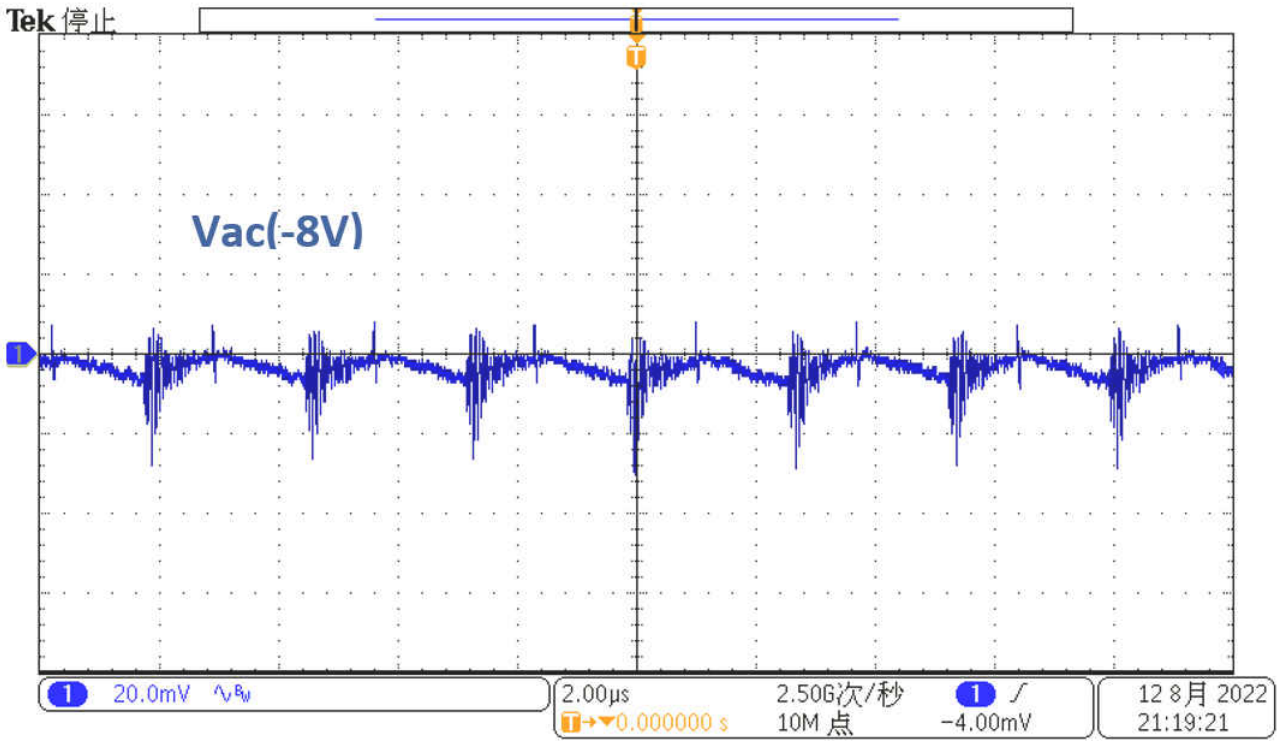


Figure 3-7. V_{OUT1} –8-V Output Ripple, V_{IN} = 12 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

3.4 Load Transients

Figure 3-8 through Figure 3-10 show the PMP40994 load transient waveforms.

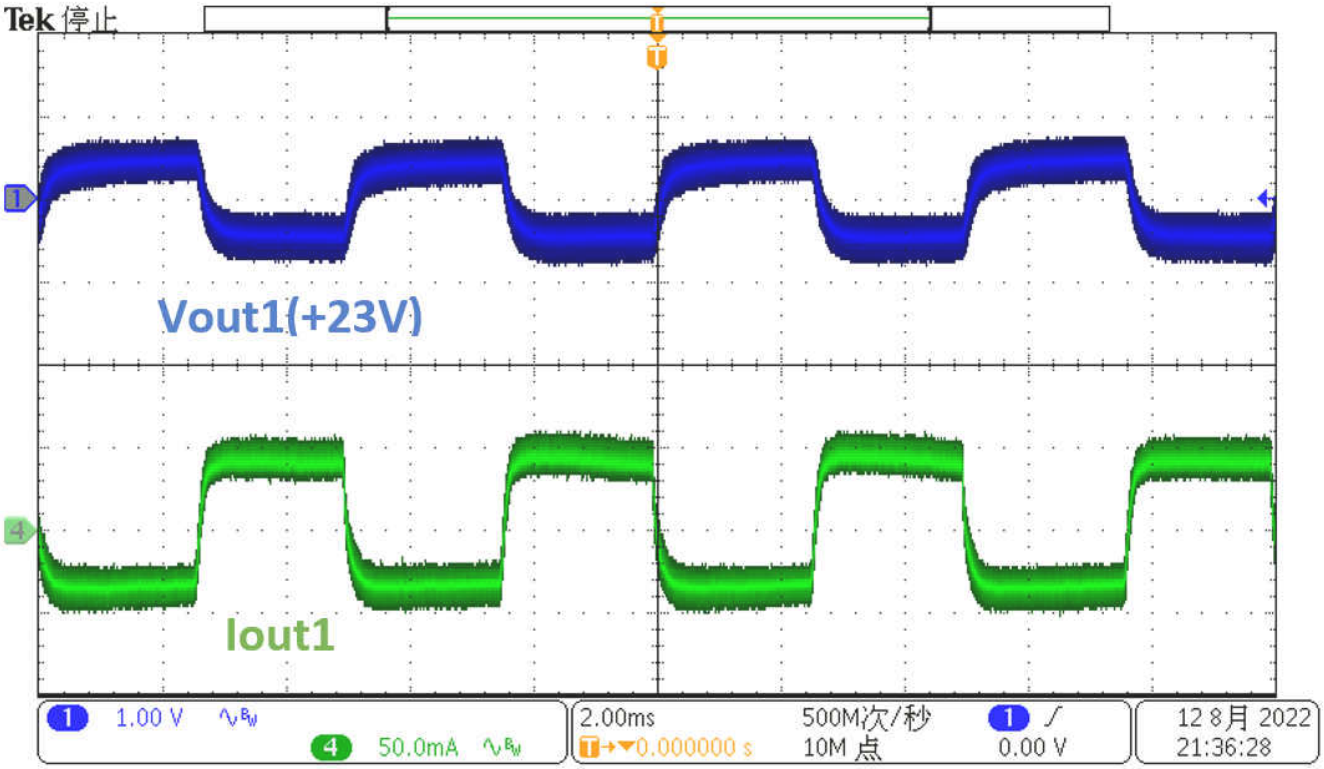


Figure 3-8. +23-V Output Load Transient at 12-V Input From 0 mA to 80 mA

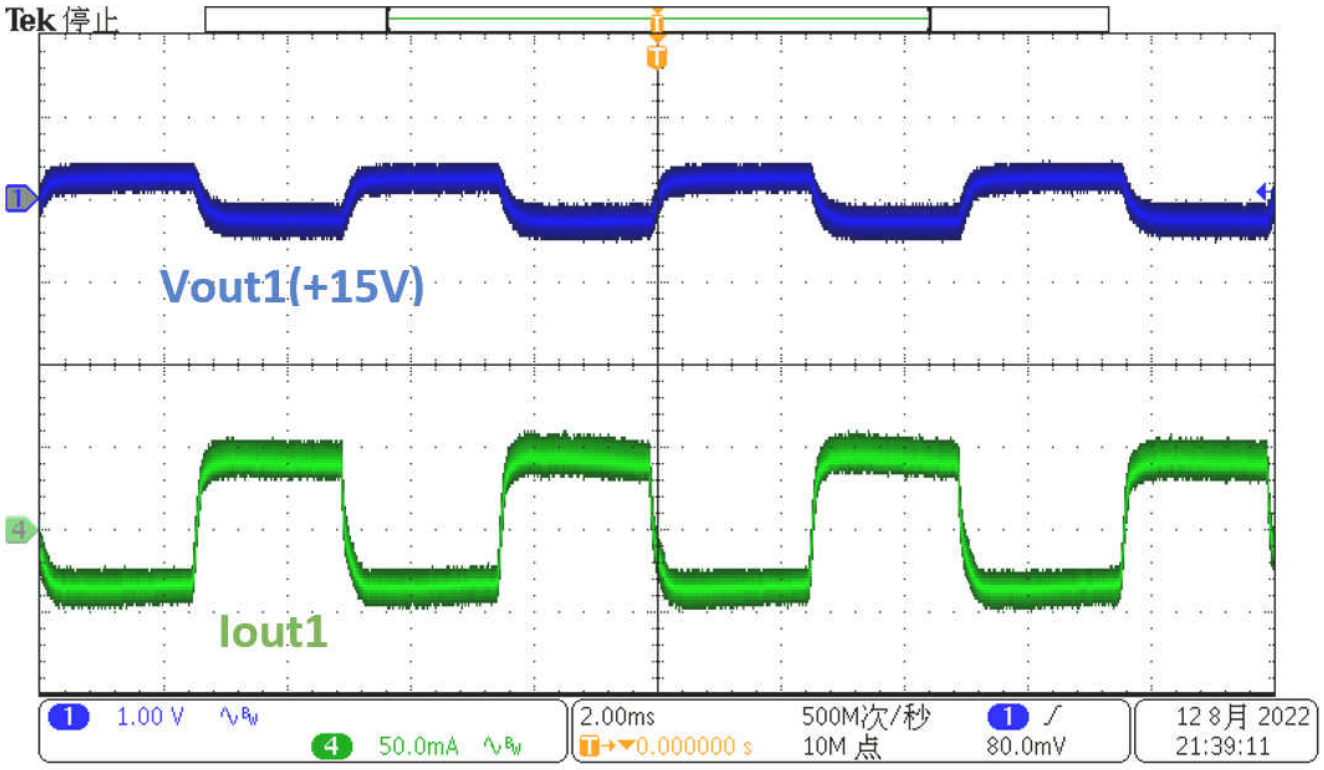


Figure 3-9. +15-V Output Load Transient at 12-V Input From 0 mA to 80 mA

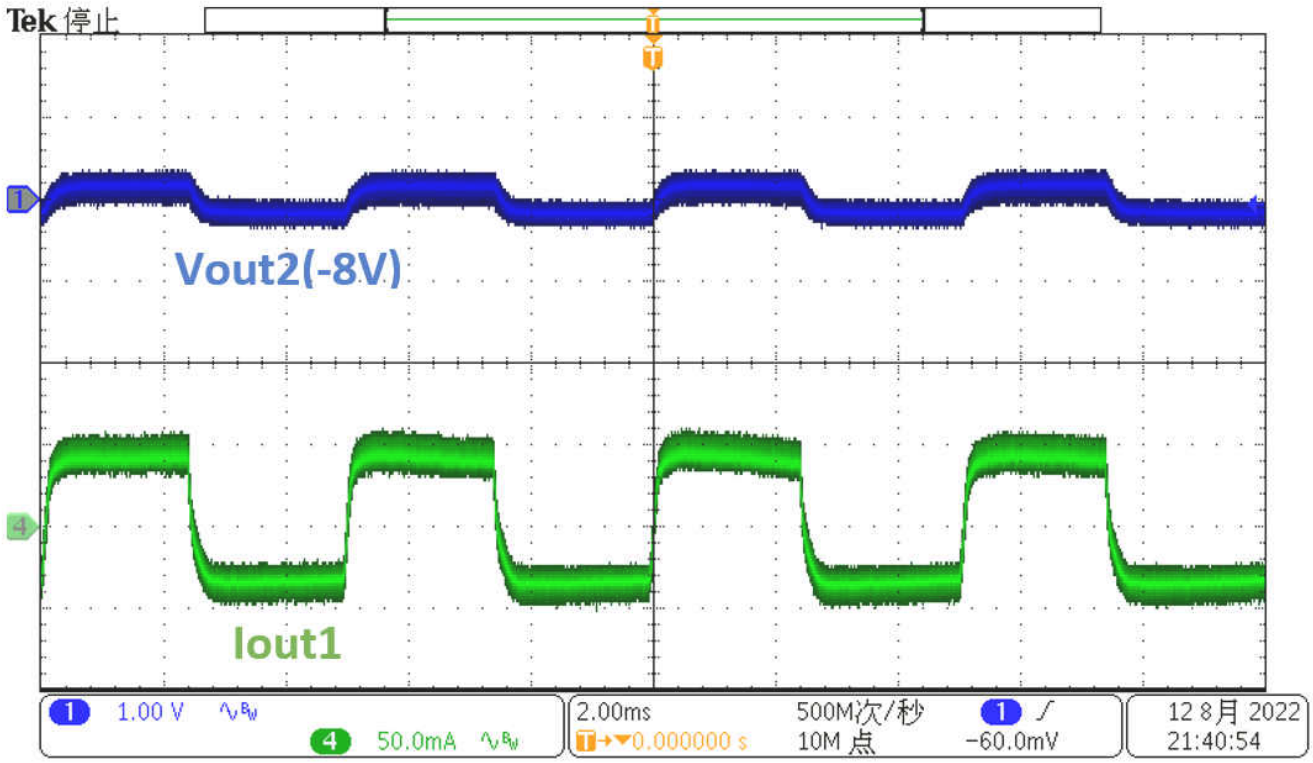


Figure 3-10. –8-V Output Load Transient at 12-V Input From 40 mA to 80 mA

3.5 Switching Node Waveforms

The following images show the PMP40994 switching node waveforms.

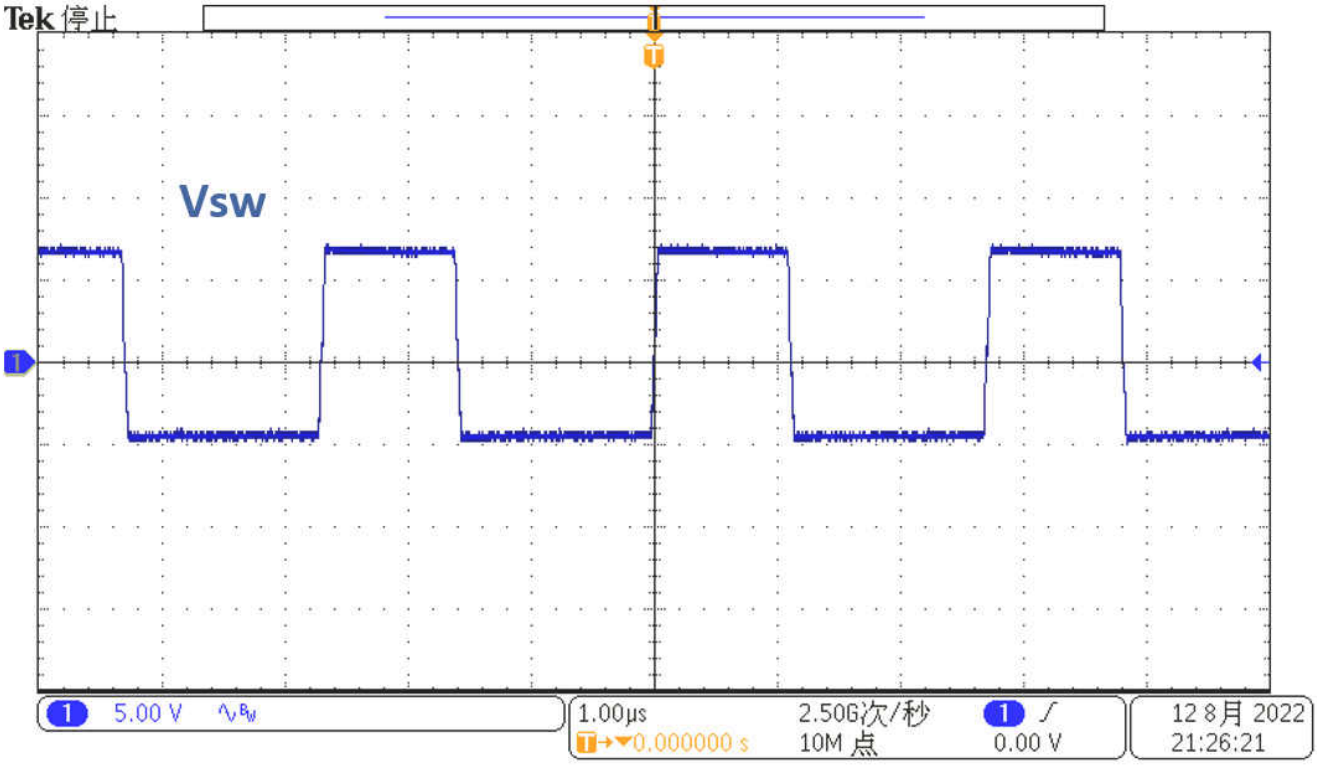


Figure 3-11. Switch Node Voltage, V_{IN} = 12 V, I_{OUT1} = 0 A, I_{OUT2} = 0 A

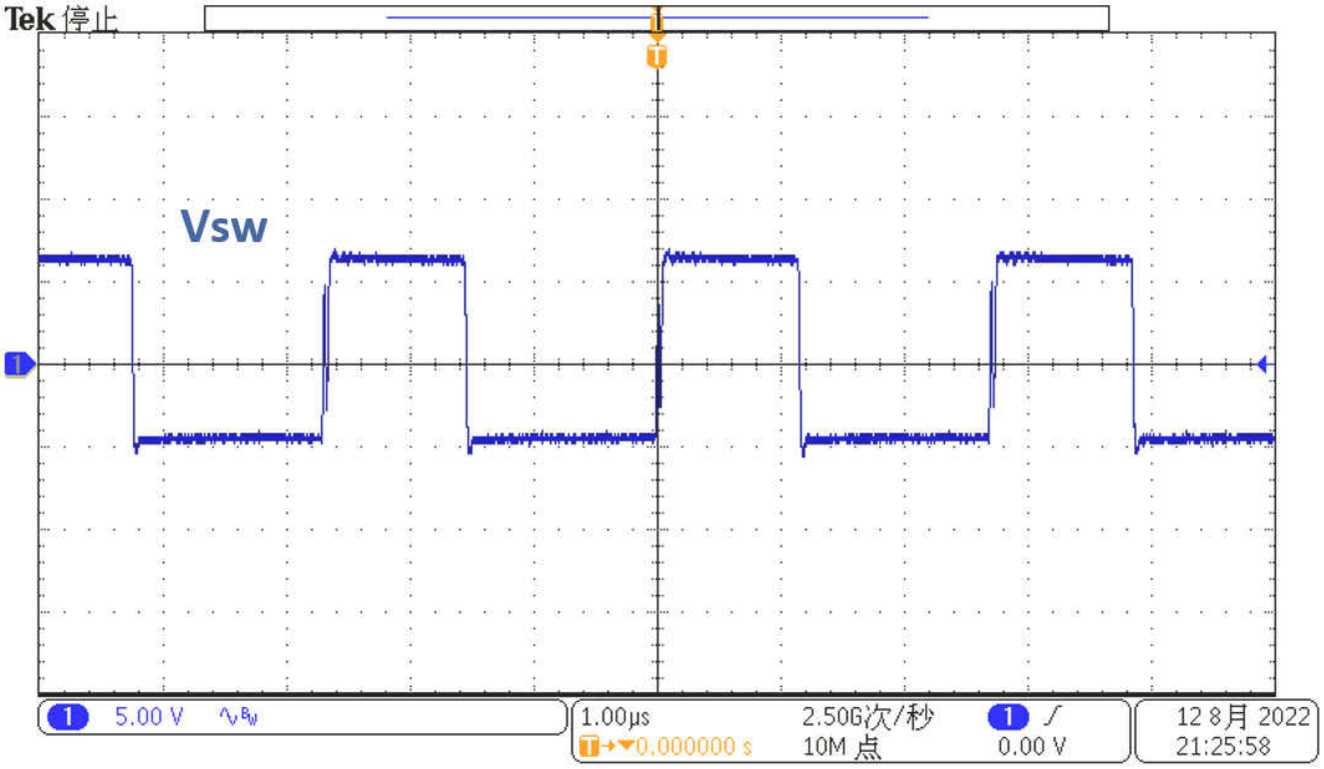


Figure 3-12. Switch Node Voltage, V_{IN} = 12 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

3.6 Short-Circuit Test

The following images show the PMP90994 short-circuit waveforms.

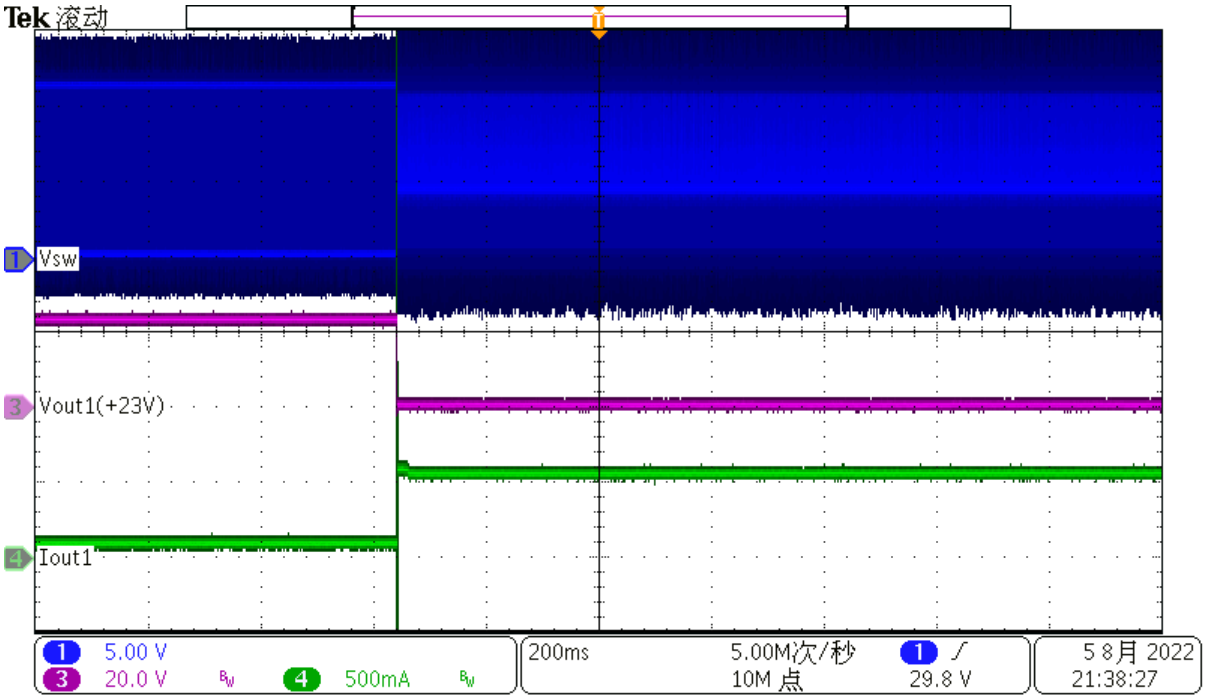


Figure 3-13. Output Short From Double Full-Load Operation To Short Circuit at 12-V Input (+23-V Rail Short Circuit)

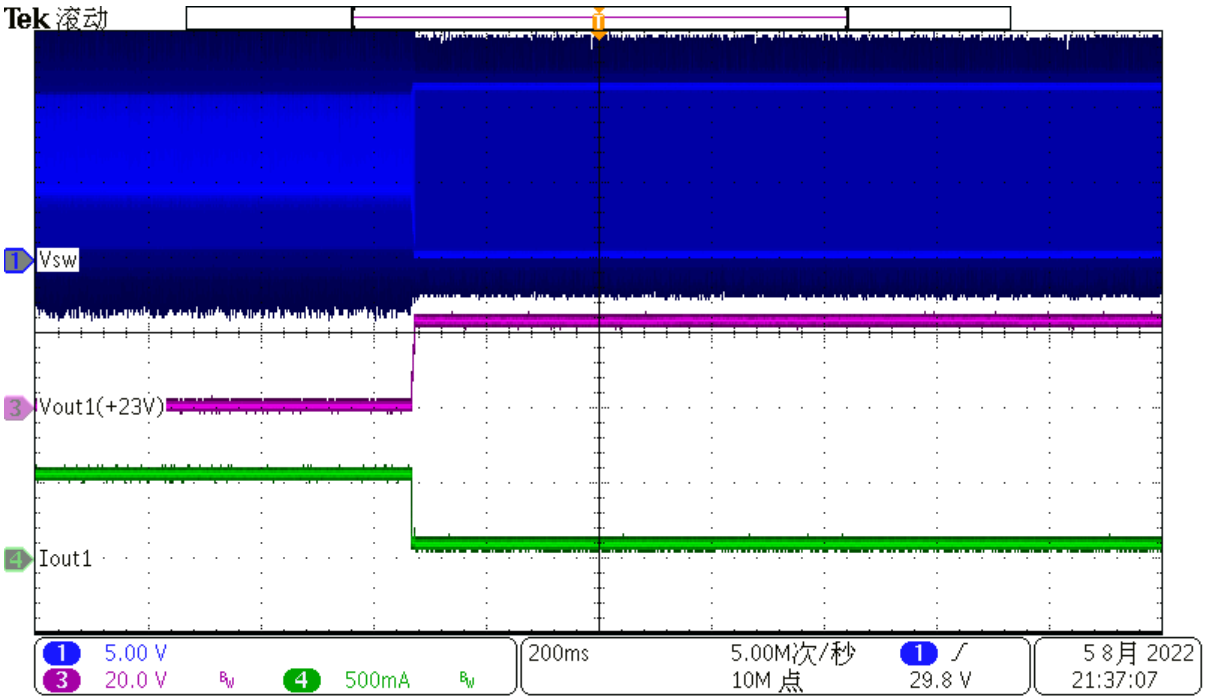


Figure 3-14. Output Short Removed Into Double Full-Load Operation at 12-V Input (+23-V Rail Short-Circuit Release)

3.7 Diode Voltage Stress

Figure 3-15 through Figure 3-18 show the PMP90994 diode voltage stress waveforms.

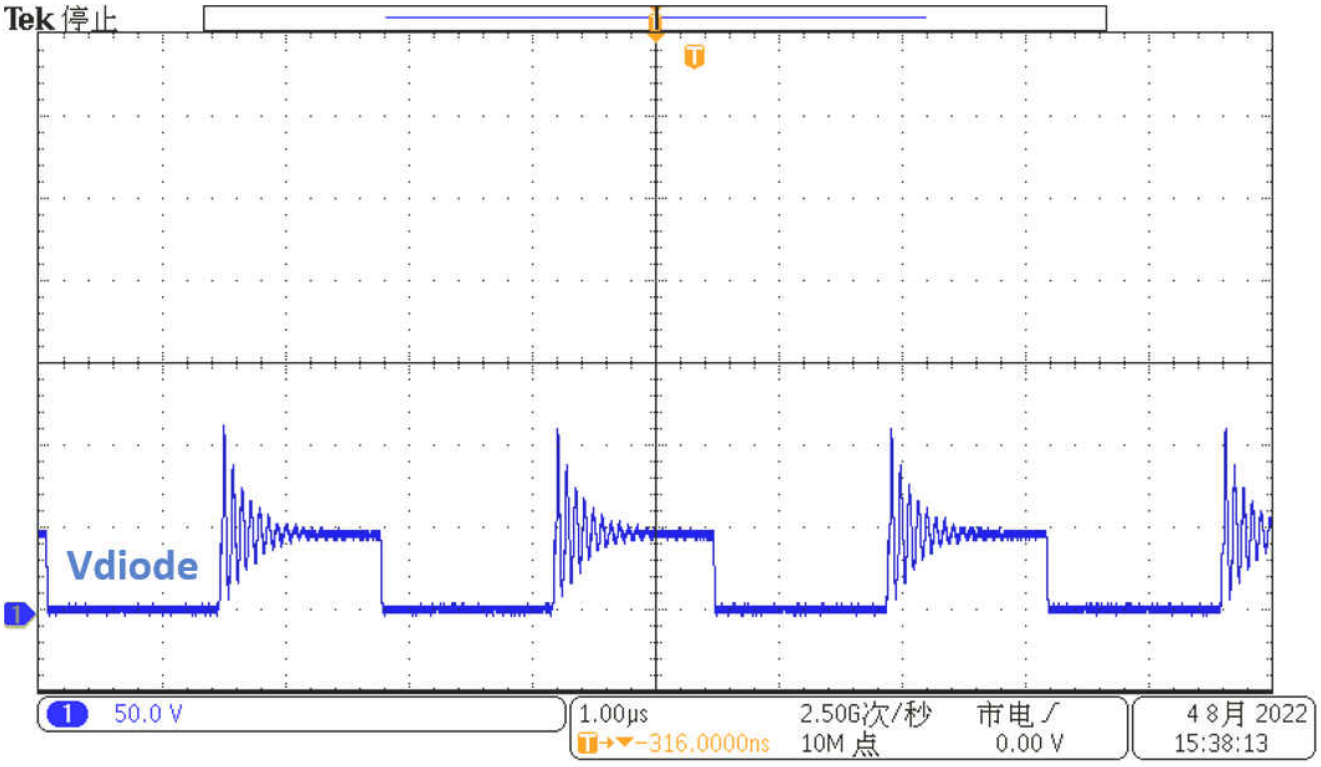


Figure 3-15. Channel A Diode Voltage Stress V_{IN} = 10 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

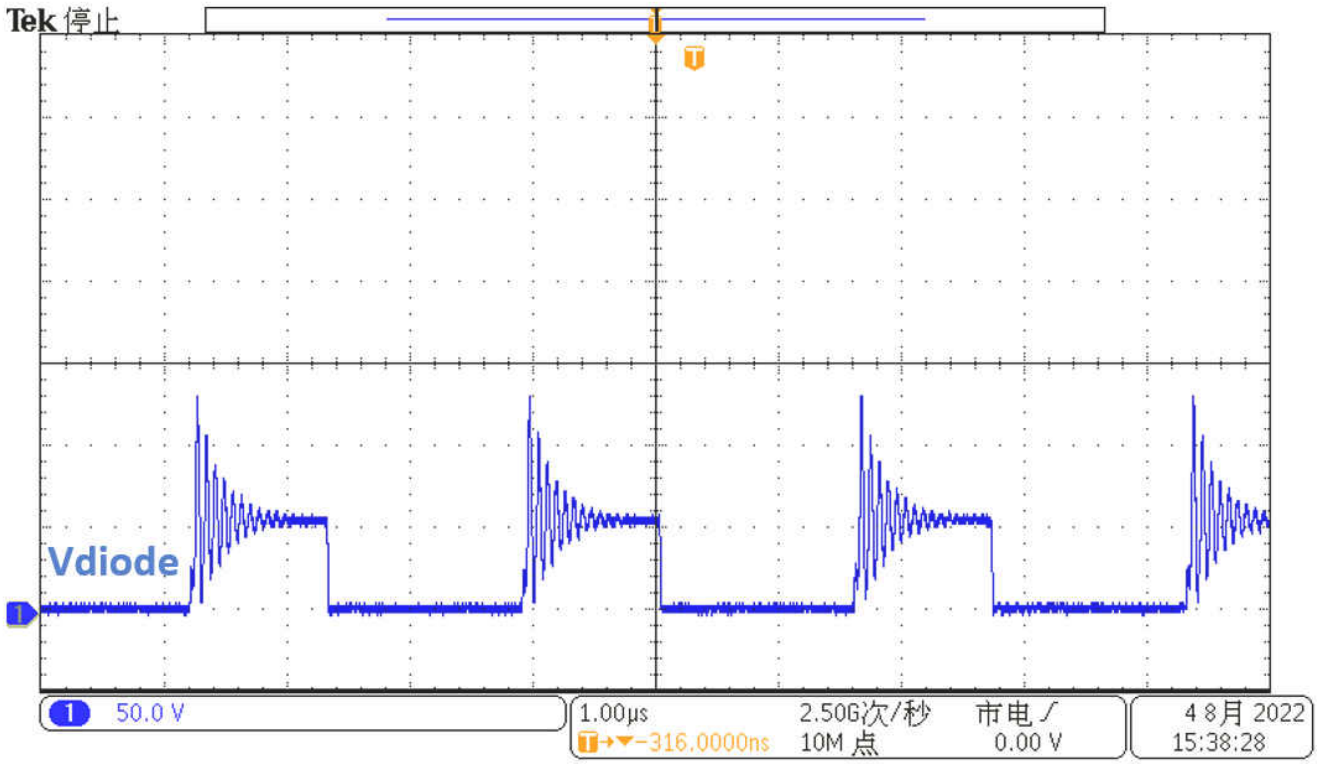


Figure 3-16. Channel A Diode Voltage Stress V_{IN} = 12 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

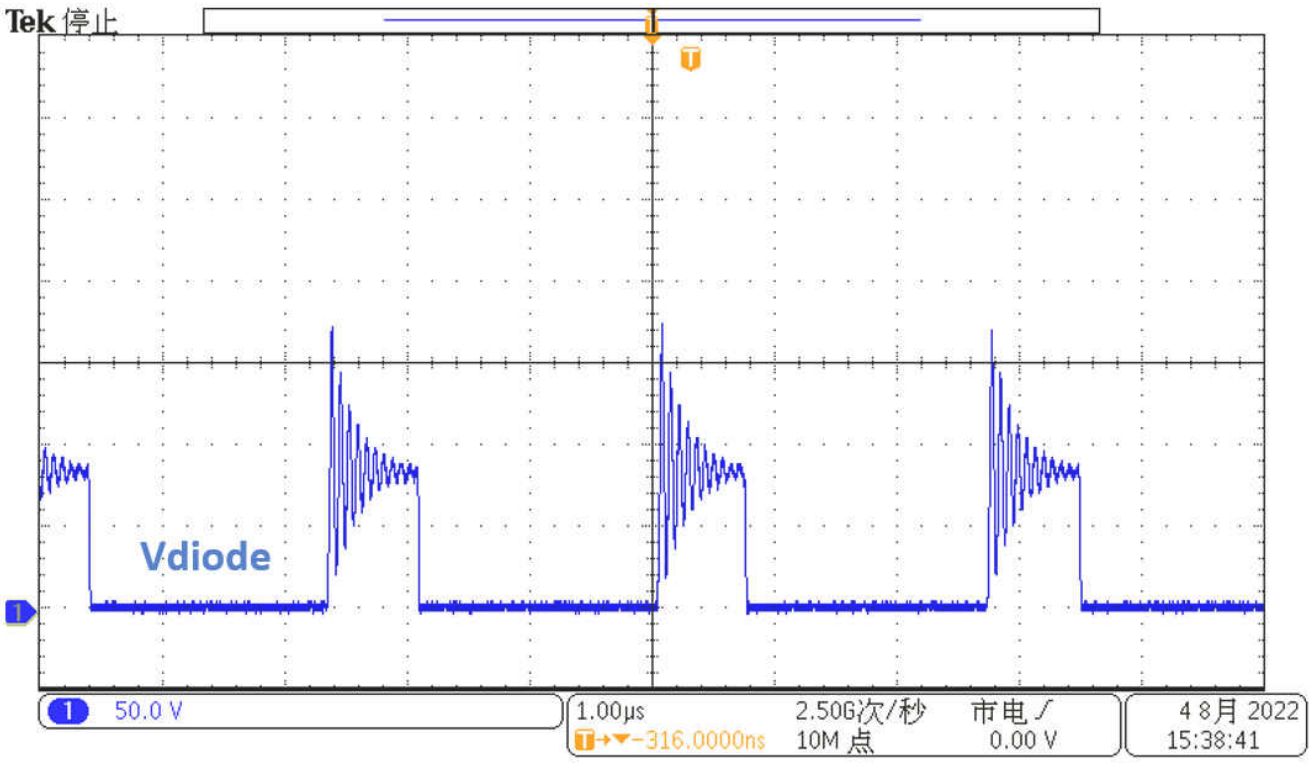


Figure 3-17. Channel A Diode Voltage Stress V_{IN} = 18 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

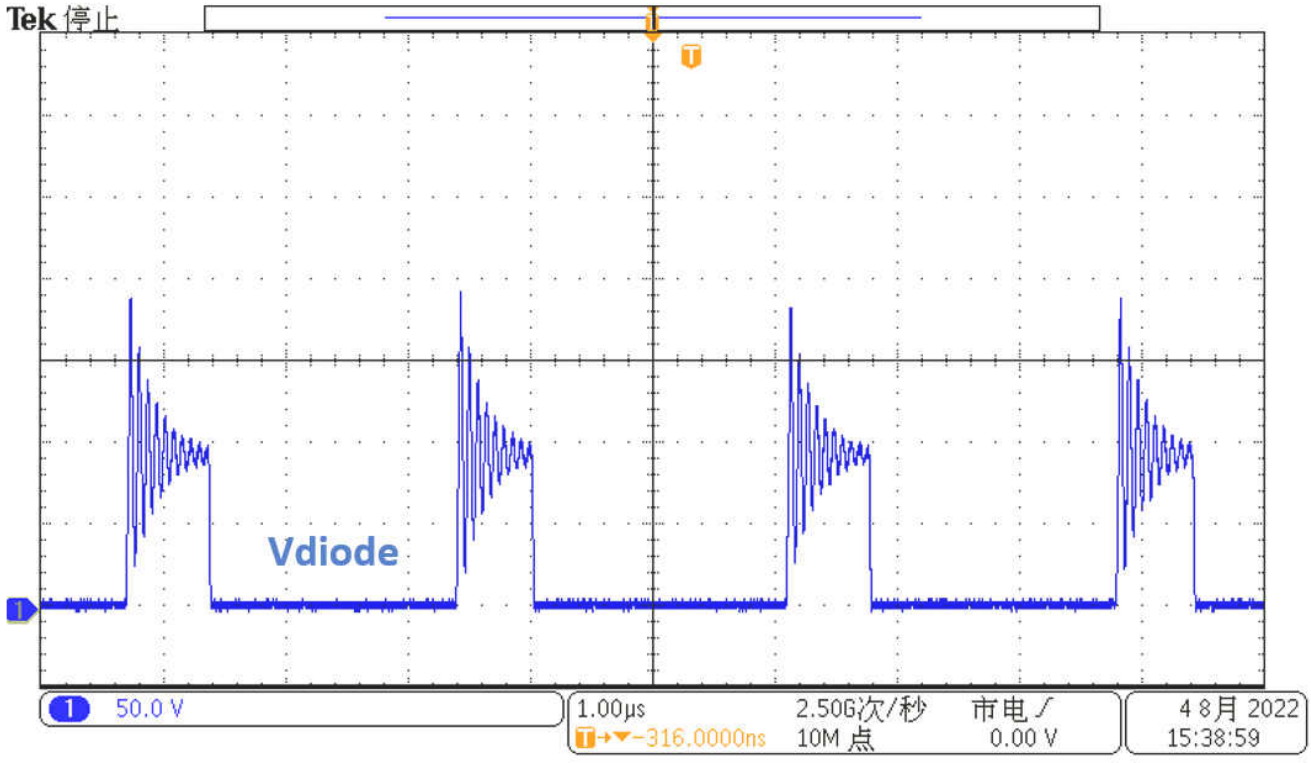


Figure 3-18. Channel A Diode Voltage Stress V_{IN} = 20 V, I_{OUT1} = 80 mA, I_{OUT2} = 80 mA

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