TI Designs

High-Accuracy AC Voltage and Current Measurement AFE for Feeder Terminal Unit Reference Design

TI Designs

This TI Design solution addresses the analog front-end needs for merging units, protection relays, DTUs, FTUs, and bay control units that require measurement of multiple voltage and current inputs (16 or more) accurately over wide input range using a simple serial peripheral interface (SPI). Using the ADS8688/ADS8688A ADC, the need for external signal conditioning of the analog input can be minimized based on the application and the input signal level. This AFE design implementation is modular, allowing easy expansion of channels while at the same time keeping the connectivity to the processor minimal by using the SPI daisy chain feature of the ADS8688/ADS8688A ADC.

Design Resources

TIDA-00307	Design Page
ADS8688	Product Folder
ADS8698	Product Folder
ADS8668	Product Folder
CSD17571Q2	Product Folder
TPS70933	Product Folder
TPS70950	Product Folder
ADS8688A	Product Folder
ADS8678	Product Folder

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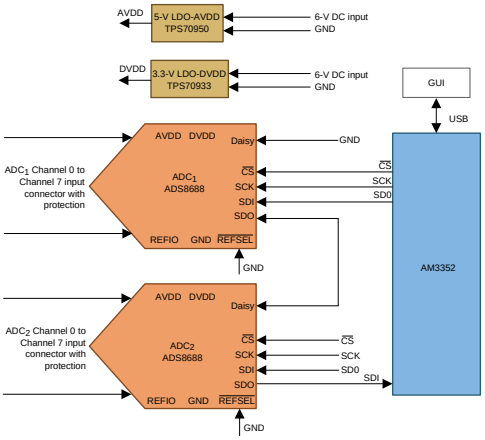
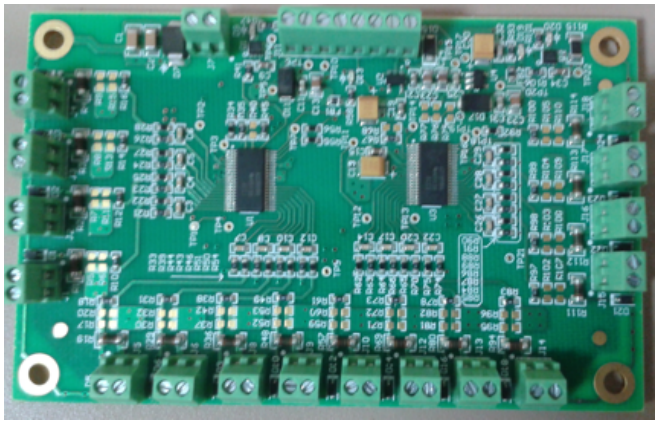
Design Features

- Design is based on ADS8688 (16-bit SAR ADC)
- ADC offers SPI to the host
- Design compatible with ADS8688A, ADS8678, ADS8668
- Two ADCs have been daisy chained to increase the number of inputs
- Based on ADC selection, ±10.24 V, ±5.12 V, ±2.56 V, ±1.28 V, and ±0.64 V programmable input ranges available for accurate measurement of low amplitude input signals
- Data output: 500K samples
- Additional ADC channel without PGA (AUX_IN)
- Dual and single supply operation
- Input overvoltage protection: up to ±20 V
- On-Chip, 4.096-V reference with low drift
- AC sensor inputs with 50, 60, or 400 Hz can be used; Ranges compatible to electronic current transformer output requirements as per IEC60044-8

Featured Applications

- Merging Units for Smart Grid applications
- Multi-function protection relays
- Power Quality Analyzer
- FTU, DTU, or RTU





1 System Description

1.1 Issues With the Existing Grid

An electrical grid is an enormous and extremely complex system consisting of centralized power plants, transmission lines, and distribution networks. An electrical grid is capable of carrying gigawatts (GW) of power while continuously balancing supply with fluctuating demand with remarkable reliability, providing little downtime.

Smart grid technologies have addressed the following electrical grid issues:

- Power outages and disruptions in the quality of power
- Inefficiency with managing peak loads
- No support for robust information flow
- Limited support for distributed generation

1.2 Smart Grid

Although access to electricity has enabled major advancements in technology, which has in turn driven an increase in the demand for electricity, little has changed in how electricity is generated, transmitted, and distributed to consumers. The term *smart grid* refers to new technology that brings the century-old method of electricity generation and distribution into the 21st century through computerized automation and control.

The smart grid technology builds upon the current grid system but uses digital technology that enables two-way communication between a power distribution utility company and customers. The ability for two-way communication creates an automated and widely-distributed electricity network that can protect, monitor, and optimize the operation of the interconnected components. This new automated network allows for utility companies to respond more efficiently to customer demand, and enables consumers to take more control over their energy usage through increased access to information.

The smart grid is composed of a number of interconnected components that monitor use and share real-time data. One of the most important parts of the smart grid is smart meters. Similar to the standard meters connected to homes and offices, smart meters collect and provide utility companies information about energy use and consumption, however smart meters provide these data more frequently. Smart meters can also communicate with appliances and programs inside homes and workplaces. Smart meters enable both utility companies and consumers to know how much energy is being used in real-time.

Similar to how smart meters communicate between utility companies and consumers, smart transmission and distribution devices can allow utility companies and transmission or distribution centers to communicate with each other. This communication can help utility companies identify inefficiencies in the transmission and distribution processes, ultimately leading to significant cost savings for the utility company and reduced electricity rates for the consumer.

Characteristics of smart grid technologies enable many functions beyond the capabilities of the existing electrical. A smart grid does the following:

- Provides the utility company with actionable information
- Provides the consumer with actionable information
- Provides customers with information about their electricity usage patterns and costs
- Automates and decentralizes decisions
- Supports and enhances new technologies

The smart grid concept penetrates throughout the entire grid to include:

- Smart meters
- Smart feeders
- Smart substations

- Smart transmission
- Smart centralized generation

1.2.1 Key Technologies Used in Smart Grid Applications

Sensing and Measurement — Sensing and measurement allow utility companies and consumers to understand and react to the state of the electrical grid in real-time. For example, households can monitor their energy demand and the current price of electricity through smart meters, which communicate with home networks that link smart appliances and display devices.

Integrated Communications — High-speed, standardized, two-way communication allows for real-time information flows and decision-making among all grid components. Several existing technologies, including wide-area wireless internet and cellular networks, could provide the required communications infrastructure.

Advanced Components — Advanced components such as GPS systems, current-limiting conductors, advanced energy storage, and power electronics will improve generation, transmission, and distribution capacity and operational intelligence for utility companies.

Advanced Control Methods — The task of managing an electrical grid becomes more complex as more information becomes available to grid controllers and faster response times are required. Advanced control systems find and process important information quickly, streamlining operations and providing clarity to human operators.

1.2.2 Key Applications of Smart Grid Technologies

The smart grid technologies that form the foundation of a new grid enable new smart grid applications, including the following:

- Automatic meter reading (AMR)
- Advanced metering infrastructure (AMI)
- Real-time pricing (RTP)
- Demand response (DR)
- Smart Charging and vehicle-to-grid
- Distribution automation
- Distributed generation integration

1.3 Process Bus Overview

A process bus is a bus or LAN used at the process level, that is, in near proximity to the measured, controlled, or both types of components.

In general, a process bus is used because it does the following:

- Satisfies the need for an interface with an optical voltage and current transformers
- Eliminates copper wiring in the field
- Minimizes configuration time
- Optimizes reconfiguration

The process bus enables the sending of digitized sampled measured values (SMV) from electronic instrument transformers to protect and control relays. The process bus also allows the connection of intelligent switchgear devices such as circuit breakers, disconnectors, or earthing switches. The features of the process bus include the following:

- Fiber-optical (fiber-optic) digital switchyard
- Merging Units (MUs) are digital interfaces to analog signals in the switchyard.
- CTs, VTs, circuit breakers, switchgear, sensors at power transformers, and others
- Ideally located at direct proximity to primary equipment
- Protection relay can be reduced to a CPU with Ethernet card, without any IO modules

The topologies of the process bus include the following:

- Point-to-point, Merging Units with multiple direct connections to IEDs
  - No high accuracy global time reference required, IEDs as synch masters, scalability issues
- Process bus as an Ethernet network is isolated from the station bus
  - Increased security and simplified engineering, required dual homed IEDs
- Process bus shares a common Ethernet network with the station bus
  - This solution is cost effective requires careful network engineering for logical separation.
- Process bus as redundant PRP Stars
  - Zero-time recovery, duplication of network, higher cost of network infrastructure
- Process bus as multiple redundant HSR rings
  - Cost-effective, large network-traffic traversing all nodes, maintenance issues

The performance requirements of the process bus performance include the following:

- Time-accuracy requirements in energy automation applications:
  - 1-s SCADA
  - 100-ms distribution automation
  - 1-ms substation automation (sequence of events)
  - 10-µs process bus
  - 1-µs synchrophasors
- Merging Unit delay bound (primary sensor to Ethernet) according to IEC 61869-9:
  - 1.5 ms for protection
  - 10 ms for metering
- Timing:
  - Currently PPS and IRIG-B are specified in 61850-9-2LE. According to 61850-9-2LE the Merging Unit will have the timestamp accuracy of category T4 which is specified in IEC 61850-5 as ±4 µs

NOTE: Data shifted at the receiving IEDs by just 30 µs results in a half-degree phase-angle error.

1.4 Merging Unit

Merging Units are analog interface units located in the substation yard. Merging Units interface with conventional or non-conventional instrument transformers and send the sampled current and voltage values over fiber, which eliminate the copper wires between the substation primary equipment and the protection as well as control and measuring devices.

As an example, Merging Units are used in substation automation systems for collecting and forwarding sensor data to further devices such as intelligent electronic devices (IEDs) provided for protection, control purposes, or both on a higher level of the respective substation automation system.

A Merging Unit is the interface from the physical analog world to the digital world using communication networks. The analog signal is converted to a digital signal and transmitted through sampled-values (SV) network communication protocol.

The IEC 61850-9-2LE Merging Unit is the optimal solution for process bus interfacing. The Merging Unit allows the consolidation of measurements made in the switchyard by feeding protection relays, meters, and fault recorders located in the control room. The use of fiber-optic communications makes the Merging Unit inherently safe. By eliminating the majority of copper wiring, the Merging Unit addresses key technical and logistic challenges affecting the cost of substation design, construction, and maintenance. The robust and simple architecture of the open IEC 61850-9-2LE process bus allows a mixture of relay, meter, and fault-recording equipment manufacturers. The Merging Unit collects data from conventional instrument transformers and converts the analog signals into a digital protocol defined by IEC 61850-9-2LE. The Merging Unit transmits the converted signal through fiber-optics using industrial-grade Ethernet hardware. Because of the low electrical burden to the instrument transformers, the Merging Unit can be inserted into an operational substation without impacting existing installations. This technology allows the customer to access process bus information at the substation and at higher level control and monitoring facilities.

The sampled values frame as specified in IEC 61850-9-2LE with a sampling rate of 80 samples per cycle has a total size of approximately 180 bytes. At 50 Hz with the sampling rate of 80 samples per cycle, a single Merging Unit sending frames consumes a bandwidth of approximately 6Mb/s. At 60 Hz with a sampling rate of 80 samples per cycle, the sending frame consumes a bandwidth of approximately 7.2 Mb/s. The IEC 61850-9-2LE data set *PhsMeas1* equals a total of eight elements: four currents and four voltages. One Merging Unit can have multiple sets of data.

The sampled value streams for protection and measurement is shown in Table 1:

Table 1. Samples Values Data Stream

PROFILE	POINTS PER CYCLE	SAMPLES PER PACKAGE	TOTAL SAMPLING	PACKAGES PER SECOND
Protection	80	1	4000 to 4800 samples per second	4000 (50 Hz) to 4800 (60 Hz)
Measurement (Power quality monitoring and waveform recording applications)	256	8	12800 to 15360 samples per second	1600 (50Hz) to 1920 (60 Hz)

1.5 Protection Relay

Protective relays detect defective lines, apparatus, or other power system conditions of an abnormal or dangerous nature. Protective relays also initiate appropriate control over circuit action. Relays detect and locate faults by measuring electrical quantities in the power system which are different during normal and intolerable conditions. The most important role of protective relays is to protect individuals and then to protect equipment. Protective relays are also tasked to minimize the damage and expense caused by insulation breakdowns which (above overloads) are called *faults*. These faults can occur as a result of insulation deterioration or unforeseen events such as lightening strikes or power trips caused by contact with trees and foliage.

Relays are not required to operate during normal operation, but must immediately activate to handle intolerable system conditions. This immediate availability criterion is necessary to avoid serious outages and damages to either parts of or the entire power network. In theory, a relay system should be capable of responding to an infinite number of abnormalities that may occur within the network. However, in practice, some compromises must be made by comparing risks. Ensuring stability and security of the entire power system is difficult if only local measurements are employed in monitoring, protection, and control schemes. One way to overcome this difficulty is to develop system-wide protection and control mechanisms that complementary to the conventional local and zonal protection strategies. To implement such mechanisms, synchronized phasor measurements can serve as an effective data source to extract critical information about the condition of the system. Synchronized-phasor measurement capabilities are one of the features available in the most advanced protective relays that are commercially available. The use of this feature is proliferating.

Protection relays are intelligent electronic devices (IEDs) that receive measured signals from the secondary side of CTs and VTs. The relays detect whether or not the protected unit is in a stressed condition (based on the type and configuration of the unit). A trip signal is sent by protective relays to the circuit breakers to disconnect the faulty components from the power system if necessary. Protective relays are categorized based on the equipment type protected such as generators, transmission lines, transformers, and loads.

Typical subsystems of a protection relay include the following:

- Power Supply
  - Wide input range (TI designs available to meet these requirements)
  - 24 to 300-V DC
  - 20 to 265-V AC
  - High-efficiency SMPS
- CPU
  - High-speed 32-Bit RISC CPU
  - > 120 MIPS
  - FLASH memory
  - Easy firmware upgrades
  - High-speed communication support
  - 10/100-Mbps Ethernet LAN
  - Redundant fiber
- DSP and CT or VT
  - Modular CT or VT configurations up to 8 CT or VTs
  - High-speed digital sampling
  - 16-bit AD
  - More than 64 samples per power cycle
  - High-speed DSP
- Digital I/O
  - Control outputs
  - Solid-state

  - Electromechanical, multiple types
  - Fast activation speeds (less than 4 ms)
  - Status inputs
  - Dry and wet contacts
  - 18 to 300-V DC
  - Fast detection speeds (< 4 ms)
- DC analog I/O
  - Transducer type inputs
  - dcmA
  - DC Voltage
  - Resistive
- Communications
  - High-speed serial
  - Asynchronous (9600 to 115 KBaud)
  - Fiber optic (single and multimode)
  - Channel redundancy

The analog-input requirements include the following:

- Current and voltage inputs
  - Secondary of CT, secondary of potential divider
- Low-voltage DC analog input (transducer input)
  - 0 to 20 mA
  - 4 to 20 mA
  - 0 to 5 V
  - 0 to 10 V
  - RTD (Pt, Ni, Cu)
- Number of current and voltage channels for protection relays
  - 4 to 16 channels
- Low-voltage DC analog input (transducer input)
  - 4 to 32 channels

1.6 TI Analog Front End Design With ADS8688

TI has a large portfolio of analog-to-digital converters (ADCs). The ADS8688 device is very well suited for measurement applications in grid infrastructure. This ADC module can measure AC inputs (voltage or current inputs). Sixteen channels are provided on the module and each channel can be configured as a current or voltage input. This TI design also includes an external protection circuit and has been tested and verified to be compliant with IEC61000-4 standards for ESD and Surge requirements.

This TI design demonstrates the following capabilities:

- Using the ADS8688 16-bit ADC to sample current and voltage inputs
- Increasing the number of analog input channels to 16 by daisy-chaining two ADCs
- Sampling of analog inputs at both protection and metering sampling rates as per IEC 61850-9-2LE
- Interfacing through a simple SPI avoids the need for an FPGA (field-programmable gate array)

The design also meets the accuracy and sampling speed requirements for Merging Units, protection relays, multifunction energy meters, and power meters.

See the design tool folder (www.ti.com/tool/TIDA-00307) or Section 8 for the design files to evaluate this design including: schematics, bill of materials (BOM), PCB layout (Altium), and Gerber files.

2 Design Features

Table 2 lists the TIDA-00307 design features.

Table 2. Design Features for TIDA-00307

REQUIREMENTS	SPECIFICATION FEATURES
ADC	16-bit, 8-channel, 500-kHz sampling rate ADS8688
Number of channels	8 channels per ADC (ninth channel without PGA)
Accuracy	< ±0.25%, without calibration at 25°C
Input voltage range	±10.24 V, ±5.12 V, ±2.56 V
Input impedance	> 1 MΩ
Daisy chain	Two ADS8688 devices in daisy-chain configuration
Power supply	5-V analog supply 3.3-V digital I/O supply
Interface	Four-wire SPI-compatible interface
Analog input connectors	Eight 2-pin screw-type terminals for each ADC to connect analog inputs.
ESD immunity	IEC 61000-4-2 : 4-kV contact discharges
Surge transient immunity	IEC 61000-4-5: ±1-kV (CM) on signal ports
Overvoltage protection	±20 V

3 Block Diagram

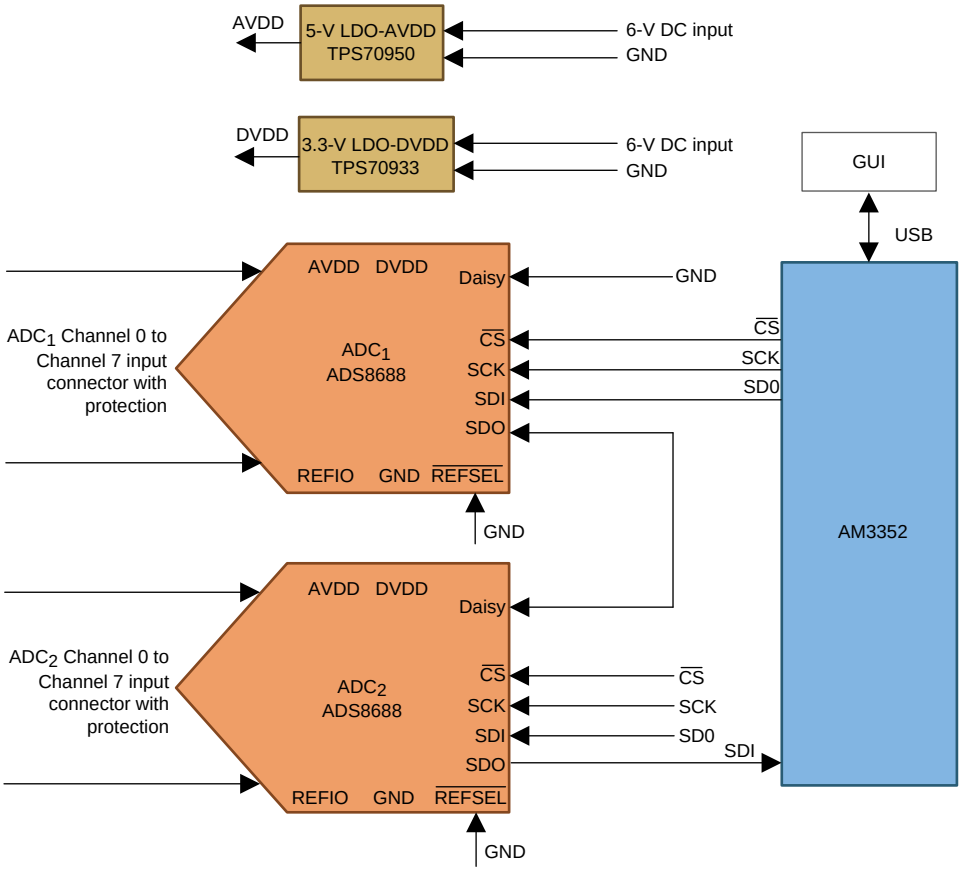


Figure 1. System Block Diagram for TIDA-00307

3.1 ADC

The ADCs used in this design are the ADS8688 device. The ADS8688 device is a 16-bit, 500-kSPS, 8-channel, single-supply, SAR ADC with a bipolar Input. This ADC has an on-chip, 4.096-V reference with low drift. Two ADCs are used in this design which can be configured as either internal or external reference.

3.2 Daisy Chaining

The ADS8688 device features a simple SPI-compatible serial interface with an option to daisy chain multiple ADCs. The two ADCs are daisy chained in this design.

3.3 Power Supply

This design incorporates the TPS70933 device for a 3.3-V power supply and the TPS70950 device for a 5-V power supply. The TPS70933 device is a 150-mA, 30-V, ultra-low I_Q, wide-input low-dropout regulator with reverse current protection. The TPS70950 device is a 150-mA, 30-V, ultra-low I_Q, wide-input low-dropout regulator with reverse current protection.

3.4 Digital Interface

This ADC module is interfaced to the AM3352 ARM Cortex-A8 processor using an SPI-compatible interface.

3.5 Analog Input Connector and Protection

Two pin screw-type connectors (one per channel, total of 16) are provided for connecting the AC analog inputs. The inputs are protected against ESD and Surge. The input applied is single-ended. The following bipolar ranges can be applied: ±2.56 V, ±5.12 V, and ±10.24 V.

3.6 ADC Diagnosis

The AUX_IN ADC channel is configured to be used for diagnosis. The ADC can be sampled during power up or at frequent intervals for diagnosis of the ADC. This channel does not have a PGA at the input.

4 Circuit Design and Component Selection

4.1 ADC

The ADS8688 device is an 8-channel integrated data-acquisition systems-based device on a 16-bit successive approximation (SAR) ADC. The device operates at a throughput of 500 kSPS. The device features integrated analog front-end circuitry for each input channel with overvoltage protection up to ±20 V, an 8-channel multiplexer with automatic and manual scanning modes, and an on-chip 4.096-V reference with extremely low drift. Operating on a single analog supply of 5 V, each input channel on the device can support true bipolar input ranges of ±2.56 V, ±5.12 V and ±10.24 V. The input range selection occurs by programming the software of the internal device registers and is independent for each channel. The device offers a 1-MΩ, constant resistive-input impedance regardless of the selected input range.

The ADS8688 device offers a SPI-compatible serial interface to the digital host and also supports a daisy chain configuration for multiple devices. The digital supply can operate from 1.65 to 5.25 V, enabling direct interface to a wide range of host controllers

The device also offers integrated front-end signal processing including a multiplexer, second-order anti-aliasing filter, ADC driver amplifier, and an extended industrial-temperature range. These features make the ADS8688 device ideal for any standard-industrial analog-input measurements. Figure 2 shows the basic block diagram of the device.

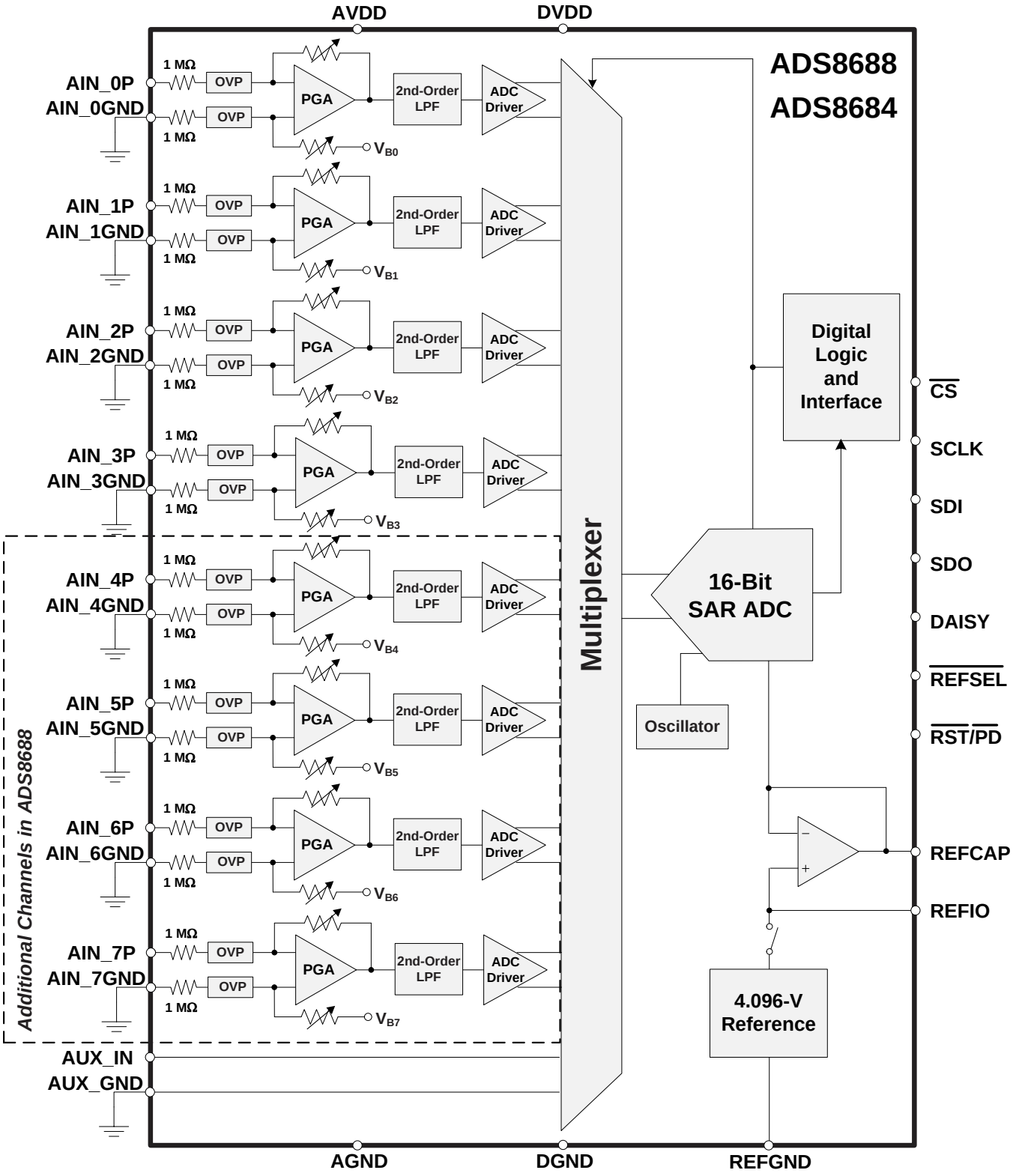


Figure 2. Internal Block Diagram of ADS8688

4.1.1 Second-Order, Low-Pass Filter (LPF)

To mitigate the noise of the front-end amplifiers and gain resistors of the PGA, each analog input channel of the ADS8688 features a second-order, antialiasing LPF at the output of the PGA. Figure 3 and Figure 4 show the magnitude and phase response of the analog antialiasing filter, respectively. For maximum performance, the –3-dB cutoff frequency for the antialiasing filter is typically set to 15 kHz. The performance of the filter is consistent across all input ranges supported by the ADC.

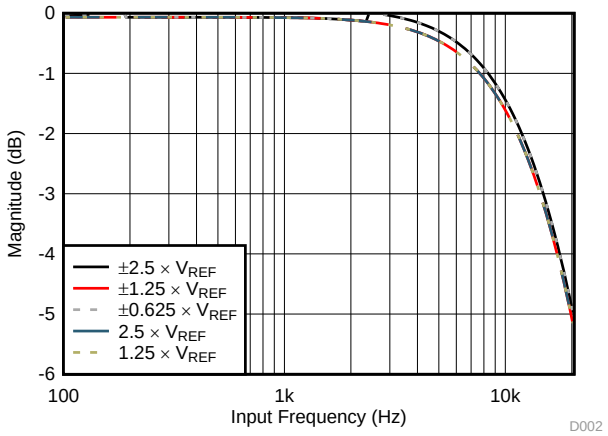


Figure 3. Second-Order LPF Magnitude Response

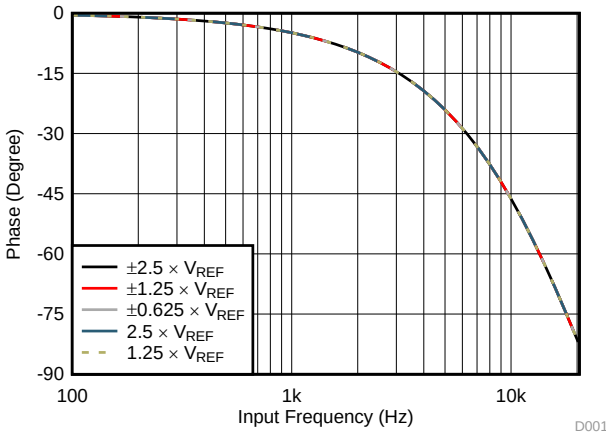


Figure 4. Second-Order LPF Phase Response

ADC filter Performance

4.1.2 ADC Driver

To meet the performance of a 16-bit SAR ADC at the maximum sampling rate (500 kSPS), the sample and hold capacitors at the input of the ADC must be successfully charged and discharged during the acquisition-time window. This drive requirement at the inputs of the ADC requires the use of a high-bandwidth, low-noise, and stable amplifier buffer. Such an input driver is integrated in the front-end signal path of each analog input channel of the device. During transition from one channel of the multiplexer to another channel, the fast integrated driver ensures that the multiplexer output settles to 16-bit accuracy within the acquisition time of the ADC regardless of the input levels on the respective channels.

4.1.3 Multiplexer

The ADS8688 device features an integrated 8-channel analog multiplexer (MUX). For each analog input channel, the voltage difference between the positive analog input, AIN_nP, and the negative ground input, AIN_nGND, is conditioned by the analog front-end circuitry before it is fed into the multiplexer. The output of the multiplexer is directly sampled by the ADC. The multiplexer in the device can scan these analog inputs in either manual or auto-scan mode, as explained in the *Channel Sequencing Modes* section of the ADS8688 datasheet. In manual mode (MAN_Ch_n), the channel is selected for every sample by a register write. In auto-scan mode (AUTO_RST), the channel number automatically increments on every $\overline{CS}$ falling edge after the present channel is sampled. The analog inputs can be selected for an auto scan with register settings. The devices automatically scan only the selected analog inputs in ascending order. The maximum overall throughput for the ADS8688 device is specified at 500 kSPS across all channels. The throughput per channel is dependent on the number of channels selected in the multiplexer scanning sequence. For example, the throughput per channel is equal to 250 kSPS if only two channels are selected but it is equal to 125 kSPS per channel if four channels are selected.

4.1.4 Reference

The ADS8688 device can operate with either an internal voltage reference or an external voltage reference using the internal buffer. The internal or external reference selection is determined by an external REFSEL pin. The devices have a built-in buffer amplifier to drive the actual reference input of the internal ADC core for maximizing performance.

4.1.5 Internal Reference

The devices have an internal 4.096-V (nominal value) reference. To select the internal reference, the REFSEL pin must be tied low or connected to the AGND pin. When the internal reference is used, the REFIO pin (pin 5) becomes an output pin with the internal reference value. TI recommends placing a 10-μF (minimum) decoupling capacitor between the REFIO pin and the REFGND (pin 6) pin, as shown in Figure 5. The capacitor must be placed as close to the REFIO pin as possible. The output impedance of the internal bandgap circuit creates a low-pass filter with this capacitor to band-limit the noise of the reference. The use of a smaller capacitor value allows higher reference noise in the system, thus degrading SNR (signal-to-noise ratio) and SINAD (signal-to-noise and distortion ratio) performance. Do not use the REFIO pin to drive external AC or DC loads because the REFIO pin has limited current output capability. The REFIO pin can be used as a source if followed by a suitable operational amplifier buffer (such as the OPA320 device).

In the current design both ADCs are used as an internal reference. Optionally, when the ADCs are configured in daisy-chain mode, ADC_1 can be configured as an internal reference and ADC_2 can be configured as an external reference. When ADC_1 is configured as an internal reference, the reference output is available on the REFIO pin which can be the reference input for ADC_2. This configuration is required when the accuracy is expected to be same for both ADC_1 and ADC_2 which also reduces power consumption. The internal and external reference is pin configurable ($\overline{REFSEL}$).

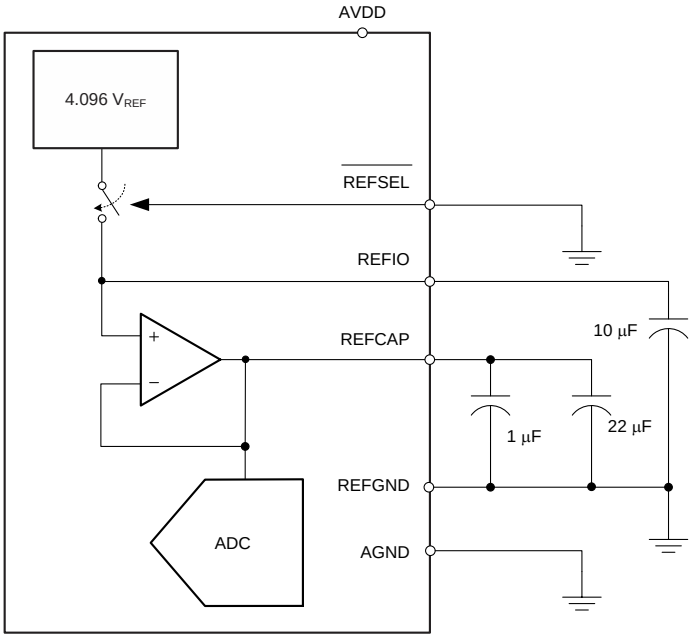


Figure 5. ADS8688 Connections for Using an Internal 4.096-V Reference

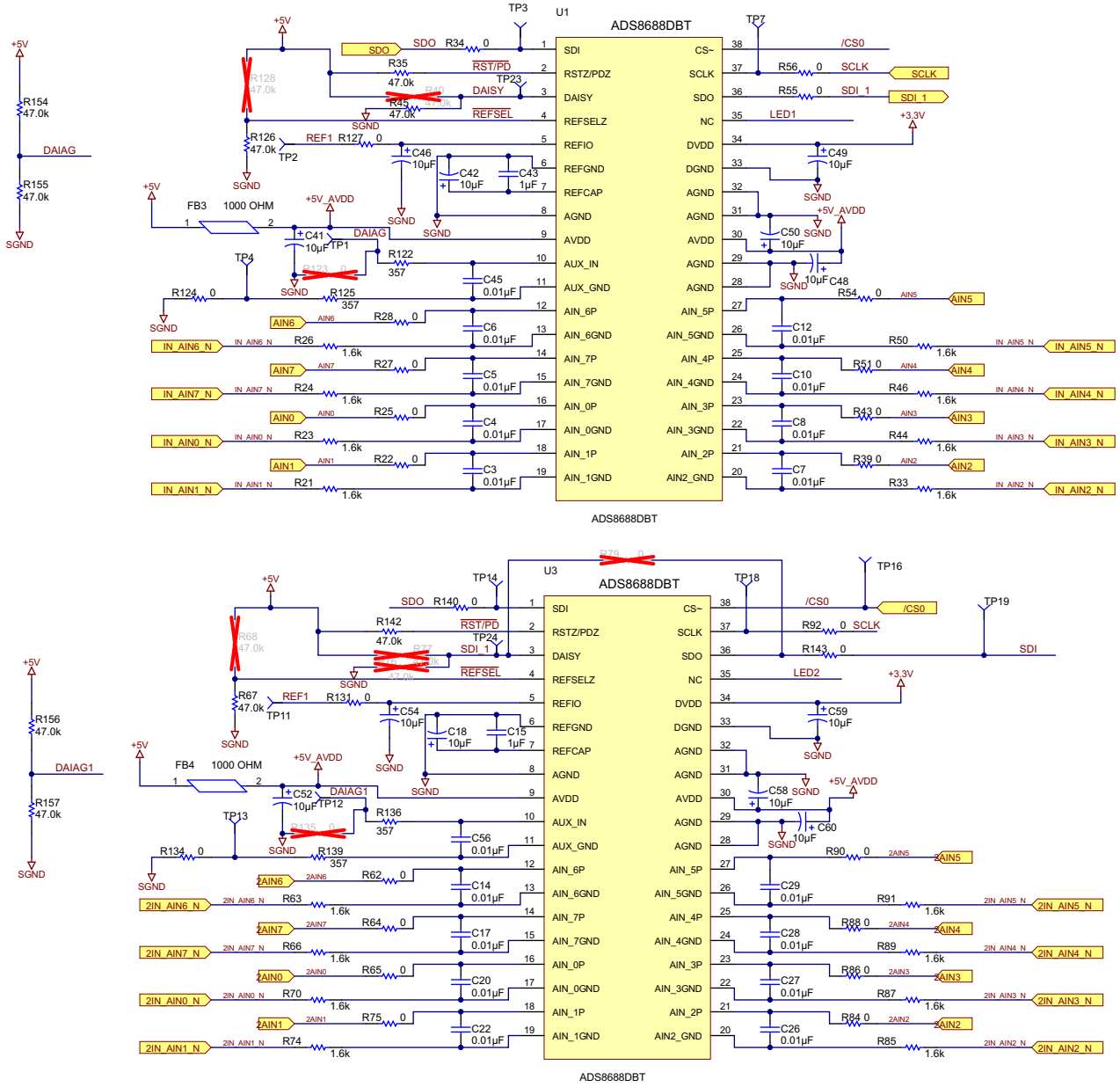


Figure 6. Two ADCs Connected in Daisy Chain Mode

4.2 Daisy Chain Configuration

Figure 7 shows a typical connection diagram with multiple devices in daisy-chain mode. The $\overline{CS}$, SCLK, and SDI inputs of all devices are connected together and controlled by a single $\overline{CS}$, SCLK, and SDO pin of the host controller, respectively. The $DAISY_1$ input pin of the first ADC in the chain is connected to the DGND pin. The SDO1 output pin is connected to the $DAISY_2$ input of ADC_2. The SDON pin of the Nth ADC (ADC_N) in the chain is connected to the SDI pin of the host controller. The devices do not require any special hardware or software configuration to enter daisy-chain mode.

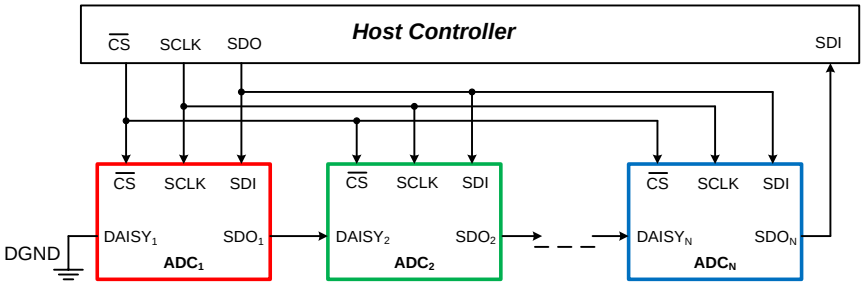


Figure 7. Daisy-Chain Diagram

Figure 7 shows a typical timing diagram for devices connected in daisy-chain mode.

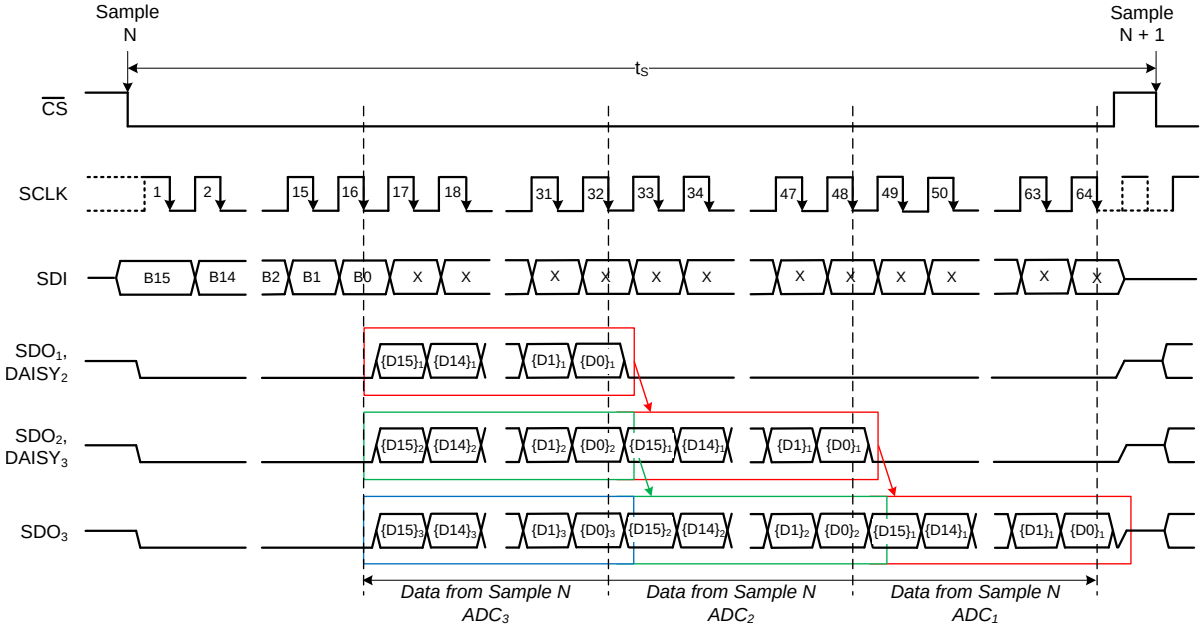


Figure 8. Timing Diagram for Devices Connected in Daisy-Chain Mode

At the falling edge of the $\overline{CS}$ signal, all devices sample the input signal at the respective selected channels and enter into conversion phase. For the first 16 SCLK cycles, the internal register settings for the next conversion can be entered using the SDI line, which is common to all devices in the chain. During this time period, the SDO outputs for all devices remain low. At the end of conversion, every ADC in the chain loads the respective conversion result into an internal 16-bit shift register. At the 16th SCLK falling edge, every ADC in the chain outputs the MSB (most-significant bit) on the respective SDO output pin. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on the $DAISY_N$ pin and shifts out the next bit of data on the SDO pin. Therefore, the digital host receives the data of ADC_N, followed by the data of ADC_{N-1}, and so forth (in MSB-first fashion). In total, a minimum of 16 × N

SCLK falling edges are required to capture the outputs of all N devices in the chain. This example uses three devices in a daisy-chain connection. Therefore, 3 × 16 = 48 SCLK cycles are required to capture the outputs of all devices in the chain along with the 16 SCLK cycles to input the register settings for the next conversion, resulting in a total of 64 SCLK cycles for the entire data frame. The overall throughput of the system is reduced proportionally with the number of devices connected in a daisy-chain configuration.

Referring to Figure 7, the following is true:

- The SDI pins for all devices are connected together so each device operates with the same internal configuration. This limitation can be overcome by spending additional host controller resources to control the SDI input of devices with unique configurations.
- If the number of devices connected in daisy-chain mode is more than four, loading increases on the shared output lines from the host controller ($\overline{CS}$, SDO, and SCLK). This increased loading may lead to digital timing errors. This limitation can be overcome by using digital buffers on the shared outputs from the host controller before feeding the shared digital lines into additional devices.

NOTE: If a daisy configuration is not required and only one device is used, make the following changes:

1. Remove R45 and Mount R40
2. Mount R79
3. Remove U3

NOTE: The current TI design is a non-isolated interface to the host. If an isolated interface is required, this design can be interfaced to the TIDA-00300 design. Care must be taken with respect to the isolator delay influencing the data output rate performance. The TIDA-00300 design is configured for 5 V. The ADC module must also be configured for 5 V.

4.3 Power Supply

4.3.1 3.3-V I/O Power Supply

The TPS70933 regulator is an ultra-low quiescent-current devices designed for power-sensitive applications. A precision bandgap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes this device an ideal solution for battery-powered always-on systems that require very little idle-state power dissipation. This device has thermal-shutdown, current-limit, and reverse-current protections for added safety. The regulator can enter shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA (typical). The TPS70933 device series is available in SON-6, SOT-23-5, and SOT-223-4 packages.

The features of the TPS70933 device include the following:

- Ultra-low I_Q: 1 µA
- Reverse current protection
- Low $I_{SHUTDOWN}$: 150 nA
- Input voltage range: 2.7 to 30 V
- Supports 200-mA peak output
- Low dropout: 245 mV at 50 mA
- 2% accuracy over temperature
- Available in fixed-output voltages: 1.2 to 6.5 V
- Thermal shutdown and overcurrent protection

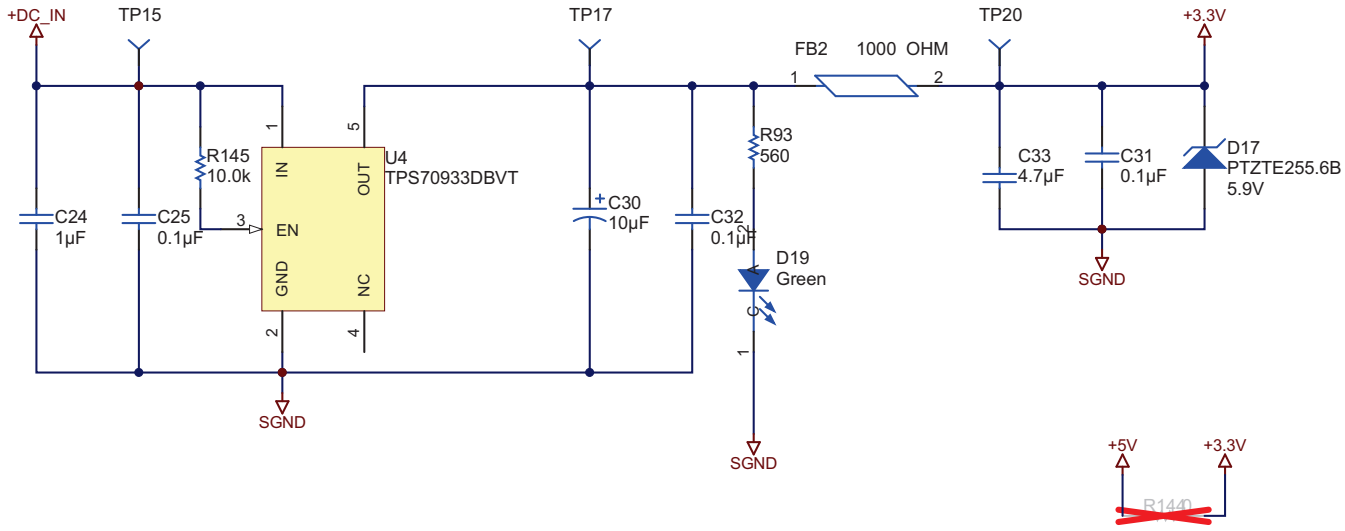


Figure 9. LDO for DVDD (3.3 V)

NOTE: The ADS8688 device can be configured to operate with single supply. Remove the components shown in Figure 9 and populate R144 to configure the ADC for 5-V operation.

4.3.2 5-V Analog Power Supply

The TPS70950 regulator is an ultra-low quiescent-current devices designed for power-sensitive applications. A precision bandgap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes this device an ideal solution for battery-powered always-on systems that require very little idle-state power dissipation. This device has thermal-shutdown, current-limit, and reverse-current protections for added safety. The regulator enters shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA, typical. The TPS70950 device series is available in SON-6, SOT-23-5, and SOT-223-4 packages.

The features of the TPS70950 device include the following

- Ultra-low I_Q: 1 µA
- Reverse current protection
- Low $I_{SHUTDOWN}$: 150 nA
- Input voltage range: 2.7 to 30 V
- Supports 200-mA peak output
- Low dropout: 245 mV at 50 mA
- 2% accuracy over temperature
- Available in fixed-output voltages: 1.2 to 6.5 V
- Thermal shutdown and overcurrent protection

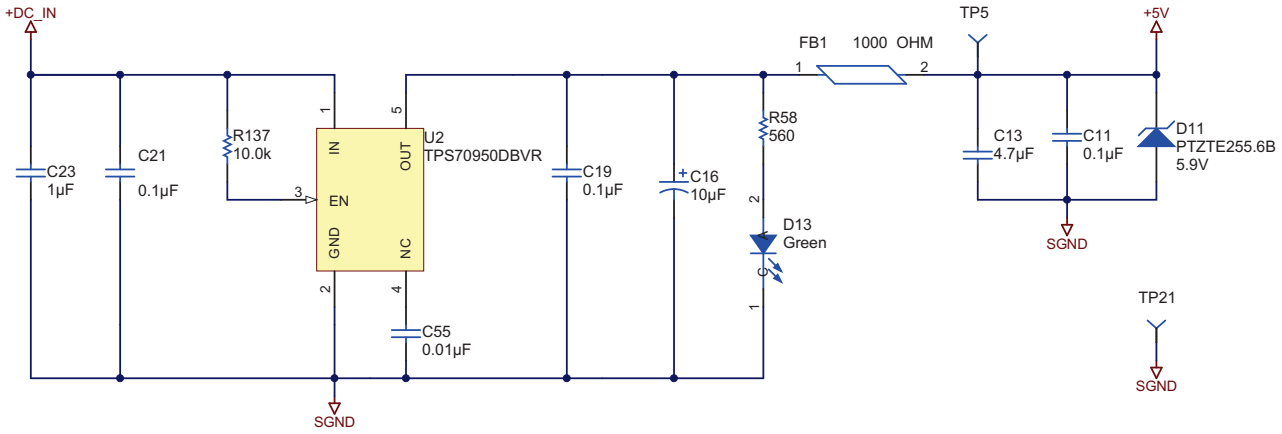


Figure 10. LDO for AVDD (5V)

4.3.3 Power Supply Recommendations

Table 3. Typical Power-Supply Current Requirements

SUPPLY TYPE	ADC_1		ADC_2	
	VOLTAGE (V)	CURRENT (mA)	VOLTAGE (V)	CURRENT (mA)
Analog	5	16	5	16
I/O	3.3	1	3.3	1

The device uses two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on the AVDD supply, while the DVDD supply is used for the digital interface. The AVDD and DVDD supplies can be independently set to any value within the permissible range.

The AVDD supply pins must be decoupled with the AGND pin by using a minimum 10-µF and 1-µF capacitor on each supply. Place the 1-µF capacitor as close to the supply pins as possible. Place a minimum 10-µF decoupling capacitor very close to the DVDD supply to provide the high-frequency digital switching current. The effect of using the decoupling capacitor is shown by the difference in the power-supply rejection ratio (PSRR) performance of the device.

4.4 Digital Interface

4.4.1 Digital Pin Description

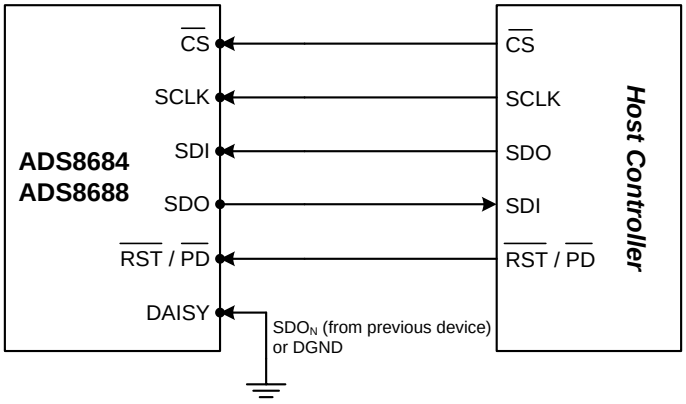


Figure 11. ADS8688 SPI

Figure 11 shows the digital data interface for the ADS8688 device.

The digital pin descriptions are as follows:

$\overline{\text{CS}}$ (Input) — The $\overline{\text{CS}}$ pin is an active-low, chip-select signal. The $\overline{\text{CS}}$ pin is also used as a control signal to trigger a conversion on the falling edge. Each data frame begins with the falling edge of the $\overline{\text{CS}}$ signal. The analog input channel to be converted during a particular frame is selected in the previous frame. On the $\overline{\text{CS}}$ falling edge, the devices sample the input signal from the selected channel and a conversion is initiated using the internal clock. The device settings for the next data frame can be input during this conversion process. When the $\overline{\text{CS}}$ signal is high, the ADC is considered to be in an idle state.

SCLK (Input) — This pin indicates the external clock input for the data interface. All synchronous accesses to the device are timed with respect to the falling edges of the SCLK signal.

SDI (Input) — The SDI pin is the serial data input line. The host processor uses the SDI pin to program the internal device registers for device configuration. At the beginning of each data frame, the $\overline{\text{CS}}$ signal goes low and the data on the SDI line are read by the device at every falling edge of the SCLK signal for the next 16 SCLK cycles. Any changes made to the device configuration in a particular data frame are applied to the device on the subsequent falling edge of the $\overline{\text{CS}}$ signal.

SDO (Output) — The SDO pin is the serial data output line. The device uses the SDO pin to output conversion data. The size of the data output frame varies depending on the register setting for the SDO format. A low level on the $\overline{\text{CS}}$ signal releases the SDO pin from the hi-Z state. The SDO pin is kept low for the first 15 SCLK falling edges. The MSB of the output data stream is clocked out on SDO on the 16th SCLK falling edge, followed by the subsequent data bits on every falling edge thereafter. The SDO line goes low after the entire data frame is output and goes to a hi-Z state when the $\overline{\text{CS}}$ signal goes high.

4.5 Analog Input Connector and Protection

The ADC module contains a terminal block that provides connections for sixteen analog inputs. The inputs can be configured to measure current or voltage inputs. The inputs are protected against ESD and Surge.

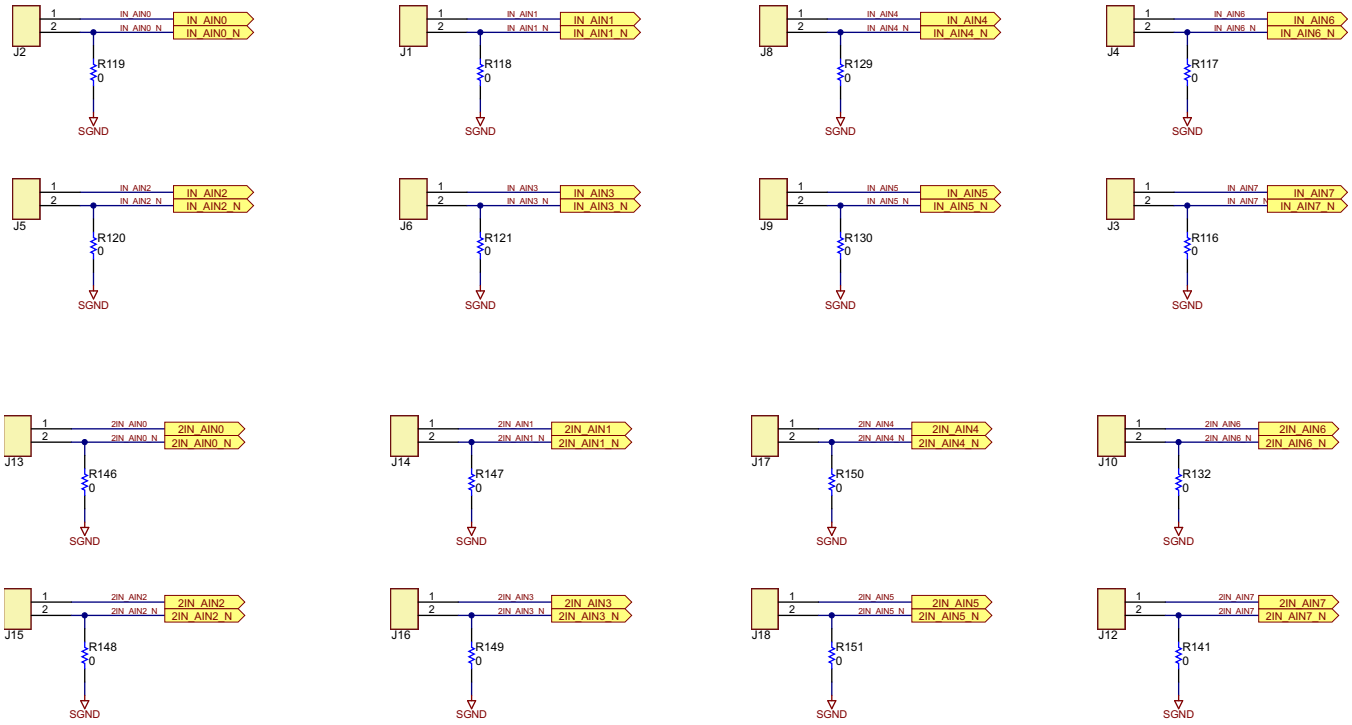


Figure 12. Analog Inputs

Table 4 lists the EMC test requirements.

Table 4. EMC Test Requirements

TEST AND STANDARD	TEST LEVEL
IEC 61000-4-2 Electrostatic Discharge (ESD)	±4-kV contact discharges
IEC 61000-4-5 Surge	±1-kV on signal ports

The transient voltage suppressor (TVS) diodes are used to clamp the surge voltage to safer limits with high-voltage capacitors Y-caps in parallel. In addition, two Y-caps have been placed at key locations to shunt transient energy quickly to earth ground. The Y-caps provides low impedance to fast transients and TVS diodes provides immunity against high voltage spikes.

4.6 ADC Diagnosis

The AUX_IN ADC channel is configured to be used for diagnosis. The 2.5-V DC voltage is connected as input for measurement and diagnosis. This channel does not have the PGA circuit and so the measurement occurs without any gain or configurable range.

4.7 Layout Guidelines

When configuring the ADCs in daisy-chain mode ensure that the traces are matched for the SCLK pin and the chip select for both ADCs connected in daisy-chain configuration.

The following lists the general layout guidelines:

- Partition the PCB into analog and digital sections. Ensure that the analog signals are separated from the digital signals. This layout helps keep the analog input and reference input signals away from the digital noise. In this layout example, the analog input and reference signals are routed on the lower side of the board while the digital connections are routed on the top side of the board.
- Using a dedicated ground plane is encouraged.
- Power sources to the ADS8688 device must be well-bypassed. Placing vias between the AVDD pin, DVDD pin, and the bypass capacitors must be avoided. All ground pins must be connected to the ground plane using short, low-impedance paths.
- Two decoupling capacitors are used for the REFCAP pin. The first capacitor is a small, 1-μF, X7R-grade, 0603-size ceramic capacitor placed close to the device pins for decoupling the high-frequency signals. The second capacitor is has a value of 10-μF which provides the charge required by the reference circuit of the device. Both of these capacitors must be directly connected to the device pins without any vias between the pins and capacitors.
- The REFIO pin also must be decoupled with a 10-μF capacitor if the internal reference of the device is used. The capacitor must be placed close to the device pins.

4.8 Enhancements Based on Application

There are multiple devices that are pin compatible and have the same input ranges. The required ADC can be chosen based on the application and the system cost. Table 5 provides details on different ADCs that can be considered.

Table 5. ADC Selection Based on Applications

SPECIFICATIONS	ADS8698	ADS8688	ADS8688A	ADS8678	ADS8668
Resolution (bits)	18	16	16	14	12
Sample rate (max) (KSPS)	500	500	500	500	500
Number of input channels	8	8	8	8	8
Operating temperature range (°C)	–40 to 125	–40 to 125	–40 to 125	–40 to 125	–40 to 125
Interface	Serial SPI	Serial SPI	Serial SPI	Serial SPI	Serial SPI
Input range (V)	±10.24 ±5.12 ±2.56 10.24 5.12	±10.24 ±5.12 ±2.56 10.24 5.12	±10.24 ±5.12 ±2.56 ±1.28 ±0.64 10.24 5.12 2.56 1.28	±10.24 ±5.12 ±2.56 ±1.28 ±0.64 10.24 5.12 2.56 1.28	±10.24 ±5.12 ±2.56 ±1.28 ±0.64 10.24 5.12 2.56 1.28

5 Software Description

5.1 Configuration for Daisy Chain

When the devices are configured in daisy-chain mode, all of the devices receive the same command input.

5.1.1 Device Features Selection Control Register (address = 03h)

The bits in this register can be used to configure the device ID for daisy-chain operation and configure the output bit format on SDO.

Figure 13. Feature Select Register

7	6	5	4	3	2	1	0
DEV[1:0]		1	0	1	SDO[2:0]		
R/W	R/W	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

Table 6. Feature Select Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	DEV[1:0]	R/W	0h	Device ID bits. 00 = ID for device 0 in daisy-chain mode 01 = ID for device 1 in daisy-chain mode 10 = ID for device 2 in daisy-chain mode 11 = ID for device 3 in daisy-chain mode
5	1	R	1h	Must always be set to 1
4	0	R	0h	Must always be set to 0
3	1	R	1h	Must always be set to 1
2:0	SDO[2:0]	R/W	0h	SDO data format bits (refer to Table 7).

Table 7. Description of Program Register Bits for SDO Data Format

SDO FORMAT SDO[2:0}	BEGINNING OF THE OUTPUT BIT STREAM	OUTPUT FORMAT			
		BITS[24:9]	BITS[8:5]	BITS[4:3]	BITS[2:0]
000	16th SCLK falling edge; no latency	Conversion result for selected channel (MSB-first)	SDO pulled low		
001	16th SCLK falling edge; no latency	Conversion result for selected channel (MSB-first)	Channel address	SDO pulled low	
010	16th SCLK falling edge; no latency	Conversion result for selected channel (MSB-first)	Channel address	Device address	SDO pulled low
011	16th SCLK falling edge; no latency	Conversion result for selected channel (MSB-first)	Channel address	Device address	Input range

Table 8. Data Output Sequence with ADS8688 Daisy Chaining

WORD OUTPUT (ASSUMING ALL EIGHT CHANNELS ARE CONFIGURED)	ADC_1 (DAISY CHAIN INPUT GROUNDED)	ADC2 (SDO FOR ADC_1 CONNECTED TO ADC2 DAISY CHAIN INPUT)
Word 1		CH0
Word 2	CH0	
Word 3		CH1
Word 4	CH1	
Word 5		CH2
Word 6	CH2	
Word 7		CH3
Word 8	CH3	
Word 9		CH4
Word 10	CH4	
Word 11		CH5
Word 12	CH5	
Word 13		CH6
Word 14	CH6	
Word 15		CH7
Word 16	CH7	

5.1.1.1 Achieving Simultaneous Sampling by Daisy-chaining

Simultaneous sampling can be achieved in protection relays by connecting the voltage inputs to ADC_1 and current inputs to ADC_2. Because the sampling for both the ADCs occurs at the same time a high level of simultaneous sampling is achieved. The only error may be because of the phase difference between the two ADC internal oscillator.

Guidelines to achieve simultaneous sampling include the following:

- Ensure minimum delay between the chip select for the two ADCs.
- Ensure the same reference is used which reduces the error and also saves power (connect the ADC_1 reference to the ADC_2 reference and disable the ADC_2 internal reference).

5.2 ADC Input Configuration

Range Select Registers (address = 05h (channel 0), 06h (channel 1), 07h (channel 2), 08h (channel 3), 09h (channel 4), 0Ah (channel 5), 0Bh (channel 6), 0Ch (channel 7))

These registers allow the selection of input ranges for all individual channels (n = 0 to 7 for ADS8688). The default value for these registers is 00h.

Figure 14. Channel *n* Input Range Registers

7	6	5	4	3	2	1	0
0	0	0	0	0	Range_CH*n*[2:0]		
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

Table 9. Channel *n* Input Range Registers Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	0	R	0h	Must always be set to 0
2:0	Range_CH*n*[2:0]	R/W	0h	Input range selection bits for channel n (n = 0 to 3 for ADS8684 and n = 0 to 7 for ADS8688). 000 = Input range is set to ±2.5 x V_{REF} 001 = Input range is set to ±1.25 x V_{REF} 010 = Input range is set to ±0.625 x V_{REF} 101 = Input range is set to 0 to 2.5 x V_{REF} 110 = Input range is set to 0 to 1.25 x V_{REF}

5.2.1 ADC Gain Control — Programmable Gain Amplifier (PGA)

The devices offer a programmable gain amplifier (PGA) at each individual analog input channel, which converts the original single-ended input signal into a fully-differential signal to drive the internal 16-bit ADC. The PGA also adjusts the common-mode level of the input signal before being fed into the ADC to ensure maximum usage of the ADC input dynamic range. Depending on the range of the input signal, the PGA gain can be accordingly adjusted by setting the Range_CHn[2:0] (n = 0 to 3 or 7) bits in the program register. The default or power-on state for the Range_CHn[2:0] bits is 000, which corresponds to an input signal range of ±2.5 × V_{REF}. Table 10 lists the various configurations of the Range_CHn[2:0] bits for the different analog input voltage ranges.

The PGA uses a very highly-matched network of resistors for multiple gain configurations. Matching between these resistors and the amplifiers across all channels is accurately trimmed to keep the overall gain error low across all channels and input ranges.

Table 10. Input Range Selection Bits Configuration

ANALOG INPUT RANGE	Range_CH*n*[2:0]		
	BIT 2	BIT 1	BIT 0
±2.5 × V_{REF}	0	0	0
±1.25 × V_{REF}	0	0	1
±0.625 × V_{REF}	0	1	0
0 to 2.5 × V_{REF}	1	0	1
0 to 1.25 × V_{REF}	1	1	0

5.3 ADC Sampling

5.3.1 Auto-Scan Sequencing Control Registers

In AUTO_RST mode, the device automatically scans the preselected channels in ascending order with a new channel selected for every conversion. Each individual channel can be selectively included in the auto channel sequencing. For the channels that are not selected for auto sequencing, the analog front-end circuitry can be individually powered down.

5.3.2 Manual Channel Selection Including Aux Channel — Command Register Description

The command register is a 16-bit, write-only register that is used to set the operating modes of ADS8688. The settings in this register are used to select the channel sequencing mode (AUTO_RST or MAN_Ch_n), configure the device in standby (STDBY) or power-down (PWR_DN) mode, and reset (RST) the program registers to their default values. All command settings for this register are listed in Table 11. During power-up or reset, the default content of the command register is all 0s and the device waits for a command to be written before being placed into any mode of operation The device executes the command at the end of this particular data frame when the $\overline{CS}$ signal goes high.

Table 11. Command Register Map

REGISTER	MSB BYTE								LSB BYTE	COMMAND (Hex)	OPERATION IN NEXT FRAME
	B15	B14	B13	B12	B11	B10	B9	B8	B[7:0]		
Continued Operation (NO_OP)	0	0	0	0	0	0	0	0	0000 0000	0000h	Continue operation in previous mode
Standby (STDBY)	1	0	0	0	0	0	1	0	0000 0000	8200h	Device is placed into standby mode
Power Down (PWR_DN)	1	0	0	0	0	0	1	1	0000 0000	8300h	Device is powered down
Reset program registers (RST)	1	0	0	0	0	1	0	1	0000 0000	8500h	Program register is reset to default
Auto Ch. Sequence with Reset (AUTO_RST)	1	0	1	0	0	0	0	0	0000 0000	A000h	Auto mode enabled following a reset
Manual Ch 0 Selection (MAN_Ch_0)	1	1	0	0	0	0	0	0	0000 0000	C000h	Channel 0 input is selected
Manual Ch 1 Selection (MAN_Ch_1)	1	1	0	0	0	1	0	0	0000 0000	C400h	Channel 1 input is selected
Manual Ch 2 Selection (MAN_Ch_2)	1	1	0	0	1	0	0	0	0000 0000	C800h	Channel 2 input is selected
Manual Ch 3 Selection (MAN_Ch_3)	1	1	0	0	1	1	0	0	0000 0000	CC00h	Channel 3 input is selected
Manual Ch 4 Selection (MAN_Ch_4)[1]	1	1	0	1	0	0	0	0	0000 0000	D000h	Channel 4 input is selected
Manual Ch 5 Selection (MAN_Ch_5)	1	1	0	1	0	1	0	0	0000 0000	D400h	Channel 5 input is selected
Manual Ch 6 Selection (MAN_Ch_6)	1	1	0	1	1	0	0	0	0000 0000	D800h	Channel 6 input is selected
Manual Ch 7 Selection (MAN_Ch_7)	1	1	0	1	1	1	0	0	0000 0000	DC00h	Channel 7 input is selected
Manual AUX Selection (MAN_AUX)	1	1	1	0	0	0	0	0	0000 0000	E000h	AUX channel input is selected

(1) Shading indicates bits, registers, or both not included in the 4-channel version of the device.

5.3.3 Auto-Scan Sequence Enable Register (address = 01h)

This register selects individual channels for sequencing in AUTO_RST mode. The default value for this register is FFh, which implies that in default condition all channels are included in the auto-scan sequence.

Figure 15. AUTO_SEQ_EN Register

7	6	5	4	3	2	1	0
CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 12. AUTO_SEQ_EN Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CH7_EN	R/W	1h	Channel 7 enable. 0 = Channel 7 is not selected for sequencing in AUTO_RST mode 1 = Channel 7 is selected for sequencing in AUTO_RST mode
6	CH6_EN	R/W	1h	Channel 6 enable. 0 = Channel 6 is not selected for sequencing in AUTO_RST mode 1 = Channel 6 is selected for sequencing in AUTO_RST mode
5	CH5_EN	R/W	1h	Channel 5 enable. 0 = Channel 5 is not selected for sequencing in AUTO_RST mode 1 = Channel 5 is selected for sequencing in AUTO_RST mode
4	CH4_EN	R/W	1h	Channel 4 enable. 0 = Channel 4 is not selected for sequencing in AUTO_RST mode 1 = Channel 4 is selected for sequencing in AUTO_RST mode
3	CH3_EN	R/W	1h	Channel 3 enable. 0 = Channel 3 is not selected for sequencing in AUTO_RST mode 1 = Channel 3 is selected for sequencing in AUTO_RST mode
2	CH2_EN	R/W	1h	Channel 2 enable. 0 = Channel 2 is not selected for sequencing in AUTO_RST mode 1 = Channel 2 is selected for sequencing in AUTO_RST mode
1	CH1_EN	R/W	1h	Channel 1 enable. 0 = Channel 1 is not selected for sequencing in AUTO_RST mode 1 = Channel 1 is selected for sequencing in AUTO_RST mode
0	CH0_EN	R/W	1h	Channel 0 enable. 0 = Channel 0 is not selected for sequencing in AUTO_RST mode 1 = Channel 0 is selected for sequencing in AUTO_RST mode

5.4 SPI for ADC Data Acquisition

5.4.1 Data Acquisition Example

This section provides an example of how a host processor can use the device interface to configure the device internal registers as well as convert and acquire data for sampling a particular input channel. Figure 16 shows the timing diagram.

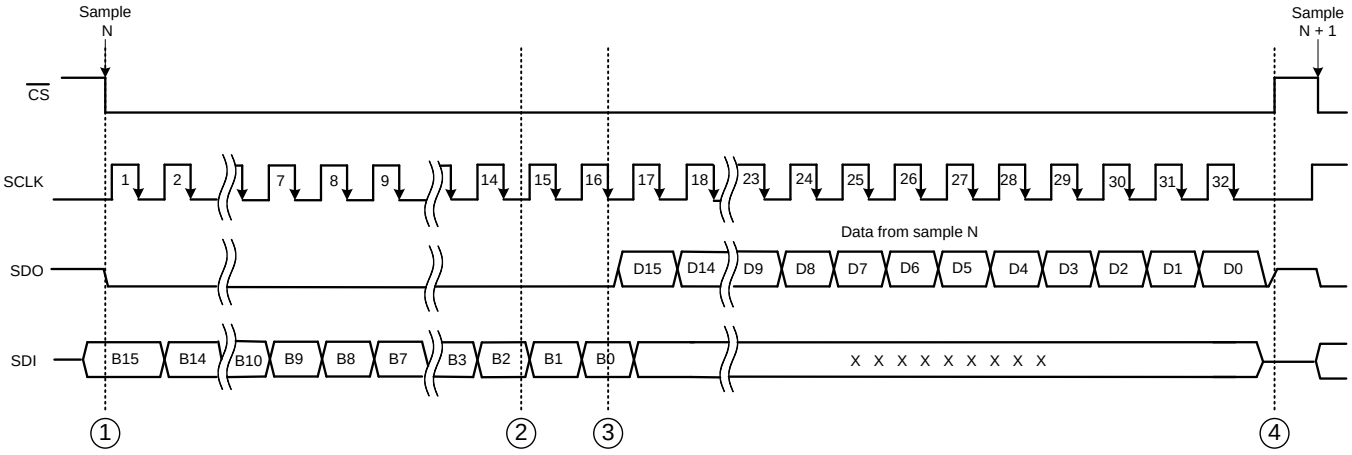


Figure 16. Device Operation Using the Serial Interface Timing Diagram

Four events are shown in Figure 16. These events are described as follows:

Event 1 — The host initiates a data conversion frame through a falling edge of the $\overline{CS}$ signal. The analog input signal at the instant of the $\overline{CS}$ falling edge is sampled by the ADC and conversion is performed using an internal oscillator clock. The analog input channel converted during this frame is selected in the previous data frame. The internal register settings of the device for the next conversion can be input during this data frame using the SDI and SCLK inputs. Initiate SCLK at this instant and latch data on the SDI line into the device on every SCLK falling edge for the next 16 SCLK cycles. At this instant, SDO goes low because the device does not output internal conversion data on the SDO line during the first 16 SCLK cycles.

Event 2 — During the first 16 SCLK cycles, the device completes the internal conversion process and data are now ready within the converter. However, the device does not output data bits on SDO until the 16th falling edge appears on the SCLK input. Because the ADC conversion time is fixed (the maximum value is given in the *Electrical Characteristics* table of the data sheet), the 16th SCLK falling edge must appear after the internal conversion is over, otherwise data output from the device is incorrect. Therefore, the SCLK frequency cannot exceed a maximum value, as provided in the Timing Requirements: Serial Interface table of the data sheet.

Event 3 — At the 16th falling edge of the SCLK signal, the device reads the LSB of the input word on the SDI line. The device does not read anything from the SDO line for the remaining data frame. On the same edge, the MSB of the conversion data is output on the SDO line and can be read by the host processor on the subsequent falling edge of the SCLK signal. For 16 bits of output data, the LSB can be read on the 3-s SCLK falling edge. The SDO outputs 0 on subsequent SCLK falling edges until the next conversion is initiated.

Event 4 — When the internal data from the device is received, the host terminates the data frame by deactivating the $\overline{CS}$ signal to high. The SDO output goes into a hi-Z state until the next data frame is initiated, as explained in Event 1.

5.5 ADC Transfer Function, Range Selection, and RMS Calculation

5.5.1 ADC Transfer Function

The ADS8688 device is a multichannel device that supports single-ended, bipolar, and unipolar input ranges on all input channels. The output of the device is in straight binary format for both bipolar and unipolar input ranges. The format for the output codes is the same across all analog channels. Figure 17 shows the ideal transfer characteristic for each ADC channel for all input ranges. The full-scale range (FSR) for each input signal is equal to the difference between the positive full-scale (PFS) input voltage and the negative full-scale (NFS) input voltage. The least-significant bit (LSB) size is equal to FSR / 216 = FSR / 65536 because the resolution of the ADC is 16 bits. For a reference voltage of V_{REF} = 4.096 V, the LSB values corresponding to the different input ranges are listed in Table 13.

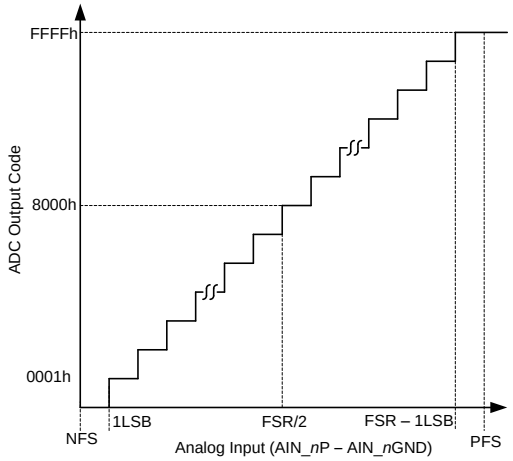


Figure 17. 16-Bit ADC Transfer Function (Straight Binary Format)

Table 13. ADC LSB Values for Different Input Ranges (V_{REF} = 4.096 V)

INPUT RANGE	POSITIVE FULL SCALE	NEGATIVE FULL SCALE	FULL-SCALE RANGE	LSB (µV)
±2.5 × V_{REF}	10.24 V	–10.24 V	20.48 V	312.5
±1.25 × V_{REF}	5.12 V	–5.12 V	10.24 V	156.25
±0.625 × V_{REF}	2.56 V	–2.56 V	5.12 V	78.125
0 to 2.5 × V_{REF}	10.24 V	0 V	10.24 V	156.25
0 to 1.25 × V_{REF}	5.12 V	0 V	5.12 V	78.125

5.5.2 Range Select Registers (address = 05h (Channel 0), 06h (Channel 1), 07h (Channel 2), 08h (Channel 3), 09h (Channel 4, 0Ah (Channel 5), 0Bh (Channel 6), 0Ch (Channel 7)

These registers allow the selection of input ranges for all individual channels (n = 0 to 3 for ADS8684 and n = 0 to 7 for ADS8688). The default value for these registers is 00h.

Figure 18. Channel *n* Input Range Registers

7	6	5	4	3	2	1	0
0	0	0	0	o	Range_CH*n*[2:0]		
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

Table 14. Channel *n* Input Range Registers Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	0	R	0h	Must always be set to 0.
2:0	Range_CH*n*[2:0]	R/W	0h	Input range selection bits for channel n (n = 0 to 3 for ADS8684 and n= 0 to 7 for ADS8688). 000 = Input range is set to ±2.5 × V_{REF} 001 = Input range is set to ±1.25 × V_{REF} 010 = Input range is set to ±0.625 × V_{REF} 101 = Input range is set to 0 to 2.5 × V_{REF} 110 = Input range is set to 0 to 1.25 × V_{REF}

5.5.3 RMS Calculation Procedure

Use the following steps to calculate the RMS (root-mean-squar) value:

Step 1. Configure the ADC for bipolar input.
Step 2. Set the required voltage input (variable) and frequency (50 or 60 Hz).
Step 3. Sample the input at 500 kSPS or the required sample rate.
Step 4. Subtract FSR / 2 (offset) from all of the samples (the ADC is unipolar).
Step 5. Square all of the samples and accumulate.
Step 6. Count the number of samples accumulated.
Step 7. Divide the accumulated samples by the number of samples accumulated.
Step 8. Calculate the square root of the accumulated samples.
Step 9. Scale the code with the configured input range (for example: 10.24 V = Full range).

6 Test Setup

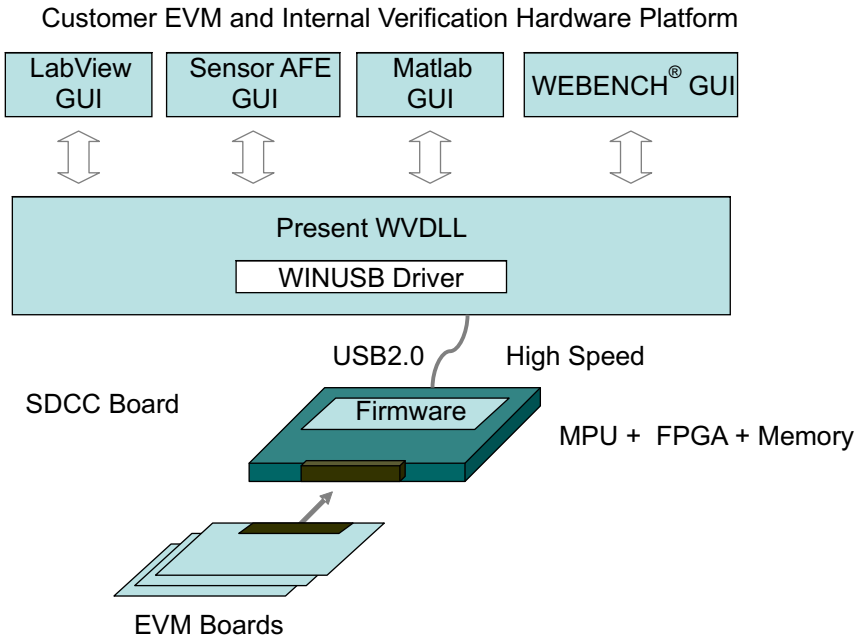


Figure 19. GUI to Capture ADC Data

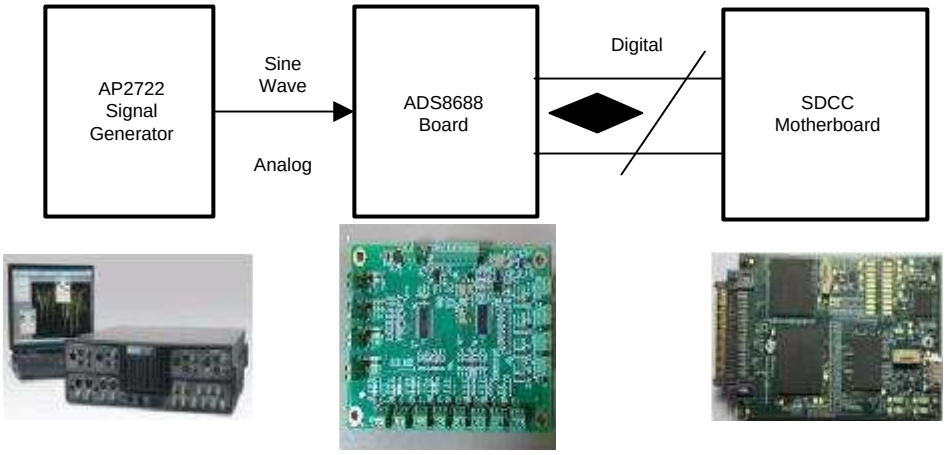


Figure 20. ADC Measurement Setup

The LabVIEW-based GUI is used to interface to the SDCC motherboard. The SDCC motherboard interfaces with the ADS8688 board through SPI interface.

7 Test Results

7.1 Functional Testing

Table 15. DC Voltage Measurements

PARAMETERS		MEASURED VALUES
Analog power supply	AVDD + 5-V DC	4.995 to 4.996
I/O power supply	DVDD + 3.3 DC	3.299 to 3.301
ADC reference	REFIO 4.096	4.097 to 4.098

7.2 ADC Functionality

7.2.1 Functional Testing with Daisy Chain

All of the 8 input channels for ADC_1 and ADC_2 sense the applied input voltage and provide the equivalent ADC codes. No accuracy was tested as part of this test.

7.2.2 Settings Made for Interfacing with ADC

Table 16. ADC Interface Settings

PARAMETERS	SETTINGS
Clock	The clock programmed was 17 MHz
Frame size	The frame size was 48 Bits (16 command + CH1 (16 bits) + Ch2 (16 Bites))
Delay between samples	>2 clocks
Analog input applied to Channel 0 and Channel 4	5-V DC, 3.5-V_{RMS} AC

7.2.3 Observations

Table 17. ADC Input Sensing

ADC CHANNELS	AC INPUT SENSING		DC INPUT SENSING	
	ADC_1	ADC_2	ADC_1	ADC_2
Channel 0	OK	OK	OK	OK
Channel 1	OK	OK	OK	OK
Channel 2	OK	OK	OK	OK
Channel 3	OK	OK	OK	OK
Channel 4	OK	OK	OK	OK
Channel 5	OK	OK	OK	OK
Channel 6	OK	OK	OK	OK
Channel 7	OK	OK	OK	OK

7.3 Analog Input Voltage Measurement

7.3.1 Procedure

- Applied an AC voltage as listed in Section 7.4 and Section 7.6 with a frequency of 60 Hz
- Captured samples using LabVIEW-based GUI
- The AM3352 processor interfaced with the ADS8688 device using SPI
- Greater than 10K ADC samples were captured
- RMS was computed for the captured samples
- All errors were measured are without any software calibration

Table 18. Input Connectors for ADC_1 and ADC_2

CHANNELS	ADC_1 CONNECTOR	ADC_2 CONNECTOR
Channel 0	J2	J13
Channel 1	J1	J14
Channel 2	J5	J15
Channel 3	J6	J16
Channel 4	J8	J17
Channel 5	J9	J18
Channel 6	J3	J10
Channel 7	J3	J12

7.4 Observations

Table 19. ADC Measurement With 3.5-V_{RMS} Input(1)

ADC CHANNELS	ADC_1 (FIRST IN THE DAISY CHAIN WITH THE DAISY-CHAIN INPUT PIN GROUNDED)		ADC_2 (LAST IN THE DAISY CHAIN)	
	APPLIED INPUT (V)	MEASURED (V)	APPLIED INPUT (V)	MEASURED (V)
Channel 0	3.553	3.5512	3.553	3.552
Channel 1	3.551	3.55	3.551	3.5501
Channel 2	3.5532	3.5512	3.5532	3.552
Channel 3	3.5518	3.55	3.5518	3.5501
Channel 4	3.557	3.555	3.557	3.5558
Channel 5	3.5532	3.5512	3.5532	3.552
Channel 6	3.5518	3.55	3.5518	3.5501
Channel 7	3.557	3.555	3.557	3.5558

(1) Measurement uncertainty is 1 to 2 mV.

Table 20. ADC Measurement With 500-mV_{RMS} Input(1)

ADC CHANNELS	ADC_1 (FIRST IN THE DAISY CHAIN WITH THE DAISY-CHAIN INPUT PIN GROUNDED)		ADC_2 (LAST IN THE DAISY CHAIN)	
	APPLIED INPUT (mV)	MEASURED	APPLIED INPUT (mV)	MEASURED
Channel 0	500.1	500.05	500.1	500.05
Channel 1	500.2	500.1	500.2	500.1
Channel 2	500.4	500.03	500.4	500.04
Channel 3	500.2	500.13	500.2	500.13
Channel 4	500.4	500.22	500.4	500.28
Channel 5	500.2	500.14	500.2	500.19
Channel 6	500.4	500.21	500.4	500.27
Channel 7	500.2	500.12	500.2	500.16

(1) Measurement uncertainty is 0.1 to 0.3 mV.

7.5 Simultaneous Sampling Verification (Peak-Samples Comparison Method)

When two devices are connected in daisy chain and the same chip select is asserted for sampling, sampling delay will be minimal between the CH0 of ADC_1 and CH0 of ADC_2.

7.5.1 Simultaneous Sampling Verification Steps

Step 1. Configure ADC_1 and ADC_2 to capture Channel 0.

Step 2. Apply 60-Hz AC input.

Step 3. Assert the chip select to initiate the conversion at maximum frequency.

Step 4. Because two channels are selected, the frame size is 48 bits and the throughput for each channel will be ≤ 250 kHz (Can be less if we have one or two clock delay between conversions).

Step 5. Capture samples for > 100 ms.

Step 6. Compare the minimum ADC sample and maximum ADC sample number for the two ADC outputs.

7.6 Accuracy Result for Simultaneously Sampled Channels in Daisy-Chain Mode

All the errors measured are without any software calibration for gain adjustment.

Table 21. ADC Accuracy for Channel 0(1)

SL NO	50-Hz ,10.24-V INPUT RANGE ACCURACY					60-Hz,10.24-V INPUT RANGE ACCURACY				
		ADC_1		ADC_2			ADC_1		ADC_2	
	ACTUAL	MEASURED	ERROR (%)	MEASURED	ERROR (%)	ACTUAL	MEASURED	ERROR (%)	MEASURED	ERROR (%)
1	0.5003	0.5068	0.0999	0.5069	0.1199	0.5005	0.5055	0.0000	0.5058	0.0599
2	1.0001	1.0067	0.0600	1.0067	0.0600	0.9995	1.0050	0.0480	1.0050	0.0480
3	1.9998	2.0048	–0.0500	2.0047	–0.0550	2.0010	2.0068	0.0400	2.0068	0.0400
4	2.9998	3.0041	–0.0567	3.0036	–0.0733	3.0010	3.0061	0.0030	3.0061	0.0030
5	4.0010	4.0037	–0.0825	4.0033	–0.0925	4.0002	4.0035	–0.0425	4.0031	–0.0525
6	4.9994	4.9932	–0.2440	4.9927	–0.2540	4.9995	4.9943	–0.2040	4.9937	–0.2160
7	6.0010	5.9940	–0.2166	5.9930	–0.2333	5.9998	5.9931	–0.1950	5.9930	–0.1967
8	6.9950	6.9864	–0.2087	6.9857	–0.2187	6.9986	6.9904	–0.1886	6.9895	–0.2015

(1) These measurements are without software offset or gain calibration.

Table 22. ADC Accuracy for Channel 4(1)

SL NO	50-Hz ,10.24-V INPUT RANGE ACCURACY					60-Hz,10.24-V Input Range Accuracy				
		ADC_1		ADC_2			ADC_1		ADC_2	
	ACTUAL	MEASURED	ERROR (%)	MEASURED	ERROR (%)	ACTUAL	MEASURED	ERROR (%)	MEASURED	ERROR (%)
1	0.4989	0.5058	0.1804	0.5059	0.2004	0.4994	0.5046	0.0400	0.5051	0.1402
2	0.9960	1.0027	0.0703	1.0034	0.1406	0.9995	1.0052	0.0700	1.0056	0.1101
3	2.0018	2.0075	–0.0150	2.0079	0.0050	1.9985	2.0044	0.0450	2.0046	0.0550
4	2.9998	3.0034	–0.0800	3.0041	–0.0567	2.9992	3.0036	–0.0200	3.0034	–0.0267
5	3.9932	3.9969	–0.0576	3.9971	–0.0526	3.9983	4.0015	–0.0450	4.0022	–0.0275
6	4.9980	4.9935	–0.2101	4.9939	–0.2021	5.0016	4.9963	–0.2059	4.9970	–0.1919
7	6.0054	5.9988	–0.2098	5.9991	–0.2048	5.9985	5.9916	–0.1979	5.9925	–0.1834
8	7.0001	6.9915	–0.2086	6.9919	–0.2029	7.0005	6.9926	–0.1843	6.9895	–0.2286

(1) These measurements are without software offset or gain calibration.

For testing the accuracy performance of the ADS8688 device, the voltage input was applied. Provision for Burden resistors are included to apply the AC current input.

7.7 Diagnosis Channel Testing

The AUX_IN ADC channel has no front end PGA and the input is limited as follows:

Table 23. AUX_IN Channel Input Range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(AUX\_IN)}$	AUX_IN voltage range	(AUX_IN – AUX_GND)	0		V_{REF}	V
	Operating input range	AUX_IN	0		V_{REF}	V
		AUX_GND		0		V

Table 24. AUX_IN Channel Measurement With 0-V DC Input

ADC	OBSERVATION WITH 0-V INPUT
ADC_1	0
ADC_2	0

Table 25. AUX_IN Channel Measurement With 5-V / 2 DC Input

ADC	OBSERVATION WITH 2.5-V (5 V / 2) INPUT
ADC_1	2.501
ADC_2	2.502

7.8 Overvoltage Protection Testing

Table 26. Overvoltage Protection

APPLIED CHANNEL	ADC READING FOR 7 V_{RMS} BEFORE APPLYING 20-V OVERVOLTAGE	ADC READING FOR 7 V_{RMS} BEFORE APPLYING 20-V OVERVOLTAGE
ADC_1 – Channel 1	6.998	6.998
ADC_2 – Channel 1	6.997	6.997

NOTE: The output voltage saturates after a 10.24-V peak input.

To simulate an overvoltage protection condition, a 20-V peak AC input was applied for >5 s.

7.9 Accuracy Performance of ADS8688

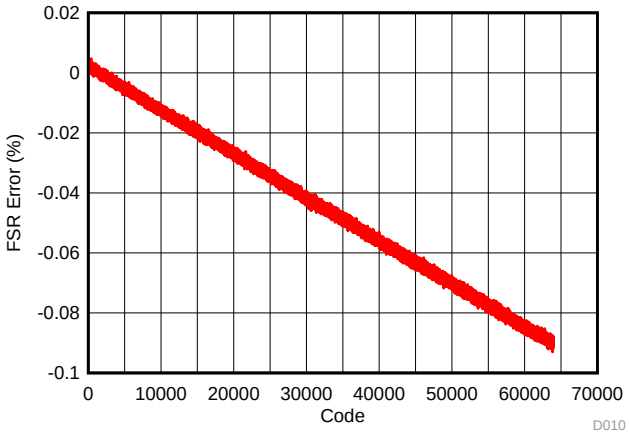


Figure 21. 0 to 5-V Range, Code versus FSR Error (%) Before Calibration

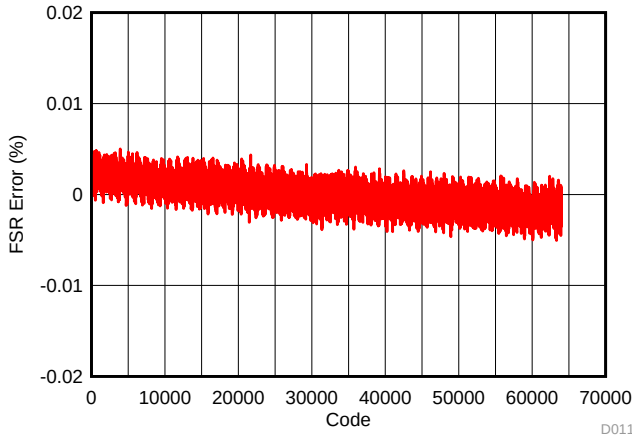


Figure 22. 0 to 5-V Range, Code versus FSR Error (%) After Calibration

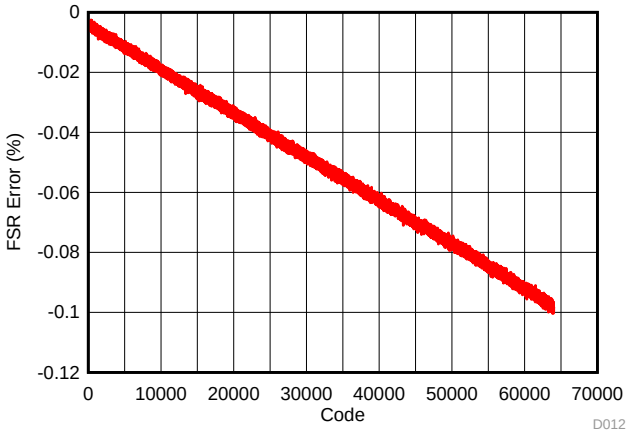


Figure 23. 0 to 10-V Range, Code versus FSR Error (%) Before Calibration

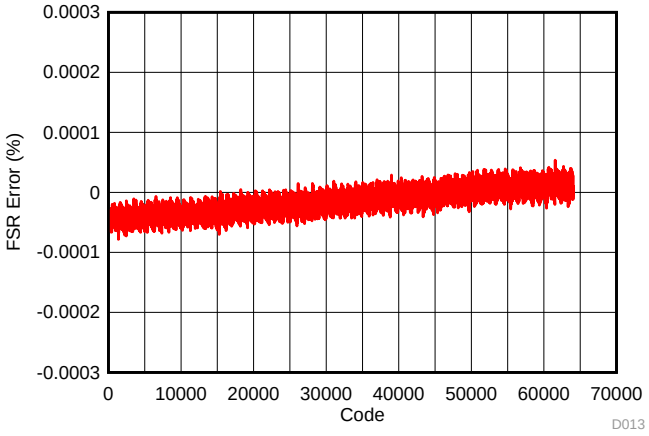


Figure 24. 0 to 10-V Range, Code versus FSR Error (%) After Calibration

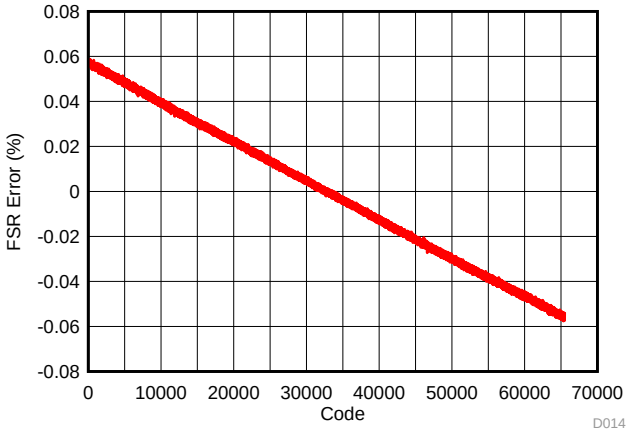


Figure 25. ±10-V Range, Code versus FSR Error (%) Before Calibration

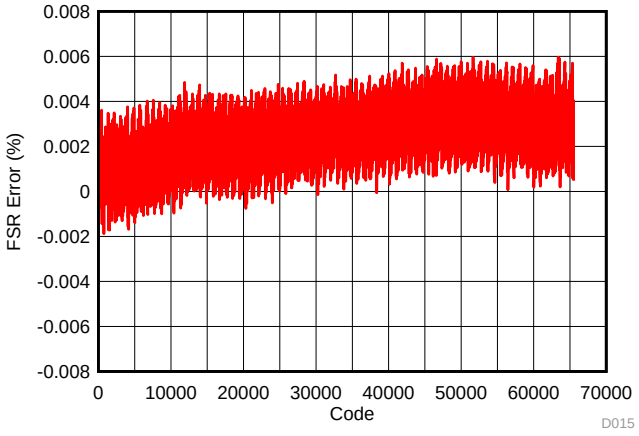


Figure 26. ±10-V Range, Code versus FSR Error (%) After Calibration

7.10 Pre-Compliance Testing

The following EMC Standard tests have been performed.

- Electrostatic Discharge (ESD), IEC61000-4-2
- Surge, IEC61000-4-5

Table 27. Performance Criteria

CRITERIA	PERFORMANCE (PASS) CRITERIA
A	The ADC module continues to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test ADC module continues to operate as intended without manual intervention.
C	During the test loss of functions accepted, but no destruction of hardware or software. After the test ADC module shall continue to operate as intended automatically, after manual restart, power off, or power on.

The following sections explain the test setup, procedures, and observations.

7.10.1 Electrostatic Discharge (ESD): IEC61000 -4-2

The ESD level at the analog input connectors and the performance criteria expected are as follows:

Table 28. ESD Test Conditions

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE
ESDIEC 61000-4-2	4-kV contact discharges applied on signal lines	Criteria B (After the test, ADC module continued to operate as intended)

Table 29. ESD Test Result

TEST NUMBER	TEST MODE	OBSERVATION
1	Contact 1 kV	Pass
2	Contact –1 kV	Pass
3	Contact 2 kV	Pass
4	Contact –2 kV	Pass
5	Contact 4 kV	Pass
6	Contact –4 kV	Pass

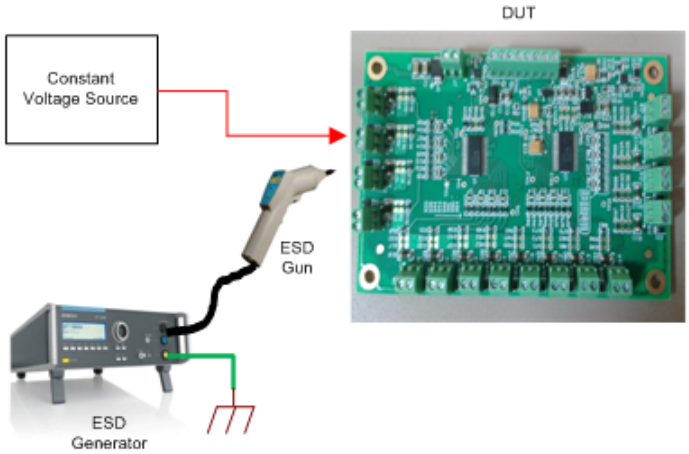


Figure 27. ESD Setup

7.10.2 SURGE- IEC61000 -4-5

7.10.2.1 Test Level and Expected Performance

The common-mode Surge at the I/O connectors and the performance criteria expected are as follows:

Table 30. Surge Test Conditions

GENERIC TEST STANDARD	TEST LEVEL	PERFORMANCE
Surge IEC 61000-4-5	±1 kV, signal lines	Criteria B (After the test ADC module continued to operate as intended)

Table 31. Surge Test Results

TEST NUMBER	TEST MODE	OBSERVATION
1	0.5 kV	Pass
2	–0.5 kV	Pass
3	1 kV	Pass
4	–1 kV	Pass

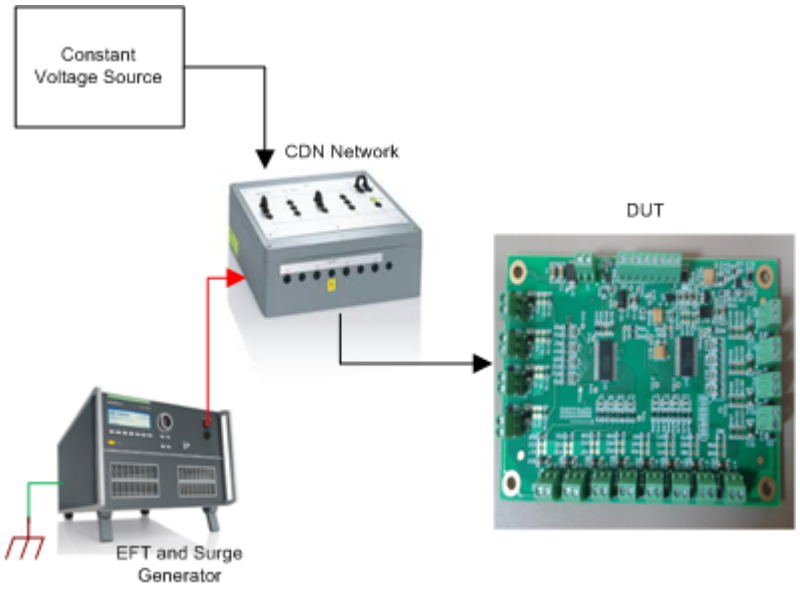


Figure 28. Surge Test Setup

7.11 Summary

Table 32. Summary of Test Results

TEST	RESULT
Daisy chaining	Daisy chaining works with two ADCs. Samples captured at 500 kHz
Sampling of all channels	Both ADCs sensed the applied analog input on all the channels as expected
Accuracy	< ±0.25% without software calibration
EMC testing	Passes ESD and Surge

8 Design Files

8.1 Schematics

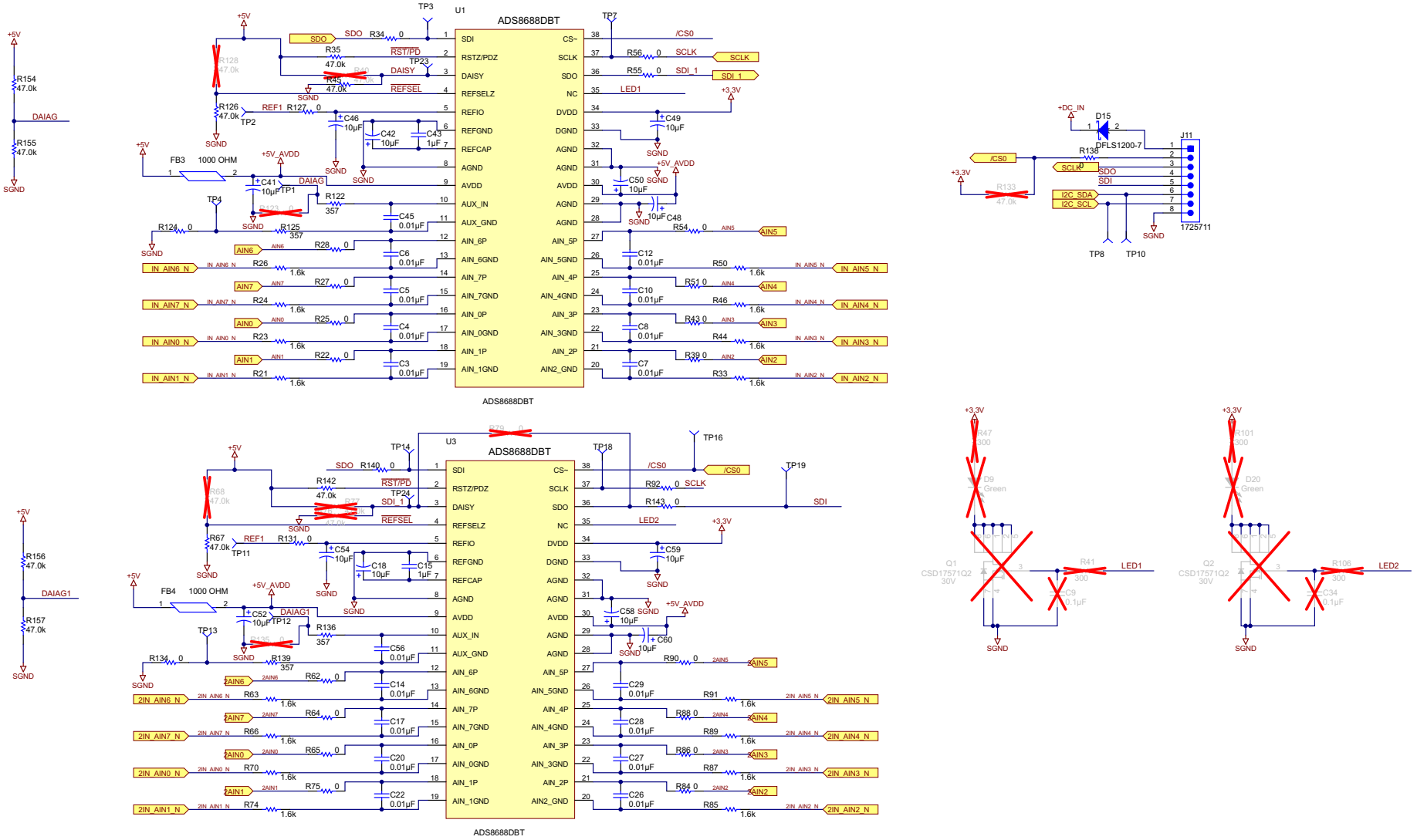


Figure 29. ADC$_1$ and ADC$_2$ Schematic

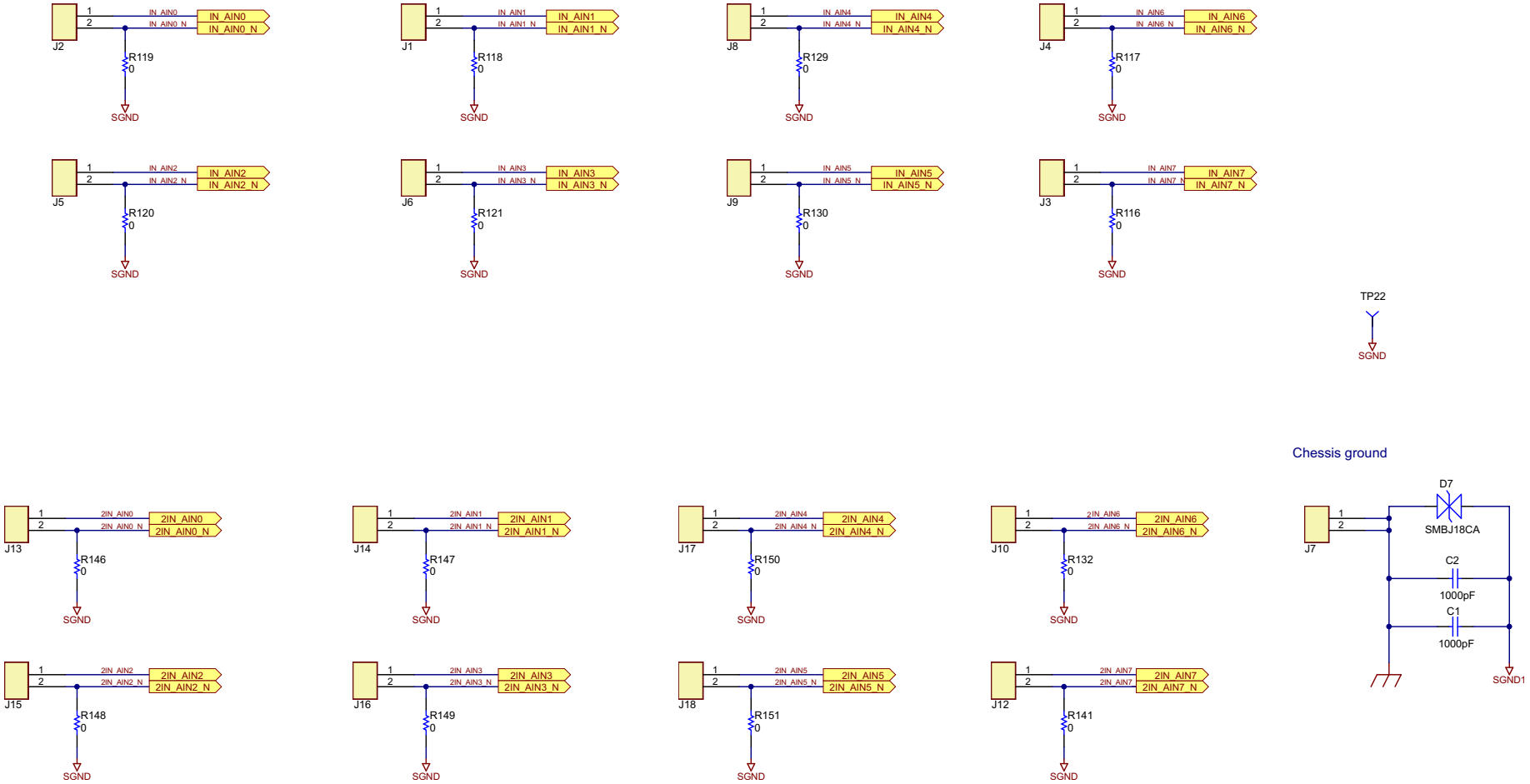


Figure 30. ADC_1 and ADC_2 Inputs Schematic

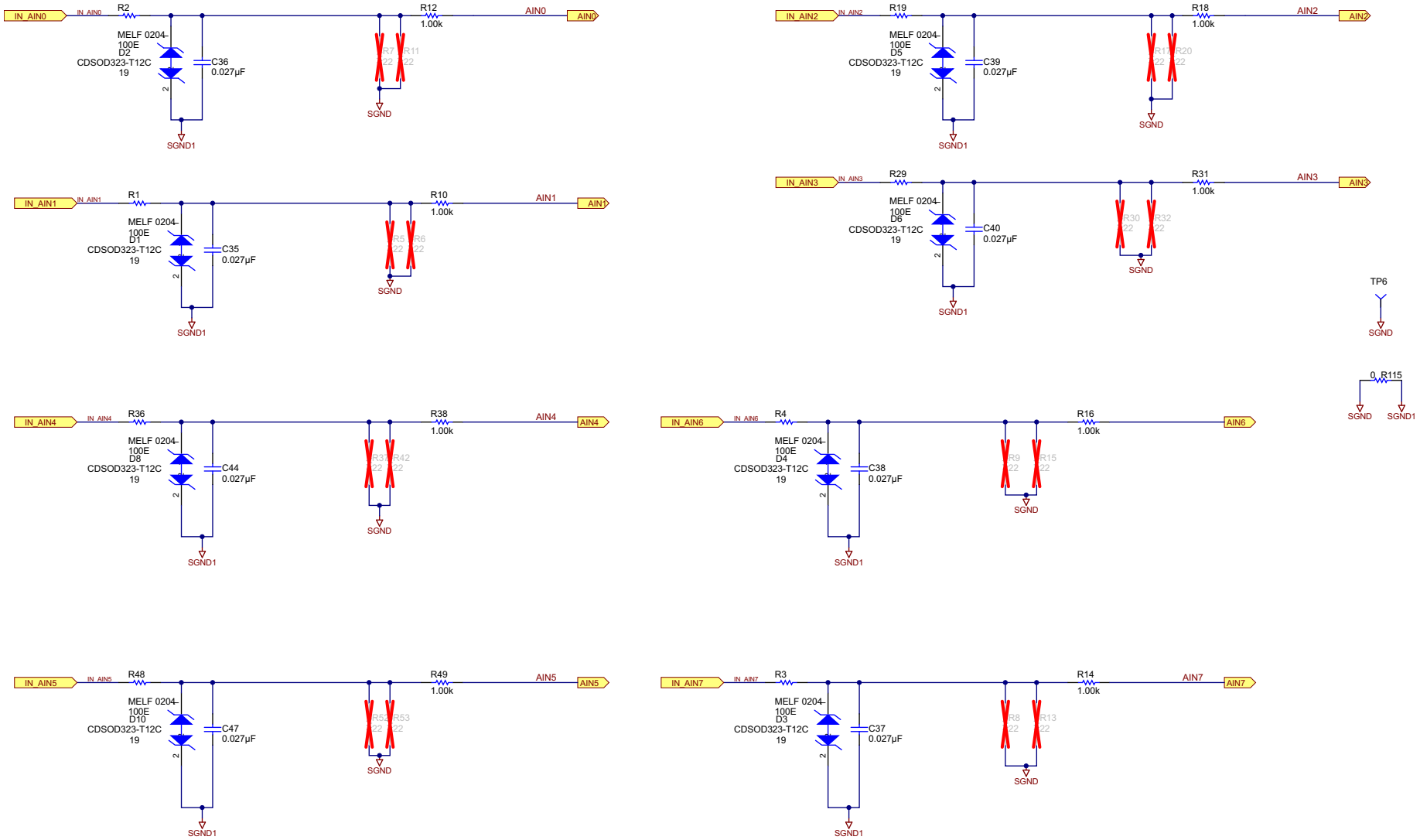


Figure 31. ADC$_1$ Filters Schematic

AN0 to AN3

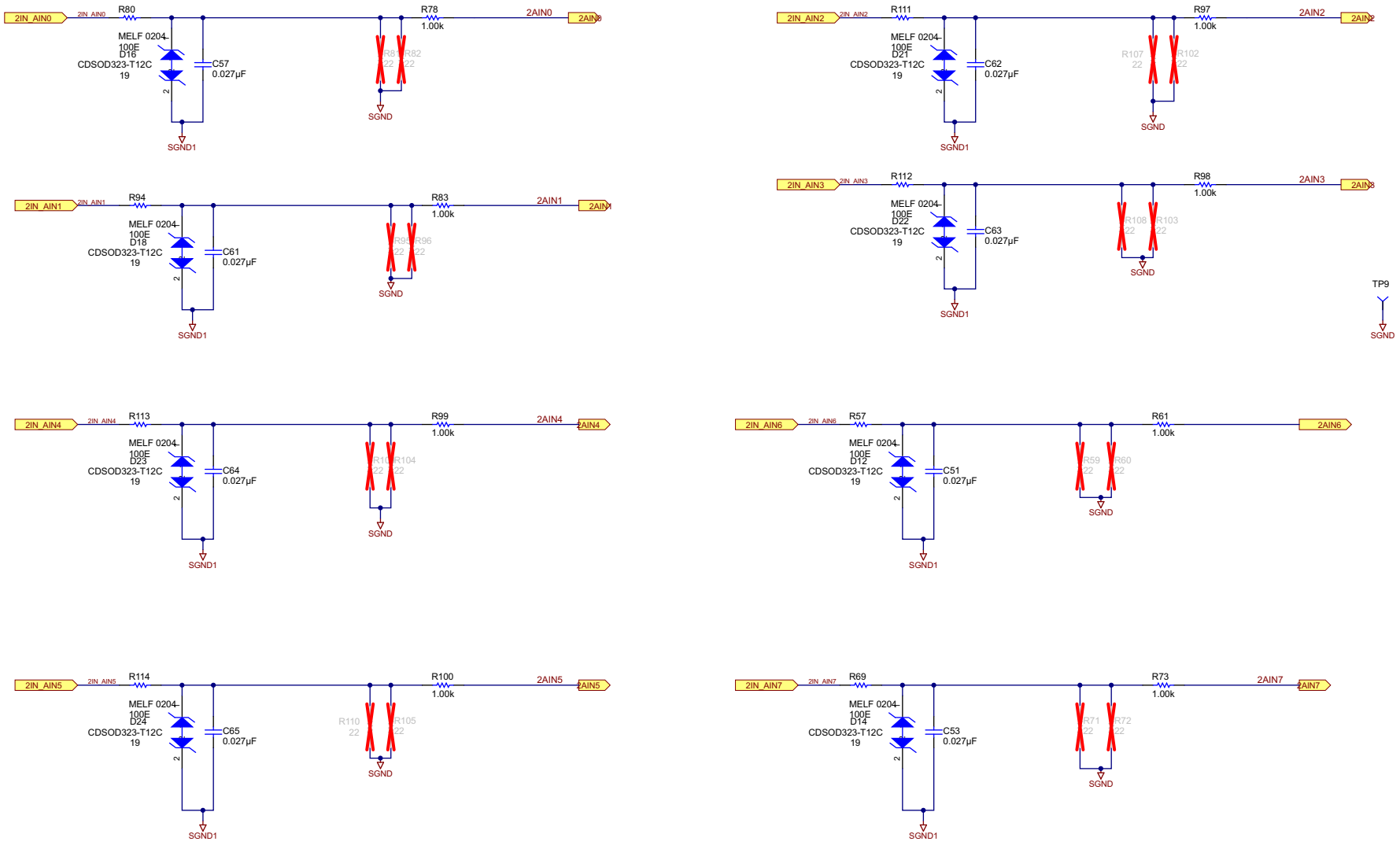


Figure 32. ADC$_2$ Filters Schematic

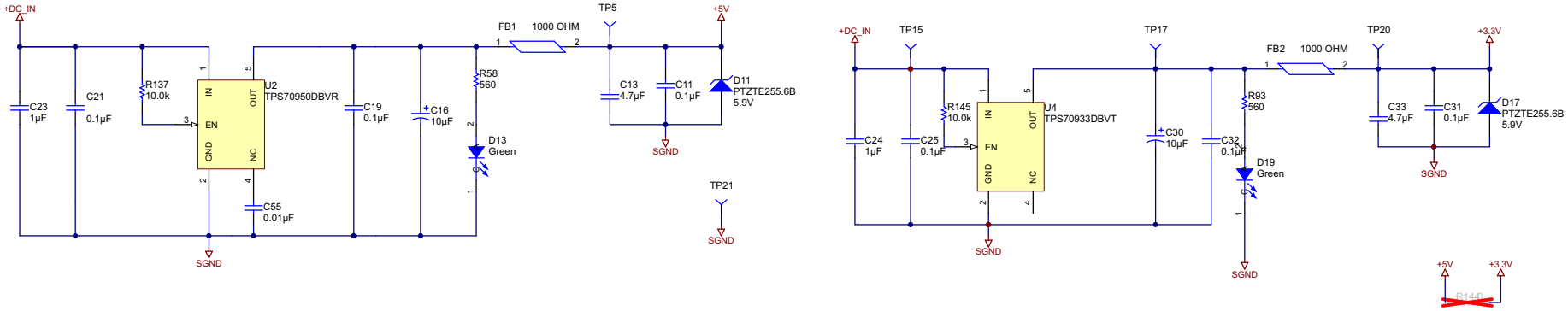


Figure 33. Power Supply Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00307.

Table 33. BOM

ITEM	QTY	REFERENCE	FITTED	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
2	2	C1, C2	Fitted	CAP, CERM, 1000pF, 2kV 10% X7R 1206	Johanson Dielectrics Inc	202R18W102kV4E	603
3	18	C3, C4, C5, C6, C7, C8, C10, C12, C14, C17, C20, C22, C26, C27, C28, C29, C45, C56	Fitted	CAP, CERM, 0.01uF, 100V, ±5%, X7R, 0603	AVX	06031C103JAT2A	603
4	0	C9, C34	Not Fitted	CAP, CERM, 0.1uF, 25V, ±5%, X7R, 0603	AVX	06033C104JAT2A	603
5	6	C11, C19, C21, C25, C31, C32	Fitted	CAP, CERM, 0.1uF, 50V, ±10%, X7R, 0603	Kemet	C0603C104K5RACTU	0805_HV
6	2	C13, C33	Fitted	CAP, CERM, 4.7uF, 50V, ±10%, X5R, 0805	TDK	C2012X5R1H475K125AB	603
7	2	C15, C43	Fitted	CAP, CERM, 1uF, 16V, ±10%, X7R, 0603	Taiyo Yuden	EMK107B7105KA-T	3528-21
8	14	C16, C18, C30, C41, C42, C46, C48, C49, C50, C52, C54, C58, C59, C60	Fitted	CAP, TA, 10 µF, 16 V, ± 10%, 2 ohm, SMD	Vishay-Sprague	T491B106K016AT	805
9	2	C23, C24	Fitted	CAP, CERM, 1uF, 50V, ±10%, X7R, 0805	AVX	08055C105KAT2A	1206
10	16	C35, C36, C37, C38, C39, C40, C44, C47, C51, C53, C57, C61, C62, C63, C64, C65	Fitted	CAP, CERM, 0.027uF, 50V, ±5%, C0G/NP0, 1206	MuRata	GRM3195C1H273JA01D	603
11	1	C55	Fitted	CAP, CERM, 0.01uF, 50V, ±5%, X7R, 0603	Kemet	C0603C103J5RACTU	sod-323
12	16	D1, D2, D3, D4, D5, D6, D8, D10, D12, D14, D16, D18, D21, D22, D23, D24	Fitted	Diode, TVS, ARRAY, 19V, SOD323	Bourns Inc.	CDSOD323-T12C	DIO_SMB_BIAAAA
13	1	D7	Fitted	TVS 18 VOLT 600 WATT BI-DIR SMB	Littelfuse Inc	SMBJ18CA	LED0603AA
14	0	D9, D20	Not Fitted	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z	powerDI123
15	2	D11, D17	Fitted	DIODE ZENER 5.9V 1W PMDS	Rohm Semiconductor	PTZTE255.6B	LED0603AA
16	2	D13, D19	Fitted	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z	powerDI123
17	1	D15	Fitted	Diode, Schottky, 200V, 1A, PowerDI123	Diodes Inc.	DFLS1200-7	FB0603
18	4	FB1, FB2, FB3, FB4	Fitted	FERRITE CHIP 1000 OHM 300MA 0603	TDK Corporation	MMZ1608B102C	FID_TOP_40_80BA
20	4	H1, H2, H3, H4	Fitted	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	CN2_MTB_P100_PD80_D1.1_S5.54X6.5_STACK
21	17	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J12, J13, J14, J15, J16, J17, J18	Fitted	Terminal Block, 4x1, 2.54mm, TH	On Shore Technology Inc	OSTVN02A150	CONN_1725711
22	1	J11	Fitted	Terminal Block, 8x1, 2.54 mm, TH	Phoenix Contact	1725711	Label_650x200
24	0	Q1, Q2	Not Fitted	MOSFET, N-CH, 30V, 22A, SON 2X2 MM	TEXAS INSTRUMENTS	CSD17571Q2	1206

Table 33. BOM (continued)

ITEM	QTY	REFERENCE	FITTED	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
25	16	R1, R2, R3, R4, R19, R29, R36, R48, R57, R69, R80, R94, R111, R112, R113, R114	Fitted	RES 100 OHM.4W 1% 0204 MELF	Vishay Beyschlag	MMA02040C1000FB300	603
26	0	R5, R6, R7, R8, R9, R11, R13, R15, R17, R20, R30, R32, R37, R42, R52, R53, R59, R60, R71, R72, R81, R82, R95, R96, R102, R103, R104, R105, R107, R108, R109, R110	Not Fitted	RES, 22 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060322R0FKEA	603
27	16	R10, R12, R14, R16, R18, R31, R38, R49, R61, R73, R78, R83, R97, R98, R99, R100	Fitted	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K00FKEA	603
28	16	R21, R23, R24, R26, R33, R44, R46, R50, R63, R66, R70, R74, R85, R87, R89, R91	Fitted	RES, 1.6k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K60JNEA	603
29	27	R22, R25, R27, R28, R34, R39, R43, R51, R54, R55, R56, R62, R64, R65, R75, R84, R86, R88, R90, R92, R124, R127, R131, R134, R138, R140, R143	Fitted	RES, 0 ohm,5%, 0.1W, 0603	Yageo America	RC0603JR-070RL	603
30	9	R35, R45, R67, R126, R142, R154, R155, R156, R157	Fitted	RES, 47.0k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW060347K0FKEA	603
31	0	R40, R68, R76, R77, R128, R133	Not Fitted	RES, 47.0k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW060347K0FKEA	603
32	0	R41, R47, R101, R106	Not Fitted	RES, 300 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603300RJNEA	603
33	2	R58, R93	Fitted	RES, 560 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603560RJNEA	603
34	0	R79, R123, R135	Not Fitted	RES, 0 ohm,5%, 0.1W, 0603	Yageo America	RC0603JR-070RL	1206
35	17	R115, R116, R117, R118, R119, R120, R121, R129, R130, R132, R141, R146, R147, R148, R149, R150, R151	Fitted	RES, 0 ohm,5%, 0.25W, 1206	Yageo America	RC1206JR-070RL	603
36	4	R122, R125, R136, R139	Fitted	RES, 357 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603357RFKEA	603
37	2	R137, R145	Fitted	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	805
38	0	R144	Not Fitted	RES, 0 ohm,5%, 0.125W, 0805	Yageo America	RC0805JR-070RL	TP1_PD40_D0.5_S50
39	24	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24	Fitted	Test Point 40mil pad 20mil drill	STD	STD	DBT0038A_M
40	2	U1, U3	Fitted	16 bit 500KSPS 8 Channel SAR ADC	TI	ADS8688DBT	DBV0005A_N
41	1	U2	Fitted	IC REG LDO 5V 0.15A SOT23-5	Texas Instruments	TPS70950DBVR	DBV0005A_N
42	1	U4	Fitted	IC REG LDO 3.3V 0.15A SOT23-5	Texas Instruments	TPS70933DBVT	

8.3 PCB Layout

To download the layer plots, see the design files at TIDA-00307.

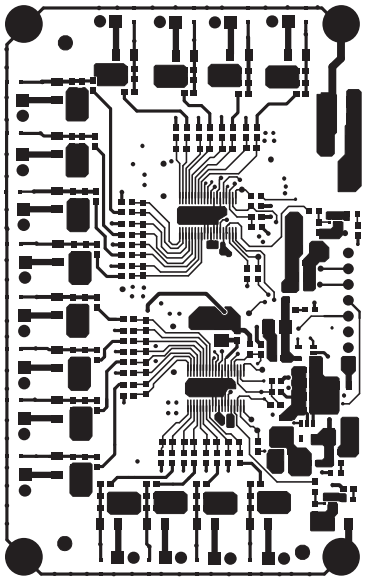


Figure 34. Top Layer

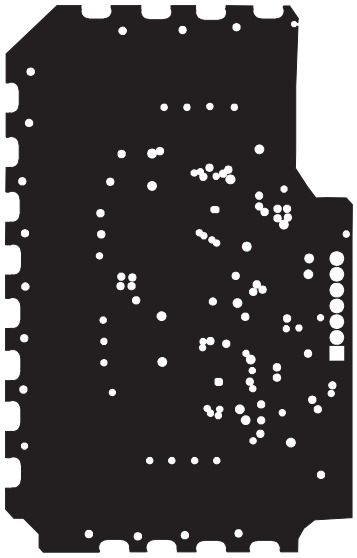


Figure 35. Ground Layer

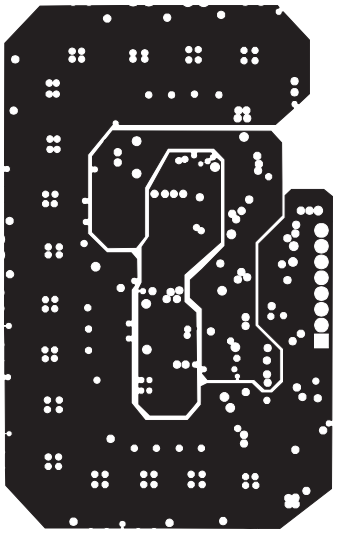


Figure 36. Power Layer

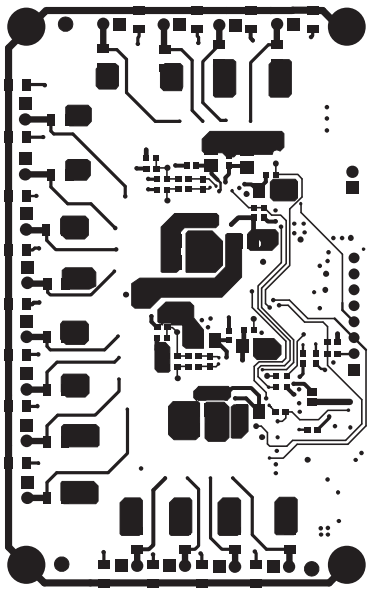


Figure 37. Bottom Layer

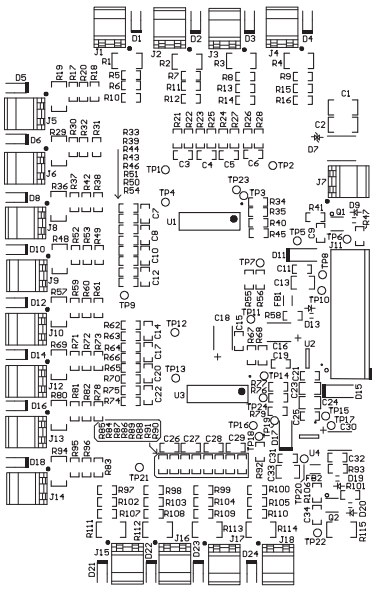


Figure 38. Top Overlay

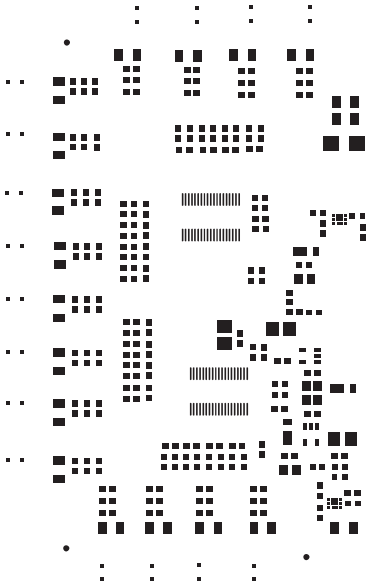


Figure 39. Top Paste

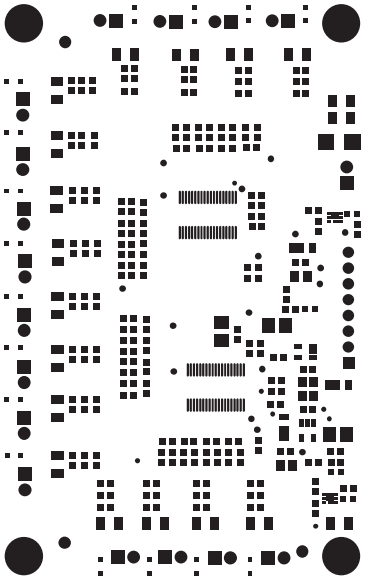


Figure 40. Top Solder

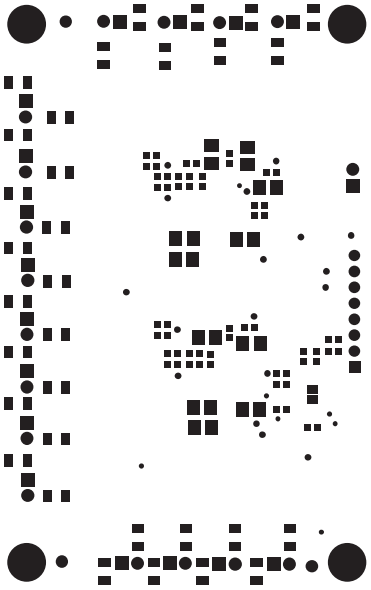


Figure 41. Bottom Solder

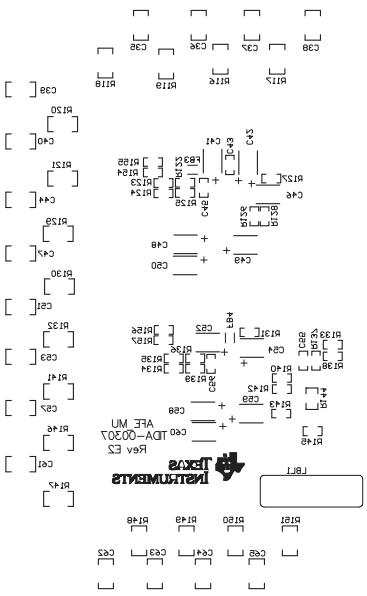


Figure 42. Bottom Overlay

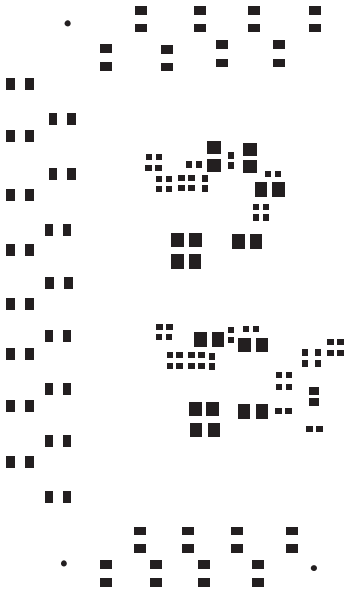


Figure 43. Bottom Paste

8.4 Gerber Files

To download the Gerber Files, see the design files at TIDA-00307.

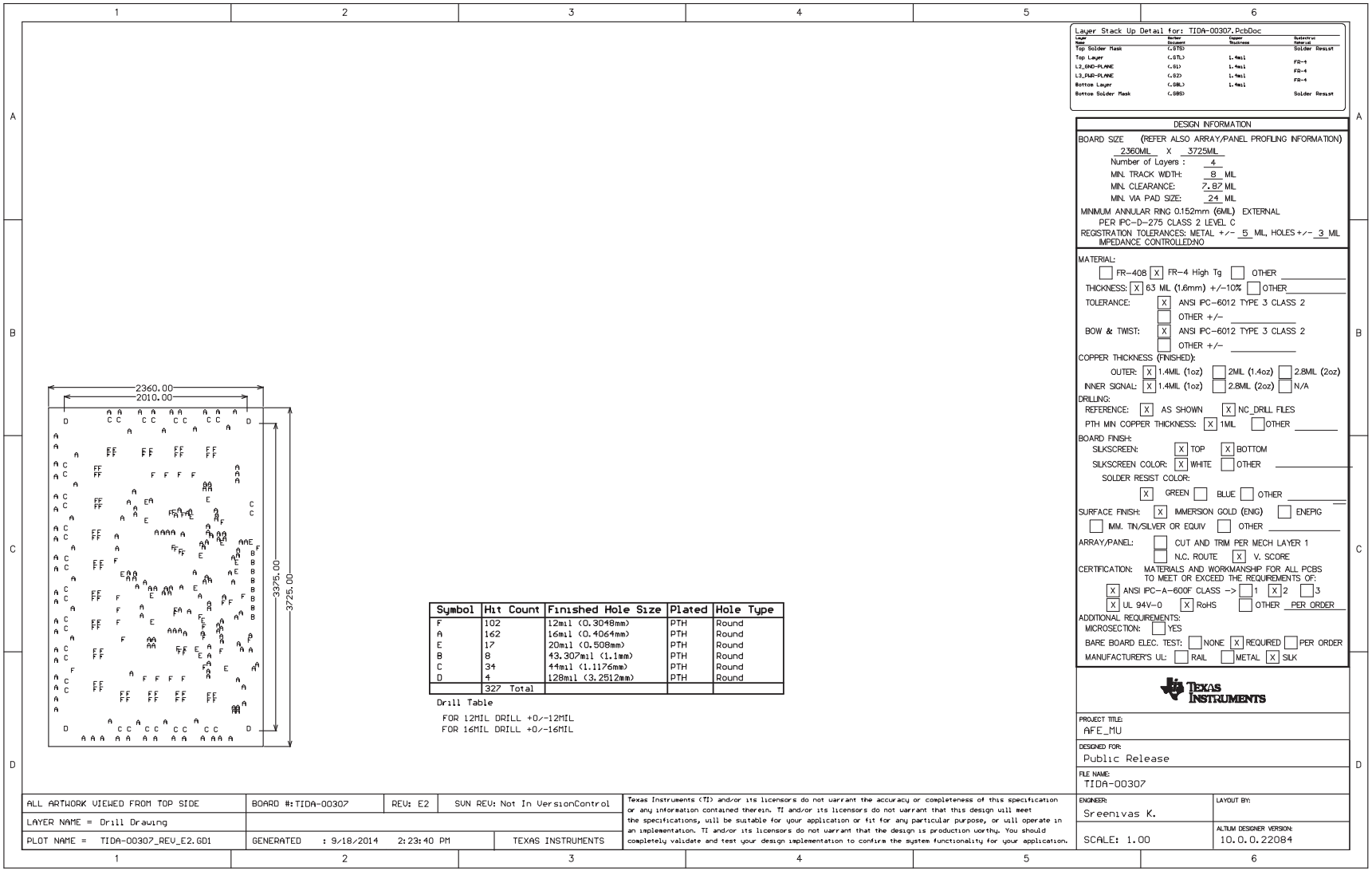


Figure 44. Fabrication Layer

8.5 Altium Project

To download the Altium project files, see the design files at TIDA-00307.

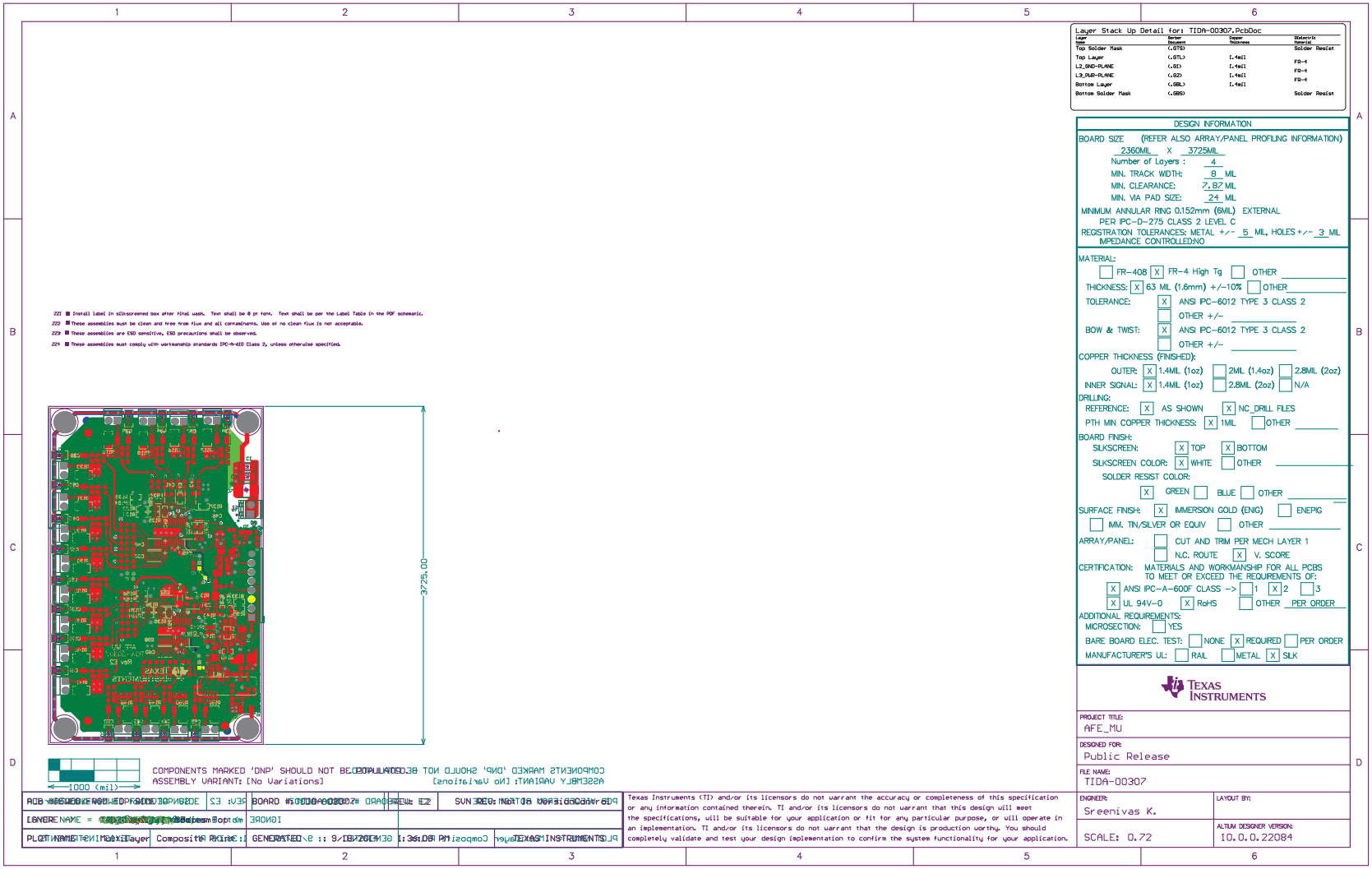


Figure 45. Altium Project

8.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00307

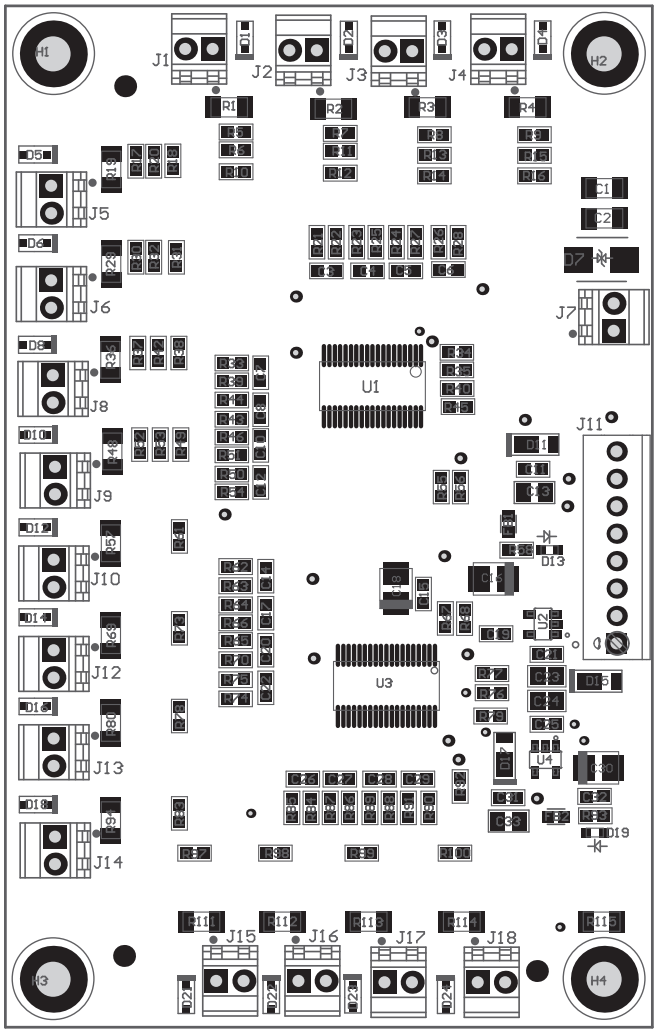


Figure 46. Top Layer

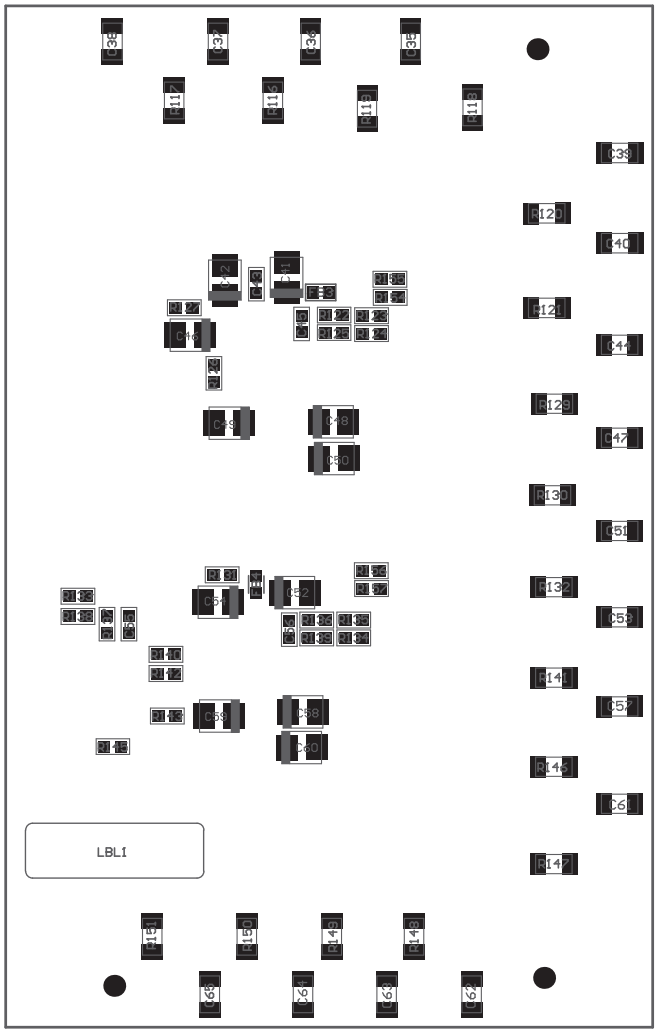


Figure 47. Bottom Layer

9 References

http://www.google.com/patents/US20140074415

10 Terminology

FTU— Feeder Terminal Unit

DTU— Distribution Terminal Unit

RTU— Remote Terminal Unit

11 About the Author

KALLIKUPPA MUNIYAPPA SREENIVASA is a systems architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Sreenivasa brings to this role his experience in high-speed digital and analog systems design. Sreenivasa earned his bachelor of electronics (BE) in electronics and communication engineering (BE-E&C) from VTU, Mysore, India.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2014) to A Revision	Page
• Changed title from *Sensor Inputs AFE for Merging Unit and Protection Relays*	1
• Changed the design description on the front page	1
• Added ADS8698 to Design Resources	1
• Added ADS8668 to Design Resources	1
• Added ADS8688A to Design Resources	1
• Added ADS8678 to Design Resources	1
• Added "Design compatible with ADS8688A, ADS8678, ADS8668" to Design Features	1
• Deleted "±10.24-V, ±5.12-V, and ±2.56-V programmable input ranges" from Design Features	1
• Added "Based on ADC selection, ±10.24 V, ±5.12 V, ±2.56 V, ±1.28 V, and ±0.64 V programmable input ranges available for accurate measurement of low amplitude input signals" to Design Features	1
• Added "AC sensor inputs with 50, 60, or 400 Hz can be used; Ranges compatible to electronic current transformer output requirements as per IEC60044-8" to Design Features	1
• Added Power Quality Analyzer to Featured Applications	1
• Added FTU, DTU, or RTU to Featured Applications	1
• Added Section 4.8	20
• Added Section 10	50

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